

Mullard

Book 1 Part 2

Transistors BFQ10 to OC36
including 2N numbers

September 1974



Mullard technical handbook

Book one

Semiconductor devices

Part two

Transistors BFQ10 to OC36
including 2N numbers

September 1974



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Book 1 comprises the following parts—

- Part 1 Transistors and accessories
- Part 2 Transistors and accessories
- Part 3 Diodes, photodiodes and phototransistors
- Part 4 Rectifier diodes, rectifier diode stacks, medium and high-power voltage regulator diodes, transient suppressor diodes
- Part 5 Thyristors, thyristor stacks and accessories
- Part 6 Digital integrated circuits
- Part 7 Linear integrated circuits

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BOOK 1 (Part 2)

SEMICONDUCTOR DEVICES

Transistors

BFQ10 to OC36

(including 2N types)

**MULLARD LTD., MULLARD HOUSE, TORRINGTON PLACE,
LONDON, WC1E 7HD**

Telephone 01-580 6633

Telex: 264341

DATA HANDBOOK SYSTEM

The Mullard data handbook system is made up of three sets of books, each comprising several parts.

The three sets of books, easily identifiable by the colours on their covers, are as follows:

Book 1	(blue)	Semiconductor devices and integrated circuits
Book 2	(orange)	Valves and tubes
Book 3	(green)	Passive components, materials, and assemblies.

Each part is completely reviewed annually; revised and reprinted where necessary. Revisions to previous data are indicated by an arrow in the margin.

The data contained in these books are as accurate and up to date as it is reasonably possible to make them at the time of going to press. It must however be understood that no guarantee can be given here regarding the availability of the various devices or that their specifications may not be changed before the next edition is published.

The devices on which full data are given in these books are those around which we would recommend equipment to be designed. Where appropriate, other types no longer recommended for new equipment designs, but generally available for equipment production are listed separately with abridged data. Data sheets for these types may be obtained on request. Older devices on which data may still be obtained on request are also included in the index of the appropriate part of each book.

Requests for information on the data handbook system and for individual data sheets should be made to

Central Technical Services
Mullard Limited
New Road
Mitcham
Surrey CR4 4XY

Telephone: 01-648 3471 Telex: 22194

Information regarding price and availability of devices must be obtained from our authorised agents or from our representatives.

SELECTION GUIDE

1. SMALL/MEDIUM SIGNAL TRANSISTORS

Germanium types

Type No.	N-P-N	P-N-P	General Purpose	Switching	Low Noise	V _{CE} max (V)			h _{FE} min			P _{tot} max (mW)	Case
						≥ 15	≥ 30	≥ 60	≤ 30	< 60	≥ 60		
AC127	★		★				★			★		340	TO-1
AC128		★	★				★				★	1000	TO-1
AC176	★		★				★			★		700	TO-1
AC187	★		★			★					★	1000	TO-1
AC188		★	★			★					★	1000	TO-1

P-N-P Silicon alloy types

Type No.	General Purpose	Switching	V _{CE} max (V)			h _{FE} min			P _{tot} max (mW)	Case
			≥ 15	≥ 30	≥ 60	≤ 30	< 60	≥ 60		
BCY30	★	★			★	★			250	TO-5
BCY31	★	★			★		★		250	TO-5
BCY32	★	★			★			★	250	TO-5
BCY33	★	★		★		★			250	TO-5
BCY34	★	★		★			★		250	TO-5
BCY38	★	★		★		★			410	TO-5
BCY39	★	★			★	★			410	TO-5
BCY40	★	★		★			★		410	TO-5
BCY54	★	★		★			★		410	TO-5

SMALL/MEDIUM SIGNAL TRANSISTORS (cont.)

N-P-N Silicon planar types

Type No.	General Purpose	Switching	Low Noise	$V_{CE\ max}$ (V)			f_T (GHz)			$P_{tot\ max}$ (mW)	Case
				≥ 15	≥ 30	≥ 60	< 0.4	< 1.0	> 1.0		
BC107†	★	★			★		★			300	TO-18
BC108†	★	★		★			★			300	TO-18
BC109†	★		★	★			★			300	TO-18
BC147	★				★		★			300	lock-fit
BC148	★			★			★			300	lock-fit
BC149	★		★	★			★			300	lock-fit
BC547	★				★		★			300	TO-92
BC548	★			★			★			300	TO-92
BC549	★		★	★			★			300	TO-92
BCW31R	★			★			★			200	μ min
BCW32R	★			★			★			200	μ min
BCW33R	★			★			★			200	μ min
BCW71R	★				★		★			200	μ min
BCW72R	★				★		★			200	μ min
BCX19	★	★			★		★			310	μ min
BCX20	★	★		★			★			310	μ min
BCX31	★					★	★			1000	lock-fit
BCX32	★					★	★			1000	lock-fit
BCX33	★				★		★			1000	lock-fit
BCX34	★				★		★			1000	lock-fit
BF180	★		★					★		150	TO-72
BF181	★		★	★				★		150	TO-72
BF194	★		★	★			★			220	lock-fit
BF195	★		★	★			★			220	lock-fit
BF196	★		★	★			★			250	lock-fit
BF197	★			★				★		250	lock-fit
BF200	★		★	★			★			150	TO-72
BF336	★					★	★			3000	TO-39
BF337	★					★	★			3000	TO-39
BF338	★					★	★			3000	TO-39
BF355		★				★	★			3000	TO-39
BF362	★			★				★		120	T pack
BF363	★			★				★		120	T pack
BFR63	★		★	★					★	3500	Capstan
BFR64	★		★	★					★	3500	Capstan
BFR90	★		★	★					★	180	T pack
BFR91	★		★	★					★	180	T pack

†Also available to BS 9365-F112

SMALL/MEDIUM SIGNAL TRANSISTORS (cont.) **N-P-N Silicon planar types (cont.)**

Type No.	General Purpose	Switching	Low Noise	$V_{CE \text{ max}}$ (V)			f_T (GHz)			$P_{\text{tot max}}$ (mW)	Case
				≥ 15	≥ 30	≥ 60	< 0.4	< 1.0	> 1.0		
BFR92	★		★	★					★	180	μ min
BFR93	★		★						★	180	μ min
BFS17R	★		★	★					★	200	μ min
BFS20R	★			★				★		200	μ min
BFT24	★		★	+					★	30	T pack
BFT25	★		★	+					★	30	μ min
BFW16A	★		★	★					★	1500	TO-39
BFW17A	★			★					★	1500	TO-39
BFW30	★		★	★					★	250	TO-72
BFX84	★	★				★	★			800	TO-5
BFX85	★	★				★	★			800	TO-5
BFX86	★	★			★		★			800	TO-5
BFX89	★		★	★					★	200	TO-72
BFY50†	★	★				★	★			800	TO-5
BFY51†	★	★				★	★			800	TO-5
BFY52†	★	★			★		★			800	TO-5
BFY53	★			★			★			800	TO-5
BFY90	★		★	★					★	200	TO-72
BSS40		★			★		★			360	TO-18
BSS41		★			★		★			360	TO-18
BSV52R		★			★			★		200	μ min
BSW66		★				★	★			800	TO-5
BSW67		★				★	★			800	TO-5
BSW68		★				★	★			800	TO-5
BSX19	★	★			★			★		360	TO-18
BSX20	★	★			★			★		360	TO-18
BSX21	★					★	★			300	TO-18
BSX59		★			★		★			800	TO-5
BSX60		★		★			★			800	TO-5
BSX61		★			★		★			800	TO-5
BSY95A		★		★			★			300	TO-18
2N1613	★	★				★	★			800	TO-5
2N1711	★	★			★		★			800	TO-5
2N2297	★	★			★		★			800	TO-5
2N2369A		★		★				★		360	TO-18
2N3053		★			★		★			800	TO-5

†Also available to BS 9365-F012

‡ $V_{CE0 \text{ max}} = 5V$

SMALL/MEDIUM SIGNAL TRANSISTORS (cont.) **P-N-P Silicon planar types**

Type No.	General Purpose	Switching	Low Noise	$V_{CE\ max}$ (V)			f_T (MHz)			$P_{tot\ max}$ (mW)	Case
				≥ 15	≥ 30	≥ 60	< 200	< 400	> 400		
BC157	★				★		★			300	lock-fit
BC158	★			★			★			300	lock-fit
BC159	★		★	★			★			300	lock-fit
BC327	★				★		★			625	Plastic
BC328	★			★			★			625	Plastic
BC557	★				★		★			300	TO-92
BC558	★			★			★			300	TO-92
BC559	★	★		★			★			300	TO-92
BCW29R	★		★	★			★			200	μ min
BCW30R	★		★	★			★			200	μ min
BCW69R	★				★		★			200	μ min
BCW70R	★				★		★			200	μ min
BCX17	★	★			★		★			310	μ min
BCX18	★	★		★			★			310	μ min
BCX35	★					★	★			1000	lock-fit
BCX36	★					★	★			1000	lock-fit
BCX37	★				★		★			1000	lock-fit
BCY70†	★	★	★		★			★		350	TO-18
BCY71†	★		★		★			★		350	TO-18
BCY72†	★	★	★	★				★		350	TO-18
BF324	★		★		★				★	250	TO-92
BF450	★		★		★			★		250	TO-92
BF451	★		★		★			★		250	TO-92
BFX29‡	★	★				★	★			600	TO-5
BFX30‡		★				★				600	TO-5
BFX87	★	★			★		★			600	TO-5
BFX88	★	★			★		★			600	TO-5
BSV68		★				★	★			250	TO-18
2N2904	★	★			★			★		600	TO-5
2N2904A	★	★				★		★		600	TO-5
2N2905	★	★			★			★		600	TO-5
2N2905A	★	★				★		★		600	TO-5
2N2906	★	★			★			★		400	TO-18
2N2906A	★	★				★		★		400	TO-18
2N2907	★	★			★			★		400	TO-18
2N2907A	★	★				★		★		400	TO-18

† Also available to BS9365-F009

‡ Also available to BS9365-F010/F011

2. L.F./H.F. POWER TRANSISTORS

Silicon types

Type No.	N-P-N	P-N-P	General Purpose	Switching	H.F.	V _{CE} max (V)		h _{FE} min	P _{tot} max (W)	Case
						≥ 35	≥ 70	≥ 30		
BD131	★		★		★	★		★	15	TO-126
BD132		★	★		★	★		★	15	TO-126
BD133	★		★		★	★		★	15	TO-126
BD135	★		★		★	★		★	6.5	TO-126
BD136		★	★		★	★		★	6.5	TO-126
BD137	★		★		★	★		★	6.6	TO-126
BD138		★	★		★	★		★	6.5	TO-126
BD139	★		★		★		★	★	6.5	TO-126
BD140		★	★		★		★	★	6.5	TO-126
BD181	★		★			★			117	TO-3
BD182	★		★			★			117	TO-3
BD183	★		★				★		117	TO-3
BD184	★		★				★		117	TO-3
BD201	★		★			★		★	55	Plastic
BD202		★	★			★		★	55	Plastic
BD203	★		★			★		★	55	Plastic
BD204		★	★			★		★	55	Plastic
BD232	★		★		★	★	300V		7	TO-126
BD233	★		★			★			25	TO-126
BD234		★	★			★			25	TO-126
BD235	★		★			★			25	TO-126
BD236		★	★			★			25	TO-126
BD237	★		★				★		25	TO-126
BD238		★	★				★		25	TO-126
BD433	★		★					★	36	TO-126
BD434		★	★					★	36	TO-126
BD435	★		★					★	36	TO-126
BD436		★	★					★	36	TO-126
BD437	★		★			★		★	36	TO-126
BD438		★	★			★		★	36	TO-126
BDX35	★			★	★	★		★	15	TO-126
BDX36	★			★	★	★		★	15	TO-126
BDX37	★			★	★		★	★	15	TO-126
BDY20	★		★	★		★			115	TO-3
BDY38	★		★			★		★	115	TO-3

L.F./H.F. POWER TRANSISTORS (cont.)

Silicon types (cont.)

Type No.	N-P-N	P-N-P	General Purpose	Switching	H.F.	V _{CE} max (V)		h _{FE} min ≥ 30	P _{tot} max (W)	Case
						≥ 35	≥ 70			
BDY90	★		★	★	★		★	★	40	TO-3
BDY91	★		★	★	★		★	★	40	TO-3
BDY92	★		★	★	★	★		★	40	TO-3
BDY93	★		★	★			★		30	TO-3
BDY94	★		★	★			★		30	TO-3
BDY95	★		★	★			★		30	TO-3
BDY96	★		★	★			350V		40	TO-3
BDY97	★		★	★			300V		40	TO-3
BDY98	★		★	★			250V		40	TO-3
BSV64	★			★	★	★		★	5	TO-39
BU126	★		★				750V		30	TO-3
BU133	★		★				750V		30	TO-3
BU204	★		★				1300V		10	TO-3
BU205	★		★				1500V		10	TO-3
BU206	★		★				1700V		10	TO-3
BU207	★		★				1300V		12.5	TO-3
BU208	★		★				1500V		12.5	TO-3
BU209	★		★				1700V		12.5	TO-3
2N3055	★		★			★			115	TO-3
2N3442	★		★				★		117	TO-3
2N4347	★		★				★		100	TO-3

Germanium types

Type No.	N-P-N	P-N-P	General Purpose	Switching	H.F.	V _{CE} max (V)			h _{FE} min ≥ 40	P _{tot} max (W)	Case
						≥ 15	≥ 30	≥ 60			
AD149		★	★				★			22.5	TO-3
AD161	★		★			★			★	4	SO-55
AD162		★	★			★			★	6	SO-55
OC28		★	★	★				★		30	TO-3
OC29		★	★	★			★		★	30	TO-3
OC35		★	★	★			★			30	TO-3
OC36		★	★	★				★		30	TO-3

3. R.F. POWER DEVICES

N-P-N Transistors

Type No.	V.H.F.	U.H.F.	V _{CE} max (V)		P _o (C.W.) (W at MHz)				Case
			≥ 18	≥ 33	175	400	470	1000	
BLX13	★			★	25†				Capstan
BLX14	★			★	50†				Stripline
BLX65	★	★	★		2		2		TO-39
BLX66	★	★	★		3		2.5		Capstan
BLX67	★	★	★		3		3		Capstan
BLX69		★	★				20		Capstan
BLX91		★		★			1.4	1.4	Capstan
BLX92		★		★			3	2.5	Capstan
BLX93		★		★			8	5	Capstan
BLX94		★		★			20		Capstan
BLY33	★			★	2‡				TO-39
BLY34	★		★		3				TO-39
BLY35	★			★	7				TO-60
BLY36	★		★		13				TO-60
BLY53A	★	★	★		7.2		7		Capstan
BLY55	★		★		4				TO-60
BLY83	★			★	7				Capstan
BLY84	★		★		13				Capstan
BLY85	★		★		0.2				Capstan
BLY89A	★		★		25				Capstan
BLY90	★		★		50				Stripline
BLY93A	★			★	25				Capstan
BLY94	★			★	50				Stripline
BLY97	★			★	0.14				Capstan
2N3375	★	★	★	★	7.5§	3			TO-60
2N3553	★			★	2.5				TO-60
2N3632	★			★	13.5				TO-60
2N3866	★	★		★		1			TO-39
2N4427	★	★	★		1		0.4		TO-39

† At 70MHz

‡ A.M. (Carrier)

§ At 100MHz

Broad Band U.H.F. Amplifier Modules

Type No.	Frequency range (MHz)	V. supply (V)	P _o min at P _{dr}	
			(W)	(W)
BGY22	380-512	13.5	2.5	0.05
BGY22A	420-480	12.5	2.5	0.05
BGY23	380-512	13.5	7	2.5
BGY23A	420-480	12.5	7	2.5

4. DARLINGTON TRANSISTORS

Type No.	N-P-N	P-N-P	V _{CE} max (V)				h _{FE} min at I _C		P _{tot} max	Case
			45	60	80	100	(A)			
							(W)			
BCX21	★		★				2000	0.15	3.5	TO-39
BDX42	★		★				1500	0.5	5	TO-126
BDX43	★			★			1500	0.5	5	TO-126
BDX44	★				★		1500	0.5	5	TO-126
BSS50	★		★				1500	0.5	5	TO-39
BSS51	★			★			1500	0.5	5	TO-39
BSS52	★				★		1500	0.5	5	TO-39
BD262		★		★			750	1.5	36	TO-126
BD262A		★			★		750	1.5	36	TO-126
BD262B		★				★	750	1.5	36	TO-126
BD263	★			★			750	1.5	36	TO-126
BD263A	★				★		750	1.5	36	TO-126
BD263B	★					★	750	1.5	36	TO-126
BDX62		★		★			1000	3	90	TO-3
BDX62A		★			★		1000	3	90	TO-3
BDX62B		★				★	1000	3	90	TO-3
BDX63	★			★			1000	3	90	TO-3
BDX63A	★				★		1000	3	90	TO-3
BDX63B	★					★	1000	3	90	TO-3
BDX64		★		★			1000	5	117	TO-3
BDX64A		★			★		1000	5	117	TO-3
BDX64B		★				★	1000	5	117	TO-3
BDX65	★			★			1000	5	117	TO-3
BDX65A	★				★		1000	5	117	TO-3
BDX65B	★					★	1000	5	117	TO-3

5. FIELD-EFFECT TRANSISTORS

(n-channel, depletion)

Type No.	Junction gate	Insulated gate	General purpose	Switching	Low noise	Low 'On' resistance	U.H.F.	V _{DSmax} (V)	Case
BF245A	★		★		★			30	TO-92
BF245B	★		★		★			30	TO-92
BF245C	★		★		★			30	TO-92
BFQ10		★	★		★			30	TO-71
BFQ11		★	★		★			30	TO-71
BFQ12		★	★		★			30	TO-71
BFQ13		★	★		★			30	TO-71
BFQ14		★	★		★			30	TO-71
BFQ15		★	★		★			30	TO-71
BFQ16		★	★		★			30	TO-71
BFR29		★	★		★			30	TO-72
BFR30	★		★					25	μ min
BFR31	★		★					25	μ min
BFS28		★	★		★		★	20	TO-72
BFW10	★		★		★			30	TO-72
BFW11	★		★		★			30	TO-72
BFW61	★		★					25	TO-72
BSV78	★			★		★		40	TO-18
BSV79	★			★		★		40	TO-18
BSV80	★			★		★		40	TO-18
BSV81		★		★		★		30	TO-72
2N3823	★		★		★			30	TO-72
2N3966	★			★				30	TO-72
2N4091	★			★		★		40	TO-18
2N4092	★			★		★		40	TO-18
2N4093	★			★				40	TO-18
2N4391	★			★		★		40	TO-18
2N4392	★			★		★		40	TO-18
2N4393	★			★				40	TQ-18
2N4856	★			★		★		40	TO-18
2N4857	★			★		★		40	TO-18
2N4858	★			★		★		40	TO-18
2N4859	★			★		★		30	TO-18
2N4860	★			★		★		30	TO-18
2N4861	★			★		★		30	TO-18

6. MICROMINIATURE TRANSISTORS

Type No.	N-P-N	P-N-P	General Purpose	Switching	Low Noise	V _{CE} max (V)			f _T (MHz)			P _{tot} max (mW)
						≥ 15	≥ 30	≥ 60	< 200	< 500	> 1000	
BCW29R		★	★		★	★			★			200
BCW30R		★	★		★	★			★			200
BCW31R	★		★			★				★		200
BCW32R	★		★			★				★		200
BCW33R	★		★			★				★		200
BCW69R		★	★				★		★			200
BCW70R		★	★				★		★			200
BCW71R	★		★				★			★		200
BCW72R	★		★				★			★		200
BCX17		★	★	★			★		★			310
BCX18		★	★	★		★			★			310
BCX19	★		★	★			★		★			310
BCX20	★		★	★		★			★			310
BFR30†			★			★						200
BFR31†			★			★						200
BFR92	★		★		★	★					★	180
BFR93	★		★		★						★	180
BFS17R	★		★		★	★					★	200
BFS20R	★		★			★				★		200
BFT25	★		★		★	†					★	30
BSV52R	★			★		★			★			200

†Field effect transistors

‡V_{CE0} max=5V

GENERAL SECTION

A





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Section I. Type Nomenclature

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Section 1

Mullard semiconductor devices are registered by Pro Electron.
The type nomenclature of a discrete device or, in certain cases, of a range of devices, consists of two letters followed by a serial number. The serial number may consist of three figures or of one letter and two figures depending on the main application of the device.

The first letter indicates the semiconductor material used:

- A — germanium
- B — silicon
- C — compound materials such as gallium arsenide
- D — compound materials such as indium antimonide
- R — compound materials such as cadmium sulphide

The second letter indicates the general function of the device:

- A — detection diode, high speed diode, mixer diode.
- B — variable capacitance diode
- C — transistor for a.f. applications (not power types)
- D — power transistor for a.f. applications
- E — tunnel diode
- F — transistor for r.f. applications (not power types)
- G — multiple of dissimilar devices; miscellaneous devices
- L — power transistor for r.f. applications
- N — photo-coupler
- P — radiation sensitive device such as photodiode, phototransistor, photo-conductive cell, or radiation detector diode
- Q — radiation generating device such as light-emitting diode
- R — controlling and switching device (e.g. thyristor) having a specified breakdown characteristic (not power types)
- S — transistor for switching applications (not power types)
- T — controlling and switching power device (e.g. thyristor) having a specified breakdown characteristic
- U — power transistor for switching applications
- X — multiplier diode such as varactor or step recovery diode
- Y — rectifier diode, booster diode, efficiency diode
- Z — voltage reference or voltage regulator diode, transient suppressor diode

The remainder of the type number is a **serial number** indicating a particular design or development and is in one of the following two groups:

- (a) Devices intended primarily for use in consumer applications (radio and television receivers, audio amplifiers, tape recorders, domestic appliances, etc.).

The serial number consists of three figures.

- (b) Devices intended mainly for applications other than (a), e.g. industrial, professional and transmitting equipments.

The serial number consists of one letter (Z, Y, X, W, etc.) followed by two figures.

Range Numbers

Where there is a range of variants of a basic type of rectifier diode, thyristor or voltage regulator diode the type number as defined above is often used to identify the range; further letters and figures are added after a hyphen to identify individual types within the range. These additions are as follows:

Rectifier Diodes and Thyristors

The group of figures indicates the rated repetitive peak reverse voltage, V_{RRM} , or the rated repetitive peak off-state voltage, V_{DRM} , whichever value is lower, in volts for each type.

The final letter R is used to denote a reverse polarity version (stud-anode) where applicable. The normal polarity version (stud cathode) has no special final letter.

Voltage Regulator Diodes, Transient Suppression Diodes

The first letter indicates the nominal percentage tolerance in the operating voltage V_Z .

A — $\pm 1\%$
B — $\pm 2\%$
C — $\pm 5\%$

D — $\pm 10\%$
E — $\pm 15\%$

The letter is omitted on transient suppressor diodes.

The group of figures indicates the typical operating voltage V_Z for each type at the nominal operating current I_Z rating of the range. For transient suppressor diodes the figure indicates the maximum recommended standoff voltage V_R .

The letter V is used to denote a decimal sign.

The final letter R is used to denote a reverse polarity version (stud anode) where applicable. The normal polarity version (stud cathode) has no special final letter.

Examples:

- | | |
|------------|---|
| BF362 | Silicon r.f. transistor intended primarily for 'consumer' applications. |
| ACY17 | Germanium a.f. transistor primarily for 'industrial' applications. |
| BTW24-800R | Silicon thyristor for 'industrial' applications. In BTW24 range with 800V maximum repetitive peak voltage, reverse polarity, stud connected to anode. |
| BZY88-C5V6 | Silicon voltage regulator diode for 'industrial' applications. In BZY88 range with 5.6V operating voltage $\pm 5\%$ tolerance. |
| RPY71 | Photoconductive cell for 'industrial' applications. |

OLD SYSTEM

Some earlier semiconductor diodes and transistors have type numbers consisting of two or three letters followed by a group of one, two or three figures.

The first letter is always 'O', indicating a semiconductor device.

The second (and third) letter(s) indicate the general class of device:

A — diode or rectifier	C — transistor
AP — photodiode	CP — phototransistor
AZ — voltage regulator diode	

The group of figures is a serial number indicating a particular design or development.

Section II

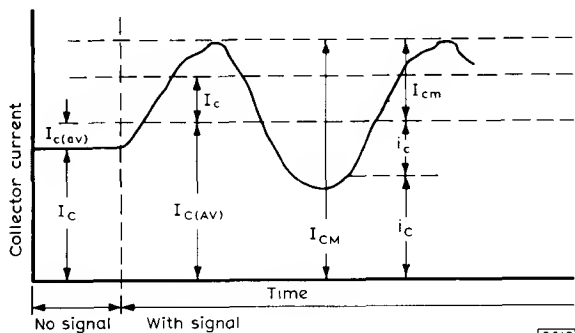
LIST OF SYMBOLS FOR SEMICONDUCTOR DEVICES

These symbols are based on British Standard Specification No. 3363: "Letter Symbols for Semiconductor Devices." A full description of the system is contained in this publication.

QUANTITY SYMBOLS

V Voltage
I Current
P Power

$\left. \begin{matrix} i \\ v \\ p \end{matrix} \right\}$	with subscripts	$\left\{ \begin{matrix} e \\ b \\ c \end{matrix} \right\}$	instantaneous value of the varying component.
$\left. \begin{matrix} i \\ v \\ p \end{matrix} \right\}$	with subscripts	$\left\{ \begin{matrix} E \\ B \\ C \end{matrix} \right\}$	instantaneous total value.
$\left. \begin{matrix} I \\ V \\ P \end{matrix} \right\}$	with subscripts	$\left\{ \begin{matrix} e \\ b \\ c \end{matrix} \right\}$	the r.m.s. value of the varying component, or with appropriate additional subscript the peak (m) or average (d.c.) (av) value of the varying component.
$\left. \begin{matrix} I \\ V \\ P \end{matrix} \right\}$	with subscripts	$\left\{ \begin{matrix} E \\ B \\ C \end{matrix} \right\}$	the no-signal (d.c.) value or, with the appropriate additional subscripts the total average value (AV) with signal or the total peak value (M).



[9613]

Examples:

I_E	d.c. emitter current no signal.
i_e	r.m.s. value of varying component of emitter current.
I_e	Instantaneous value of varying component of emitter current.
i_E	Instantaneous value of total emitter current.
$I_{E(AV)}$	Average (d.c.) value of total emitter current with signal applied.
$i_{e(av)}$	Average (d.c.) value of the varying component of the emitter current.
I_{em}	Peak value of the varying component of the emitter current.
I_{EM}	Peak value of the total emitter current.

Subscripts for quantity symbols

A, a	Anode terminal	I, i	Input
AV, av	Average	J, j	Junction
B, b	Base terminal	K, k	Cathode terminal
BO	Breakover	M, m	Peak value
BR	Breakdown	O, o	Open-circuit, output
C, c	Collector terminal, conversion, capacitive	OV	Average value of overload
D, d	Delay, Off-state (i.e. non trigger) drain terminal	R, r	Resistive, reverse, repetitive
E, e	Emitter terminal	S, s	Short-circuit, series, shield, source
F, f	Forward	T, t	On-state (i.e. triggered)
G, g	Gate terminal	W, w	Working
H, h	Holding	X, x	Specified circuit, reactive
		Z, z	Reference or regulator (i.e. Zener), impedance

The letter O is used with three terminal devices as a third subscript only to denote that the terminal not indicated in the subscript is open-circuited.

The letter S is also used with three terminal devices as a third subscript to denote that the terminal not indicated in the subscript is shorted to the reference terminal.

Sequence of subscripts

The first subscript denotes the terminal at which the current or terminal voltage is measured.

The second subscript denotes the reference terminal or circuit mode that the current or terminal voltage is measured.

Where the reference terminal or circuit is understood the second subscript may be omitted where its use is not required to preserve the meaning of the symbol.

The supply voltage shall be indicated by repeating the terminal subscript. The reference terminal may then be designated by the third subscript.

Examples V_{EE} , V_{CC} , V_{BB} , V_{EEB}

In devices having more than one terminal of the same type, the terminal subscripts shall be modified by adding a number following the subscript and on the same line.

Example B2

In multiple unit devices the terminal subscripts shall be modified by a number preceding the terminal subscript.

Example 2B

Where ambiguity might arise the complete terminal designations shall be separated by hyphens or commas.

Example $V_{1C1-2C1}$

the voltage at the first collector of the first unit referred to the voltage at the first collector of the second unit.

The first subscript in the matrix notation shall identify the element of the four pole matrix.

i input
o output
f forward transfer
r reverse transfer

A second subscript may be used to identify the circuit configuration.

e common emitter
b common base
c common collector

Example $V_{ie} = h_{ie} \cdot I_{ie} + h_{re} \cdot V_{oe}$

When the common terminal is understood the second subscript may be omitted.

Static value of parameters shall be indicated by the upper case (capital) subscripts.

Example h_{IE}, h_{IB}

The four pole matrix parameters of the device are represented by lower case symbols with the appropriate subscripts

h_{ib}

The four pole matrix parameters of external circuits and of circuits in which the device forms only a small part are represented by upper case symbols with the appropriate subscripts.

H_i, Z_o

Symbols for the components of small-signal equivalent circuits used to represent devices are qualified by lower case symbols.

$r_b, r_e, r_{bb'}$

ELECTRICAL PARAMETERS

	Device	Associated circuit
Resistance	r	R
Reactance	x	X
Impedance	z	Z
Admittance	y	Y
Conductance	g	G
Susceptance	b	B
Mutual inductance	m	M
Inductance	l	L
Capacitance	c	C
Distortion	D	
Frequency limits	f max. f min. Δf	
Bandwidth		B
Bandwidth (for associated circuits)		N
Noise factor		

List of Symbols for Semiconductor Devices

C_d	diode capacitance (reverse bias)
C_f	diode capacitance (forward bias)
C_{ib}	transistor input capacitance (grounded base)
C_{ie}	transistor input capacitance (grounded emitter)
C_j	junction capacitance (of the intrinsic diode)
C_{min}	diode capacitance (at breakdown voltage)
C_o	diode capacitance (zero bias)
C_{ob}	transistor output capacitance (grounded base)
C_{oe}	transistor output capacitance (grounded emitter)
C_p	parasitic (parallel) capacitance
C_s	stray capacitance
C_{Te}	capacitance of the emitter depletion layer
C_{Tc}	capacitance of the collector depletion layer
f_{co}	varactor diode cut-off frequency
f_{hfb}	transistor cut-off frequency (the frequency at which the parameter indicated by the subscript is 0.7 times its low frequency value)
f_{hte}	
f_l	frequency of unity current transfer ratio modulus
f_{max}	maximum frequency of oscillations
f_r	tunnel diode resistive cut-off frequency
f_T	transition frequency (common emitter gain-bandwidth product)
g_i	tunnel diode negative conductance (of the intrinsic diode)
g_p	small signal power gain
G_p	large signal power gain
h_{IB}	the static value of the input resistance with the output voltage held constant
h_{IE}	
h_{IC}	
$h_{ib} (h_{11})$	The small-signal value of the input impedance with the output short-circuited to alternating current
$h_{ie} (h_{11})$	
h_{ic}	
h_{RB}	The static value of the reverse voltage transfer ratio with the input current held constant
h_{RE}	
h_{RC}	
$h_{rb} (h_{12})$	The small-signal value of the reverse voltage transfer ratio with the output voltage held constant
$h_{re} (h_{12})$	
h_{rc}	
h_{FB}	The static value of the forward current transfer ratio with the output voltage held constant
h_{FE}	
h_{FC}	
$h_{fb} (h_{21})$	The small-signal forward current transfer ratio with the output short-circuited to alternating current
$h_{fe} (h_{21})$	
h_{fc}	
h_{OB}	The static value of the output conductance with the input current held constant
h_{OE}	
h_{OC}	
$h_{ob} (h_{22})$	The small-signal value of the output admittance with the input open-circuited to alternating current
$h_{oe} (h_{22})$	
h_{oc}	
$h_{FE(sat)}$	transient forward current transfer ratio in saturation
h_{FEL}	inherent forward current transfer ratio = $\frac{I_C - I_{CBO}}{I_B + I_{CBO}}$

I_B, I_C, I_E	total d.c. current
$I_{B(AV)}, I_{C(AV)}, I_{E(AV)}$	average (d.c.) value of total current
I_{BBX}	base current (with both junctions reverse biased)
I_{BEX}, I_{CEX}	base (respectively collector) cut off current in a specified circuit
I_{BM}, I_{CM}, I_{EM}	peak value of total current
i_b, i_c, i_e	r.m.s. value of varying component of current
I_{bm}, I_{cm}, I_{em}	peak value of varying component of current
i_B, i_C, i_E	instantaneous total value of current
i_b, i_c, i_e	instantaneous value of varying component of current
$I_{(BO)}$	thyristor breakover current (d.c.)
I_{CBO}	collector cut-off current (emitter open-circuited)
I_{CBS}, I_{CES}	collector cut-off current (emitter short-circuited to base)
I_{CBX}	collector current with both junctions reverse biased with respect to base
I_{CEO}	collector cut-off current (base open-circuit)
I_{CER}	collector cut-off current (with specified resistance between base and emitter)
I_D	thyristor continuous (d.c.) off-state current, field effect transistor drain current
I_{EBO}	emitter cut-off current (collector open-circuit)
I_{EBX}	emitter current with both junctions reverse biased with respect to base
I_F	D.C. forward current
i_F	instantaneous forward current
$I_{F(AV)}$	average forward current
I_{FG}	thyristor forward gate current
I_{FGM}	thyristor peak forward gate current
I_{FM}	peak forward current
$I_{F(OV)}, I_{FOM}$	overload mean forward current
I_{FRM}	repetitive peak forward current
I_{FSM}	surge (non-repetitive) forward current
I_{GD}	thyristor gate non-trigger current
I_{GT}	thyristor gate trigger current
I_{GQ}	thyristor gate turn-off current
I_H	thyristor holding current (d.c.)
I_L	thyristor latching current
I_O	average output current
I_{ORM}	repetitive peak output current
I_P	tunnel diode peak point current
I_P/I_V	tunnel diode peak to valley point current ratio
I_R	continuous (d.c.) reverse leakage current
i_R	instantaneous reverse leakage current
I_{RG}	thyristor reverse gate current
I_{RRM}	repetitive peak reverse current
I_{RSM}	non-repetitive peak reverse current
I_S	source current
I_T	thyristor continuous (d.c.) on-state current
$I_{T(OV)}$	thyristor overload mean on-state current
$I_{T(AV)}$	thyristor average on-state current
I_{TRM}	thyristor repetitive peak on-state current
I_{TSM}	thyristor non-repetitive peak on-state current

GENERAL EXPLANATORY NOTES

SEMICONDUCTOR DEVICES

I_V	tunnel diode valley point current
I_Z	voltage regulator (zener) diode continuous (d.c.) operating current
$I_{Z(AV)}$	voltage regulator (zener) diode average operating current
I_{ZM}	voltage regulator (zener) diode peak current
L_c	conversion loss
L_s	series inductance
N_f	flicker noise
N_{if}	noise figure at intermediate frequency
N_o	overall noise figure
N_r	noise temperature ratio
P_G	thyristor average gate power
P_{GM}	thyristor peak gate power
P_{tot}	total power dissipated within the device
Q_s	recovered (stored) charge
$r_{bb'}$	extrinsic base resistance
R_S	source resistance
r_s	series resistance
R_{th}	thermal resistance
r_Z	voltage regulator (zener) diode differential resistance
S_{ts}	tangential signal sensitivity
S_Z	voltage regulator (zener) diode temperature coefficient of the operating voltage
T_{amb}	ambient temperature
T_{case}	case temperature
T_j	junction temperature
T_{mb}	mounting base temperature
T_{stg}	storage temperature
t_d	delay time
t_f	fall time
t_{fr}	forward recovery time
t_{gt}	thyristor gate controlled turn-on time
t_{gq}	thyristor gate controlled turn-off time
t_p	pulse duration
t_q	thyristor circuit-commutated turn-off time
t_{on}	turn-on time
t_{off}	turn-off time
t_r	rise time
t_{rr}	reverse recovery time
t_s	storage time
θ_h	thermal resistance of heat sink
θ_i	contact thermal resistance
θ_{j-amb}	thermal resistance junction to ambient
θ_{j-case}	thermal resistance junction to case
θ_{j-mb}	thermal resistance junction to mounting base
τ_C	collector time coefficient of a switching transistor
τ_S	carrier storage time coefficient of a switching transistor
τ_F	fall time factor
τ_R	rise time factor

$V_{BE(sat)}$	base-emitter saturation voltage
$V_{(BO)}$	thyristor breakover voltage
$V_{(BR)}$	breakdown voltage
$V_{(BR)CBO}$	breakdown voltage collector to base (emitter open-circuited)
$V_{(BR)CBS}$	breakdown voltage collector to base (emitter and base short-circuited)
$V_{(BR)CEO}$	breakdown voltage collector to emitter (base open circuited)
$V_{(BR)CER}$	breakdown voltage collector to emitter (with specified resistance between base and emitter)
$V_{(BR)CES}$	breakdown voltage collector to emitter (emitter and base short-circuited)
$V_{(BR)CEX}$	breakdown voltage collector to emitter (with specified circuit between base and emitter)
$V_{(BR)EHO}$	breakdown voltage emitter to base (collector open-circuited)
$V_{(BR)R}$	reverse breakdown voltage
V_{CB}	collector-base voltage (d.c.)
V_{CBO}	collector-base voltage (with emitter open-circuited)
V_{CBfl}	collector-base floating potential
V_{CC}	collector supply voltage (d.c.)
V_{CE}	collector to emitter voltage (d.c.)
V_{CEO}	collector to emitter voltage (with base open-circuited)
V_{ce}	collector to emitter r.m.s. voltage
$V_{CE(knee)}$	collector knee voltage
$V_{CE(sat)}$	collector to emitter saturation voltage
$V_{CE(sust)}$	collector to emitter sustaining voltage
V_D	thyristor continuous (d.c.) off-state voltage
V_{DG}	drain to gate voltage
V_{DM}	thyristor peak off-state voltage
V_{DRM}	thyristor repetitive peak off-state voltage
V_{DS}	drain to source voltage
V_{DSM}	thyristor non-repetitive off-state voltage
V_{DWM}	thyristor crest (peak) working off-state voltage
V_{EB}	emitter-base voltage (d.c.)
V_{EBO}	emitter-base voltage (with collector open circuited)
V_{eb}	emitter-base r.m.s. voltage
V_{EBfl}	emitter-base floating potential
V_{ECfl}	emitter-collector floating potential
V_F	D.C. forward voltage
v_F	instantaneous total value of the forward voltage
V_{FG}	thyristor forward gate voltage
V_{FGM}	thyristor peak forward gate voltage
V_{fr}	signal diode forward recovery voltage
V_{GB}	gate to substrate voltage
V_{GD}	thyristor gate non-trigger voltage
V_{GS}	gate to source voltage
V_{GT}	thyristor gate trigger voltage
V_i	input voltage
V_{IRM}	repetitive peak input voltage
V_{ISM}	non-repetitive peak input voltage
V_{IWM}	crest working input voltage
V_O	output voltage

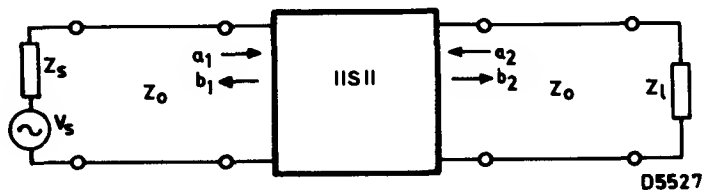
V_P	peak point voltage
V_{PP}	projected peak point voltage
V_R	D.C. reverse voltage
v_R	instantaneous total value of the reverse voltage
V_{RG}	thyristor reverse gate voltage
V_{RGM}	thyristor peak reverse gate voltage
V_{RM}	peak reverse voltage
V_{RRM}	repetitive peak reverse voltage
V_{RSM}	non-repetitive peak reverse voltage
V_{RWM}	crest (peak) working reverse voltage
V_T	thyristor continuous (d.c.) on-state voltage
$V_{T(TO)}$	thyristor threshold voltage
V_V	valley point voltage
V_Z	voltage regulator (zener) diode operating voltage
Z_{if}	intermediate frequency impedance
Z_v	video impedance

y-parameters

Common base	Common emitter		
$y_{ib} (y_{11})$	$y_{ie} (y'_{11})$	Input admittance	} Output short-circuited
$g_{ib} (g_{11})$	$g_{ie} (g'_{11})$	Input conductance	
$c_{ib} (c_{11})$	$c_{ie} (c'_{11})$	Input capacitance	
ϕ_{ib}	ϕ_{ie}	Phase angle of input admittance	
$y_{ob} (y_{22})$	$y_{oe} (y'_{22})$	Output admittance	} Input short-circuited
$g_{ob} (g_{22})$	$g_{oe} (g'_{22})$	Output conductance	
$c_{obs} (c_{22})$	$c_{oes} (c'_{22})$	Output capacitance	
ϕ_{ob}	ϕ_{oe}	Phase angle of output admittance	
$ y_{rb} (y_{21})$	$ y_{re} (y'_{21})$	Transfer admittance	} Output short-circuited
g_{rb}	g_{re}	Transfer conductance	
c_{rb}	c_{re}	Transfer capacitance	
$\phi_{rb} (\phi_{21})$	$\phi_{re} (\phi'_{21})$	Phase angle of transfer admittance	
$ y_{fb} (y_{12})$	$ y_{fe} (y'_{12})$	Feedback admittance	} Input short-circuited
g_{fb}	g_{fe}	Feedback conductance	
c_{fb}	c_{fe}	Feedback capacitance	
$\phi_{fb} (\phi_{12})$	$\phi_{fe} (\phi'_{12})$	Phase angle of feedback admittance	

Scattering parameters

In distinction to the conventional h, y and z parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected travelling wave quantities a_1 , b_1 , a_2 and b_2 , which are square roots of power.



$$a_1^2 = \text{the power incident at the input} \quad \left(= \frac{V_{i1}^2}{Z_o} \right)$$

$$a_2^2 = \text{the power incident at the output} \quad \left(= \frac{V_{i2}^2}{Z_o} \right)$$

$$b_1^2 = \text{the power reflected from (or generated at) the input} \quad \left(= \frac{V_{r1}^2}{Z_o} \right)$$

$$b_2^2 = \text{the power reflected from (or generated at) the output} \quad \left(= \frac{V_{r2}^2}{Z_o} \right)$$

Z_o = the characteristic impedance of the transmission line in which the two-port is connected

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, o for 22, f for 21 and r for 12, it follows that

$$s_i = s_{11} = \left. \frac{b_1}{a_1} \right|_{a_2 = 0}$$

$$s_f = s_{21} = \left. \frac{b_2}{a_1} \right|_{a_2 = 0}$$

$$s_o = s_{22} = \left. \frac{b_2}{a_2} \right|_{a_1 = 0}$$

$$s_r = s_{12} = \left. \frac{b_1}{a_2} \right|_{a_1 = 0}$$

a_1 can be made zero by terminating the input side with $Z_s = Z_o$ (no input power and no reflection from the source).

a_2 can be made zero by terminating the output side with $Z_1 = Z_o$ (no reflection from the load).

Because $\frac{b_1}{a_1} = \frac{V_{r1}}{V_{i1}}$ it can be seen that s_i is the input reflection coefficient; in the same way s_o is the output reflection coefficient.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient (for the given characteristic impedance) – Ratio between the square root of the power reflected from the input and the square root of the power incident at the input, output terminated with the characteristic impedance.

$s_f = s_{21}$ = Forward transmission coefficient (for the given characteristic impedance) – Ratio between the square root of the power generated at the output and the square root of the power incident at the input, output terminated with the characteristic impedance.

$s_o = s_{22}$ = Output reflection coefficient (for the given characteristic impedance) – Ratio between the square root of the power reflected from the output and the square root of the power incident at the output, input terminated with the characteristic impedance.

$s_r = s_{12}$ = Reverse transmission coefficient (for the given characteristic impedance) – Ratio between the square root of the power generated at the input and the square root of the power incident at the output, input terminated with the characteristic impedance.

Section III. Explanation of Handbook Data

1. FORM OF ISSUE

The semiconductor data published in the Handbook follows the same pattern, as much as possible, concerning, (a) the forms of issue, (b) the ratings system and (c) the ratings presentation.

1.1 Types of Data

The Handbook data is published either as tentative or final data.

Tentative Data

Tentative data aims at providing information on new devices as early as possible to allow the customer to proceed with circuit design. The tentative data may not include all the characteristics or ratings which will be incorporated later in the final data and some of the numerical values quoted may be slightly adjusted later on.

Final Data

The transfer from tentative data to final data involves the addition of those numerical values and curves which were not available at tentative data stage and small adjustments to those values already quoted in tentative data. Reissue of final data may be made from time to time to incorporate additional information resulting from prolonged production experience or to meet new applications.

1.2 Presentation of Data

The information on the published data sheets is presented in the following form:

- description of basic application and physical characteristics of the device.
- quick reference data giving the most important ratings and characteristics.
- outline and dimensions. Reference to standard outline nomenclature if applicable and lead connections.
- Ratings. Voltage, current, power and thermal ratings.
- Characteristics.
- Application information or operating conditions.
- Mechanical and environmental data if applicable.
- Charts showing ratings and characteristics.

2. RATINGS

A rating is a limiting condition of usage specified for a device by the manufacturer, beyond which the serviceability may be impaired.

A rating system is a set of principles upon which ratings are established and which determines their interpretation. There are three systems which have been internationally accepted and which allocate responsibility between the device manufacturer and the circuit designer differently.

2.1 Rating Systems

Unless otherwise stated the ratings given in semiconductor data sheets follow the absolute maximum rating system.

The definitions of the three systems accepted by the International Electro-technical Commission are as follows:

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any device of a specified type as defined by the published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for variations in equipment or environment, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other devices in the equipment.

The equipment manufacturer should design so that initially and throughout life no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of the device under consideration and of all other devices in the equipment.

DESIGN-CENTRE RATING SYSTEM

Design-centre ratings are limiting values of operating and environmental conditions applicable to a bogey device of a specified type as defined by its published data, and should not be exceeded under normal conditions. These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of all other devices in the equipment. The equipment manufacturer should design so that initially no design-centre value for the intended service is exceeded with a bogey device in equipment operating at the stated normal supply voltage.

DESIGN-MAXIMUM RATING SYSTEM

Design-maximum ratings are limiting values of operating and environmental conditions applicable to a bogey device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the device under consideration.

The equipment manufacturer should design so that initially and throughout life no design-maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of the device under consideration and of all other devices in the equipment.

3 Transistor ratings

The ratings are presented as voltage, current, power and temperature ratings. The list of these ratings and their definitions is given as follows:

3.1 Transistor voltage ratings

Collector to base voltage ratings

$V_{CB} \text{ max}$ The maximum permissible instantaneous voltage between collector and base terminals. The collector voltage is negative with respect to base in PNP transistors and positive w.r.t. base in NPN types.

$V_{CB} \text{ max } (I_E = 0)$ The maximum permissible instantaneous voltage between collector and base terminals, when the emitter terminal is open circuited.

Emitter to base voltage ratings

$V_{EB} \text{ max}$ The maximum permissible instantaneous reverse voltage between emitter and base terminal. The emitter voltage is negative w.r.t. base for PNP transistor and positive w.r.t. base for NPN types.

$V_{EB} \text{ max } (I_C = 0)$ The maximum permissible instantaneous reverse voltage between emitter and base terminals when the collector terminal is open circuited.

Collector to emitter voltage ratings

$V_{CE} \text{ max}$ The maximum permissible instantaneous voltage between collector and emitter terminals. The collector voltage is negative w.r.t. emitter in PNP transistors and positive w.r.t. emitter in NPN types. This rating is very dependent on circuit conditions and collector current and it is necessary to refer to the curve of V_{CE} versus I_C for the appropriate circuit condition in order to obtain the correct rating

$V_{CE} \text{ max (Cut-off)}$ The maximum permissible instantaneous voltage between collector and emitter terminals when the emitter current is reduced to zero by means of a reverse emitter base voltage, i.e. the base voltage is normally positive w.r.t. emitter for PNP transistor and negative w.r.t. emitter for NPN types.

NOTE: The term "cut-off" is sometimes replaced by $V_{BE} > x$ volts, or $\frac{R_B}{R_E} \leq y$ which are equivalent conditions under which the device may be cut-off.

$V_{CE \text{ max }} (I_C = x \text{ mA})$ The maximum permissible instantaneous voltage between collector and emitter terminals when the collector current is at a high value, often the max. rated value.

$V_{CE \text{ max }} (I_B = 0)$ The maximum permissible instantaneous voltage between collector and emitter terminals when the base terminal is open circuited or when a very high resistance is in series with the base terminal. Special care must be taken to ensure that thermal runaway due to excessive collector leakage current does not occur in this condition.

Due to the current dependency of V_{CE} it is usual to present this information as a voltage rating chart which is a curve of collector current versus collector to emitter voltage (see Fig. 1).

This curve is divided into two areas:

A permissible area of operation under all conditions of base drive provided the dissipation rating is not exceeded (area 1) and an area where operation is allowable under certain specified conditions (area 2).

To assist in determining the rating in this second area, further curves are provided relating the voltage rating to external circuit conditions, for example:

$$\frac{R_B}{R_E}, R_B, Z_{B\theta}, V_{BE}, I_B \text{ or } \frac{V_{BB}}{R_B}$$

An example of this type of curve is given in Fig. 2 as V_{CE} versus $\frac{R_B}{R_E}$ for two different values of collector current.

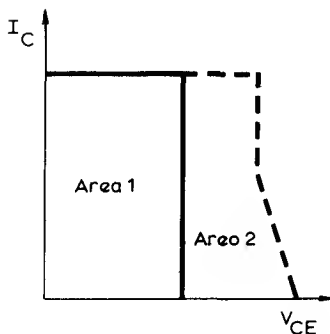


Fig 1

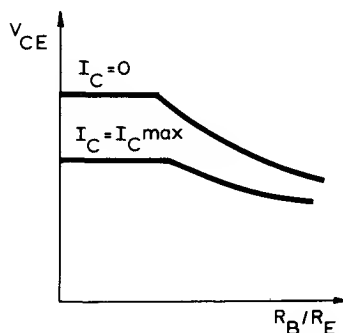


Fig 2

It should be noted that when R_E is shunted by a capacitor, the collector voltage V_{CE} during switching must be restricted to a value which does not rely on the effect of R_E .

In the case of an inductive load and when an energy rating is given, it may be permissible to operate outside the rated area provided the specified energy rating is not exceeded.

3.2 Transistor Current Ratings

Collector current ratings

$I_C \text{ max}$	The maximum permissible collector current. Without further qualification, the dc value is implied.
$I_{C(AV)} \text{ max}$	The maximum permissible average value of the total collector current.
I_{CM}	The maximum permissible instantaneous value of the total collector current.

Emitter current ratings

$I_E \text{ max}$	The maximum permissible emitter current. Without further qualification, the dc value is implied.
$I_{E(AV)} \text{ max}$	The maximum permissible average value of the total emitter current.
$I_{ER(AV)} \text{ max}$	The maximum permissible average value of the total emitter current when operating in the reverse emitter-base breakdown region.
I_{EM}	The maximum permissible instantaneous value of the total emitter current.
I_{ERM}	The maximum permissible instantaneous value of the total reverse emitter current allowable in the reverse breakdown region.

Base current ratings

$I_B \text{ max}$	The maximum permissible base current (without further qualification, the dc value is implied).
$I_{B(AV)} \text{ max}$	The maximum permissible average value of the total base current.
$I_{BR(AV)} \text{ max}$	The maximum permissible average value of the total reverse base current allowable in the reverse breakdown region.
I_{BM}	The maximum permissible instantaneous value of the total base current. The rating also includes the switch off current.
I_{BRM}	The maximum permissible instantaneous value of the total reverse current allowable in the reverse breakdown region.

3.3 Transistor Power Ratings

$P_{tot \text{ max}}$: The total maximum permissible continuous power dissipation in the transistor and includes both the collector-base dissipation and the emitter-base dissipation. Under steady state conditions the total power is given by the expression:

$$P_{tot} = V_{CE} \times I_C + V_{BE} \times I_b$$

In order to distinguish between "steady state" and "pulse" conditions the terms "steady state power (P_S)" and "pulse power (P_P)" are often used. The permissible total power dissipation is dependent upon temperature and its relationship is shown by means of a chart as shown in figure 3.

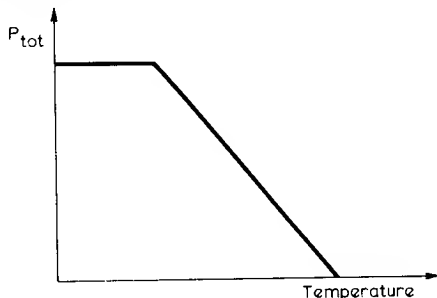


Fig 3

The temperature may be ambient, case or mounting base temperatures. Where a cooling clip or a heatsink is attached to the device, the allowable power dissipation is also dependent on the efficiency of the heatsink.

The efficiency of this clip or heatsink is measured in terms of its thermal resistance (θ_h) normally expressed in degrees centigrade per watt (deg. C/W). For mounting base rated device, the added effect of the contact resistance (θ_i) must be taken into account.

The effect of heatsinks of various thermal resistance and contact resistance is often included in the above chart.

Thus for any heatsink of known thermal resistance and any given ambient temperature, the maximum permissible power dissipation can be established. Alternatively, knowing the power dissipation which will occur and the ambient temperature, the necessary heatsink thermal resistance can be calculated.

A general expression from which the total permissible steady state power dissipation can be calculated is:

$$P_{tot} = \frac{T_j - T_{amb}}{\theta_{j-amb}}$$

where θ_{j-amb} is the thermal resistance from the transistor junction to the ambient. For case rated or mounting base rated devices, the thermal resistance θ_{j-amb} is made up of the thermal resistance junction to case or mounting base (θ_{mb}), the contact thermal resistance (θ_i) and the heatsink thermal resistance (θ_h).

For the calculation of pulse power operation P_p , the maximum pulse power is obtained by the aid of a chart as shown in figure 4.

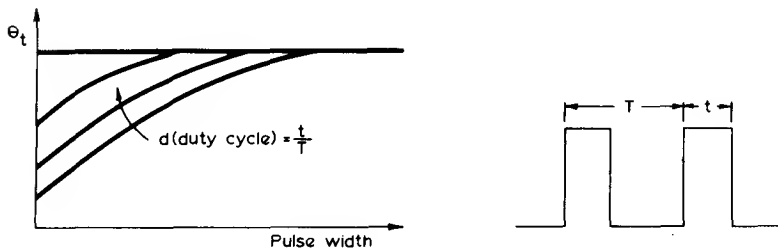


Fig.4

the general expression from which the maximum pulse power dissipation can be calculated is:

$$P_p = \frac{T_j - T_{amb} - P_s \times \theta_{j-amb}}{\theta_t + d(\theta_{case-amb})}$$

where θ_t and d are given in the above chart and $\theta_{case-amb}$ is the thermal resistance between case and ambient for case rated device. For mounting base rated device, it is equal to $\theta_h + \theta_t$ and is zero for free air rated device because the effect of the temperature rise of the case over the ambient for a pulse train is already included in θ_t .

3.4 Temperature Ratings

$T_j \text{ max}$	The maximum permissible junction temperature which is used as the basis for the calculation of power ratings. Unless otherwise stated, the continuous value is implied.
$T_j \text{ max (continuous operation)}$	The maximum permissible continuous value.
$T_j \text{ max (intermittent operation)}$	The maximum permissible instantaneous junction temperature usually allowed for a total duration of 200 hours.
T_{mb}	The temperature of the surface making contact with a heatsink. This is confined to devices where a flange or stud for fixing onto a heatsink forms an integral part of the envelope.
T_{case}	The temperature of the envelope. This is confined to devices to which may be attached a clip-on cooling fin.

Section IV. Mounting and Soldering Recommendations

1. MOUNTING OF "LOCKFIT" TRANSISTORS

1.1 Mounting on printed-wiring boards

The "Lockfit" encapsulation is usable with printed-wiring boards having either the standard e-grid or the more closely spaced ϵ -grid. The relevant dimensions of these boards are given in Table 1.

TABLE 1
Dimensions of Printed-wiring Boards

Board	Grid	Hole diameter	Maximum board thickness
e-board	2.54mm (0.1in)	1.05 ± 0.05 mm (up to 1.30mm allowable)	1.7mm
ϵ -board	0.635mm (0.025in)	0.80 ± 0.03 mm	1.1mm

The pins of "Lockfit" transistors each have three enlargements along their length, as shown in Fig. 1. At the tip is a spade-shaped (lock 'B'); partway up is a tapered cross-piece (lock 'A') that projects further left and right than lock 'B'; and nearest to the body of the assembly is another cross-piece (lock 'C') that extends even further left and right than lock 'A'.

Hole spacing in either type of grid allows the insertion of the "Lockfit" pins; but as the holes of the closely spaced ϵ -grid are necessarily of smaller diameter than those of the other grid, the pins cannot be (or should not be) pushed in beyond the middle expansion – lock 'A'. Thus the functions of the three locks are as indicated in Fig. 1a for e-grid boards and Fig. 1b for ϵ -grid boards.

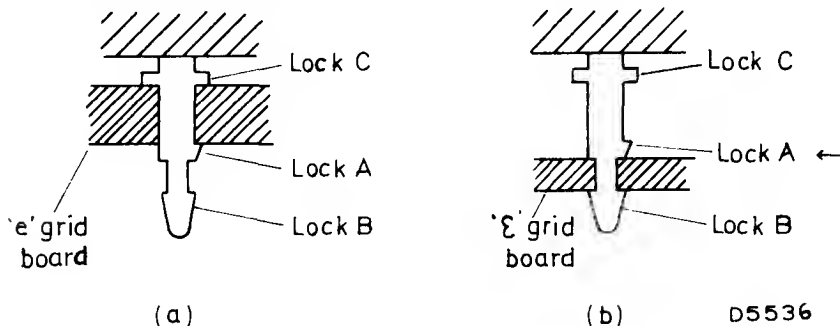


Fig. 1 – Detail of "Lockfit" pins, and function of three "locks" when used with
(a) e-grid and (b) ϵ -grid printed-wiring boards

1.1.1 Mounting procedure with e-grid boards

The best insertion procedure with the e-(2.54mm) grid is as follows:
 (1) Place the rear two pins into their corresponding printed-circuit board holes with the transistor at a slight angle to the vertical (Fig. 2a).
 (2) Place the centre pin into the remaining hole by light pressure at a slight angle to the vertical on the device. Continue this light pressure until both the 'A' locks of the rear two leads are inside the holes (Fig. 2b).
 (3) Tilt the device with light pressure from the rear until it is in a vertical position. Lock 'A' of the centre lead will now enter the hole (Fig. 2c).
 (4) Move the device perpendicularly downwards with light pressure until all three 'A' locks snap into position beneath the printed-wiring board, and the 'C' locks rest on the upper side of the board (Fig. 2d).

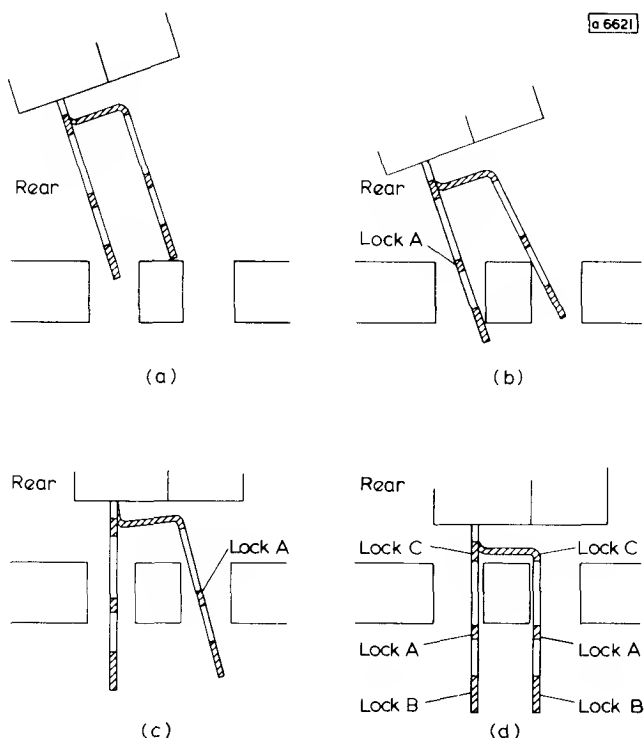


Fig. 2 - Mounting procedure for "Lockfit" transistors using e-grid printed-wiring boards; procedure is similar for e-grid boards

1.1.2 Mounting procedure with ε -grid boards

The best insertion procedure with the ε -(0.635mm) grid is as follows:

(1) Place the rear two pins into their corresponding printed-circuit board holes with the transistor at a slight angle to the vertical.

(2) Place the centre pin into the remaining hole by light pressure at a slight angle to the vertical on the device. Continue this light pressure until both the 'B' locks of the rear two leads are inside the holes.

(3) Tilt the device with light pressure from the rear until it is in a vertical position. Lock 'B' of the centre lead will now enter the hole.

(4) Move the device perpendicularly downwards with light pressure until all three 'B' locks snap into position beneath the printed-wiring board, and the 'A' locks rest on the upper side of the board.

No attempt should be made to force lock 'A' through this type of board.

1.2 Soldering

For both boards, the temperature should not exceed 300°C and the application time should not exceed 3 seconds.

INTRODUCTION TO TECHNICAL DATA

1. LEAD DESIGNATIONS

Source S, s. Drain D, d. Gate G, g. Substrate B, b.

2. SEQUENCE OF SUBSCRIPTS

The first subscript denotes the terminal at which the current or voltage is measured.

Where the reference terminal or circuit is understood, the second subscript may be omitted where its use is not required to preserve the meaning of the symbol.

The letter O is used with three terminal devices as a third subscript only to denote that the terminal not indicated in the subscript is open circuited. The letter S is used as a third subscript to denote that the terminal not indicated in the subscript is short circuited to the reference terminal. The letter X is used as a third subscript to denote measurements taken under specified circuit conditions.

2.1 Quantity Symbols

	V	—	Voltage
	I	—	Current
	P	—	Power
i	d		
v with subscripts	s		instantaneous value of varying component
p	g		
i	D		
v with subscripts	S		instantaneous total value
p	G		
I	d		the r.m.s. value of the varying component or
V with subscripts	s		with appropriate subscript the peak (m) average
P	g		(d.c.) (av) value of the varying component
I	D		the no-signal (d.c.) value of or with the
V with subscripts	S		appropriate additional subscripts the total
P	G		average value (AV) with signal or the total peak value (M)

The letter symbol usually indicates by two subscripts the two reference terminals. The first subscript indicates the terminal which is positive with respect to the second subscript.

e.g.

$V_{DS} = 6V$: Drain is 6V positive w.r.t. Source

$V_{DS} = -6V$: Drain is 6V negative w.r.t. Source

Reversal of the subscripts also changes the polarity sign
For example the following statements are identical

$$V_{DS} = -6V; V_{SD} = 6V; -V_{DS} = 6V$$

The supply voltage shall be indicated by repeating the terminal subscript.
The reference terminal may then be designated by the third subscript.

Examples

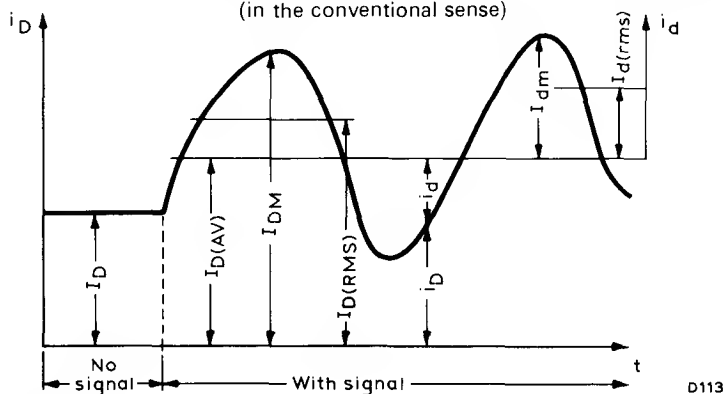
$$V_{DD}, V_{SS}, V_{SSD}$$

2.3 Current

Conventionally, current which flows into the transistor terminals has a positive value.

e.g. $I_D = 1\text{mA}$ means 1mA flowing into the drain terminal
(in the conventional sense)

$I_S = -1\text{mA}$ means 1mA flowing out of the source terminal
(in the conventional sense)



Examples

- I_D d.c. drain current—no signal
- $I_{D(AV)}$ Average (d.c.) value of total drain current with signal applied
- I_{DM} Peak value of total drain current
- $I_{D(RMS)}$ Root-mean-square value of total drain current
- i_D Instantaneous value of total drain current
- i_{dm} Peak value of the varying component of the drain current
- $i_{d(rms)}$ Root-mean-square value of varying component of drain current
- i_d Instantaneous value of varying component of the drain current

The following are examples of the implied relationship

$$I_{DM} = I_{D(AV)} + i_{dm}; i_D = I_{D(AV)} + i_d; I_{D(RMS)} = \sqrt{I_{D(AV)}^2 + i_{d(rms)}^2}$$

To avoid any misunderstanding with maximum or minimum values the negative sign is always put in front of the letter symbol and not in front of the value given.

For example in quoting a limit value

$$-I_S \text{ max} = 50\text{mA}$$

and in quoting a spread value

$$-V_{P(GS)} \leq 1.5\text{V}$$

In devices having more than one terminal of the same type the terminal subscripts shall be modified by adding one number following the subscript and on the same line.

Examples:

V_{G1S}, V_{G2S} , refers to a dual gate MOS device

$|V_{G1S1} - V_{G2S2}|$ refers to a matched pair of junction FET's

where the gate-source voltage of the first device is referred to the gate-source voltage of the second device, as a modulus of their difference over a given temperature range.

- 2.4** The first subscript in the matrix notation identifies the element of the four pole matrix.

i — input
o — output
f — forward transfer
r — reverse transfer.

A second subscript may be used to identify the circuit configuration.

d — common drain
s — common source
g — common gate

Examples

$C_{is} \ C_{os} \ C_{rs}$

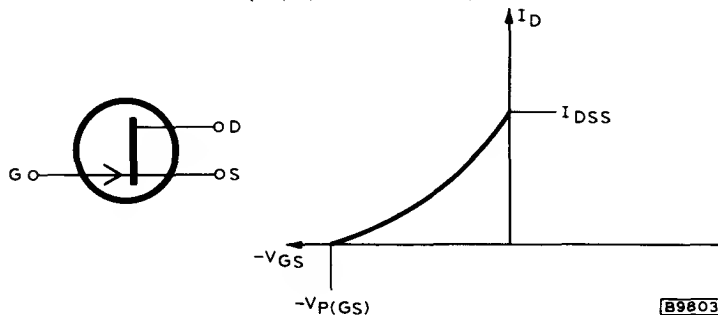
Input, output and reverse feedback capacitances in common source configuration.

3. TYPES OF FIELD EFFECT TRANSISTORS

3.1 Junction gate Field effect transistors

N-channel-junction FET

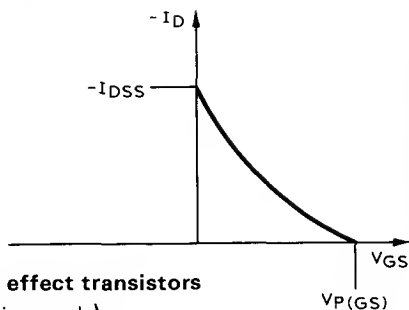
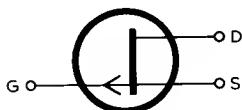
$$(V_{P(GS)} < 0, I_{DSS} > 0)$$



B9803

P-channel-junction FET

$$(V_{P(GS)} > 0, I_{DSS} < 0)$$

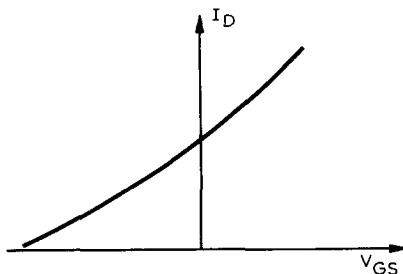
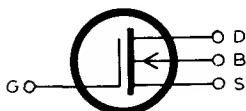


3.2 Insulated gate M.O.S. field effect transistors

N-channel-M.O.S.-FET (depletion mode)

$$(V_{P(GS)} < 0, I_{DSS} > 0)$$

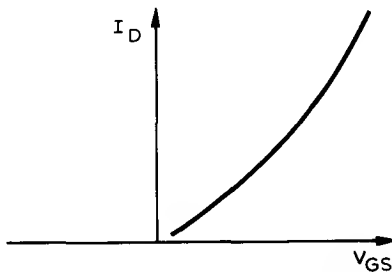
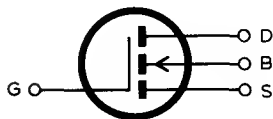
B9804



N-channel-M.O.S.-FET (enhancement mode)

B9805

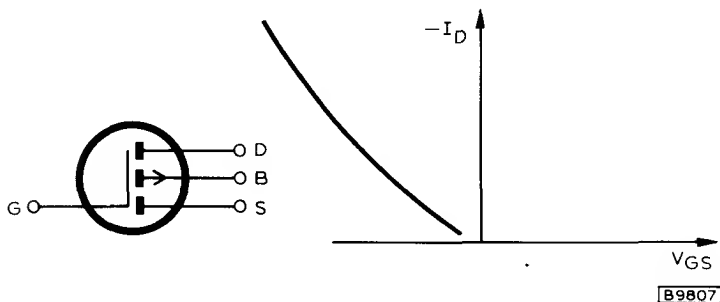
$$(V_{P(GS)} \geq 0, I_{DSS} \approx 0)$$



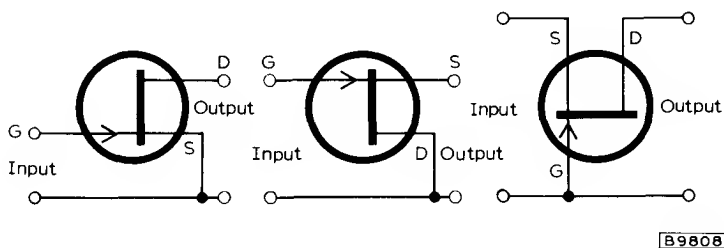
B9806

P-channel-M.O.S.FET (enhancement mode)

$$(V_{P(GS)} \leq 0, I_{DSS} \approx 0)$$



4. BASIC CIRCUITS CONFIGURATIONS



Grounded-source
The source is common to input and output

Grounded-drain
The drain is common to input and output

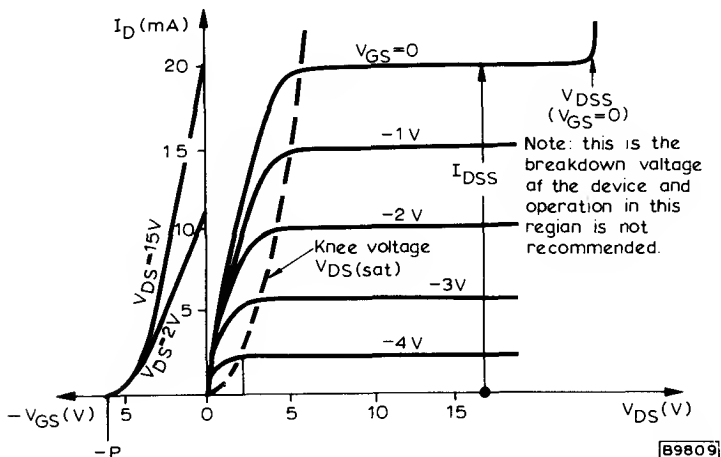
Grounded-gate
The gate is common to input and output

An additional subscript s, d or g may be used to identify the circuit configuration

Example C_{is} is input capacitance with grounded source

5. CHARACTERISTICS

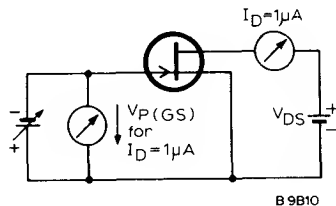
The characteristics are given in data sheets as either typical values and/or minimum and maximum values. Published curves are usually typical curves and are applicable only at the stated temperature.



5.1 Cut-off Voltage ($V_{P(GS)}$)

The cut-off voltage $V_{P(GS)}$ is the gate-source voltage for a given small value of drain current I_D at a stated drain source voltage V_{DS} .

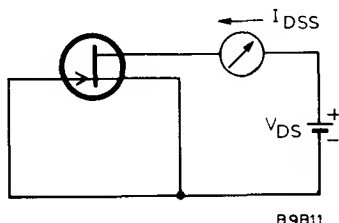
TEST CIRCUIT FOR $V_{P(GS)}$



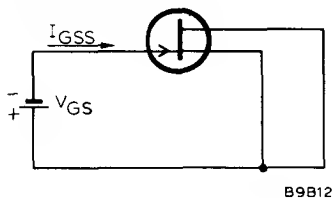
5.2 Drain-source short circuit current (I_{DSS})

The drain-source short circuit current I_{DSS} is the current flowing between drain and source with the gate short-circuited to the source ($V_{GS} = 0$) and at a stated drain-source voltage (V_{DS}).

TEST CIRCUIT FOR I_{DSS}

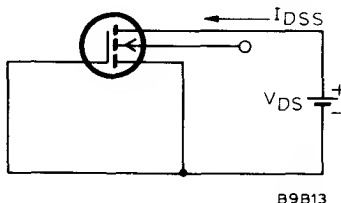


5.3 Leakage currents



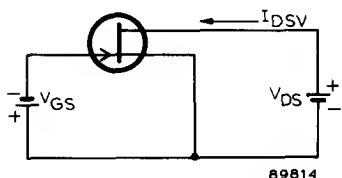
B9B12

Gate-source leakage/current
 I_{GSS}



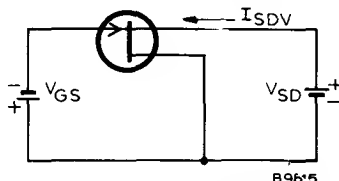
B9B13

Drain-source leakage current
 I_{DSS}
(enhancement mode device)



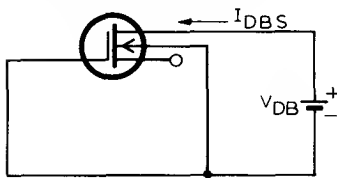
B9B14

Drain-source leakage current
 I_{DSV} , at specified V_{DS} and V_{GS}
and grounded source



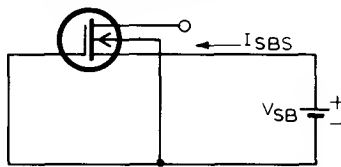
B9B15

Source-drain leakage current
 I_{SDV} with specified V_{SD} and V_{GS}
with grounded drain



B9B16

Drain-substrate leakage current
 I_{DBS}

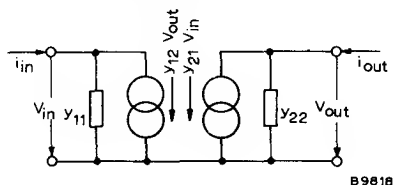


B9B17

Source-substrate leakage current
 I_{SBS}

6. SMALL SIGNAL-Y PARAMETERS

Four-pole equivalent circuit



B9B18

$$\begin{aligned}
 y_{11} = y_i &= \frac{i_{in}}{V_{in}} \quad V_{out} = 0 && \text{input admittance with output short circuited} \\
 y_{12} = y_r &= \frac{i_{in}}{V_{out}} \quad V_{in} = 0 && \text{reverse transfer admittance with input short circuited} \\
 y_{21} = y_f &= \frac{i_{out}}{V_{in}} \quad V_{out} = 0 && \text{forward transfer admittance with output short circuited} \\
 y_{22} = y_o &= \frac{i_{out}}{V_{out}} \quad V_{in} = 0 && \text{Output admittance with input short circuited}
 \end{aligned}$$

A second subscript on the y -parameter indicates the circuit configuration

e.g. y_{is} = input admittance in common source configuration

where y_{is} is the complex form

$$y_{is} = g_{is} + jb_{is} \quad \text{and} \quad b_{is} = \omega C_{is}$$

For example

C_{is} = input capacitance in common source

and

C_{rs} = feedback capacitance in common source

The forward transfer admittance in common source configuration at low frequency (e.g. below about 1MHz) is indicated in the following forms

$$gm = g_{21s} = g_{fs} = |y_{fs}|$$

at high frequency this parameter is a complex quantity and the modulus $|y_{fs}|$ is usually given in the data with a specified frequency of measurement.

ABSOLUTE MAXIMUM RATING SYSTEM

7. Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any device of a specified type as defined by the published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for variation in equipment or environment, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other devices in the equipment.

The equipment manufacturer should design so that initially and throughout life no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of the device under consideration and of all other devices in the equipment.

7.1 Ratings (maximum permissible values)

V_{DS} max	—	Drain-source voltage
V_{DB} max	—	Drain-substrate voltage
V_{SB} max	—	Source-substrate voltage
V_{GD} max	—	Gate-drain voltage
V_{GS} max	—	Gate-source voltage
V_{GB} max	—	Gate-substrate voltage
I_D max	—	Drain current
I_S max	—	Source current
I_G max	—	Gate Current

*applies only to junction F.E.T.'s if a forward-voltage is applied to the gate.

7.2 Power Dissipation

- where T_J max = maximum permitted junction temperature
 T_{amb} max = maximum permitted ambient temperature
 T_{case} max = maximum permitted case temperature
 $R_{th(j-amb)}$ = Thermal resistance junction to ambient
 $R_{th(case-amb)}$ = Thermal resistance case to ambient.

The limiting value of the maximum permitted device dissipation P_{tot} max is stated for either

$$T_{amb} = \frac{T_J \text{ max} - T_{amb} \text{ max}}{R_{th(j-amb)}}$$

$$\text{and } P_{tot} \text{ max} = \frac{T_J \text{ max} - T_{case} \text{ max}}{R_{th(case-amb)}}$$

8. SOLDERING AND WIRING RECOMMENDATIONS

- 8.1 When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should, if possible, be kept to a minimum by the use of a thermal shunt.
- 8.2 Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of five seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
- 8.3 Care should be taken not to bend the leads nearer than 1.5mm from the seal.
- 8.4 If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances, the leads should be retinned using a suitable activated flux.

9. OPERATING NOTE (M.O.S. insulated gate F.E.T.'s)

Mounting and handling instructions

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conductive rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.



SECTION VI

Safe Operating ARea for power transistors

INTRODUCTION

One of the main restrictions in the operation of power transistors is the phenomenon known as 'second breakdown'. This is the name given to a transistor condition whereby the collector-emitter voltage abruptly switches from a high to a low voltage with increased current.

A diagram illustrating the output characteristics of a power transistor is shown in Fig. 1. It is not representative of any particular device but merely serves to demonstrate the I_C against V_{CE} characteristics of a transistor as it goes into second breakdown. On the horizontal axis the forward and reverse-biased base regions are clearly grouped, with the base open-circuit condition dividing the two regions.

The transistor will enter second breakdown at a certain critical current value

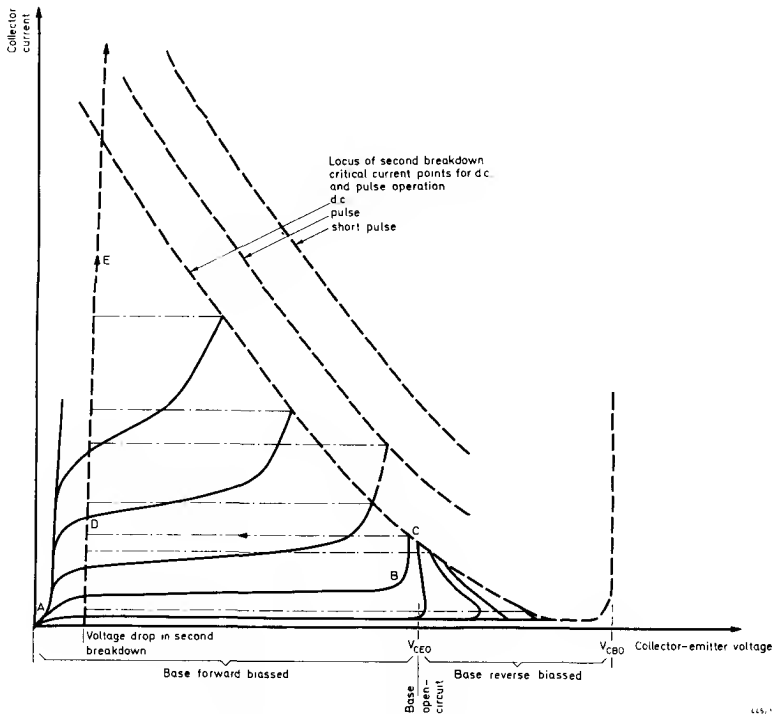


Fig. 1—Output characteristics of a power transistor

which is low at high collector-emitter voltages and higher at low voltages. Three loci for critical current values are shown on the diagram; these represent d.c., pulse, and short pulse operation. The extension of the second-breakdown locus for pulse operation is dependent on the pulse duration t_p and also, to a lesser extent, on the duty cycle d (see Figs. 2 and 3). Thus the greatest extension is permissible with single-shot pulses ($d \approx 0.01$) of short duration, say $10\mu s$. (The value $d = 0.01$ can be considered as single-shot because there is ample time for cooling between power pulses).

Observation of second breakdown

Consider the I_C against V_{CE} characteristic ABCDE shown in Fig. 1. At point B the device goes into avalanche, otherwise known as first breakdown. At this point the collector current starts to rise sharply for very little increase in the collector-emitter voltage. If the current is allowed to increase up to a critical value at C the device will enter second breakdown. This is noted by an abrupt switching of the collector-emitter voltage to a low value at point D. In second breakdown the device offers only a very low resistance to collector current, and is invariably destroyed if the current is not specially limited by a circuit external to the transistor. Beyond point C the process is generally irreversible whereas up to point C in avalanche the trace can be returned with no serious alteration to the transistor properties. It is in the forward-biased mode of operation that the phenomenon of second breakdown has been extensively studied over recent years, and a method of presenting the Safe Operating Area (abbreviated to SOAR) is now being published in Mullard data for power transistors.

In many applications, however, the reverse-bias breakdown characteristics are also of importance. For example, when a power transistor with an inductive load is turned off by reverse biasing the base, the collector voltage will rise above the supply voltage because of the stored inductive energy of the coil. For such applications transistors have been developed which permit excursions outside the V_{CEOMax} rating under specified conditions.

With reverse bias on the base, second breakdown is always preceded by first-breakdown. At low collector currents the voltage across the transistor can exceed the V_{CEO} rating as shown in Fig. 1. In first breakdown, or avalanche, the device goes through a negative resistance region until a critical current value is reached at which point the collector-emitter voltage abruptly switches to a very low value in second breakdown.

Second breakdown in the transistor is usually caused by current concentration at a point in the emitter active area; this is described in detail elsewhere⁽¹⁾

SIMPLE METHOD OF USING PUBLISHED SOAR CURVES

In addition to the methods described in the MTC article ⁽¹⁾ sufficient SOAR information is provided in the published data of each power transistor to cover 90% of all applications.

⁽¹⁾TP 1454 reprinted from MTC No. 122 APRIL 1974

Thus, in most cases the user will merely select the appropriate SOAR curve already constructed—without having to calculate and manipulate M_{SB} values.

In general, the data provides SOAR curves for pulse durations in multiples of 1, 2, 5, and 10, starting at pulse durations in the region 10 to 50 μ s. The families of curves are plotted at duty cycles of 0.01 (single-shot) 0.1, 0.2, 0.5, and 1.0 (d.c.). The transient thermal impedance curves are also included so that the operating mounting-base temperature can be calculated. Typical SOAR data curves for duty cycles of 0.2, 0.5 are illustrated in Figs. 4 and 5.

These curves will be used in the examples that follow.

In the few applications (about 10%) which are not covered by the published SOAR curves, the user can derive M_{SB} curves from the single-shot and d.c. SOAR information, and construct the boundaries using the method fully described in the reference TP 1454

All Mullard data, including pulsed power ratings, assume the use of square waves and resistive loads. Therefore, the system for using the SOAR and transient thermal impedance curves to be described deals with this type of waveform first, and then methods for other practical cases will be considered. It is assumed that the electrical and time conditions are the fixed parameters of an application at the design stage, and that the thermal conditions can be most easily adjusted. The maximum

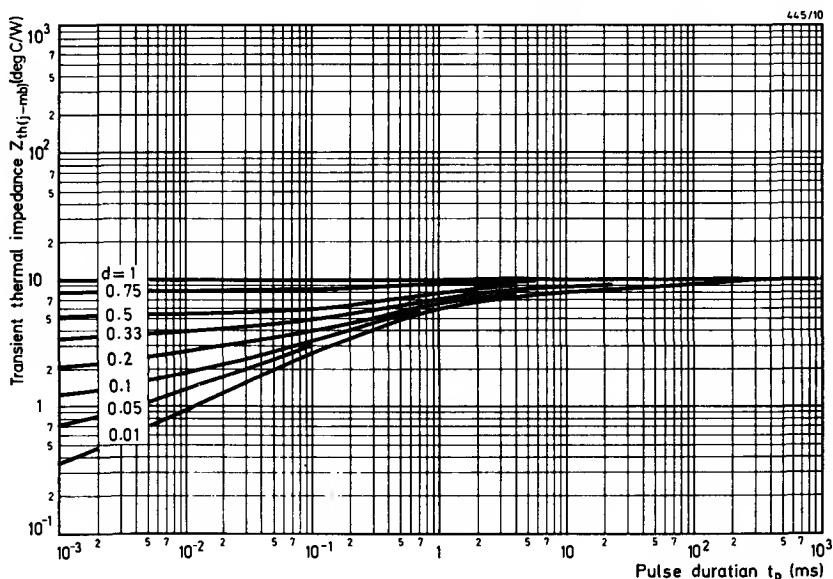


Fig. 2—Typical thermal impedance curves at various duty cycles

power must be calculated at the worst-case condition; when the worst-case condition is not obvious, all discrete sets of conditions need to be assessed.

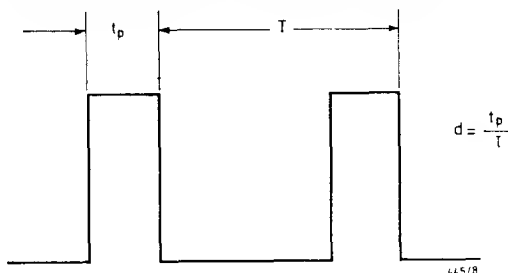


Fig. 3—Relationship between duty cycle (d), pulse duration (t_p) and period (T)

Construction of SOAR using published data

The procedure for constructing a SOAR for one specific set of conditions is described with reference to the curves shown in Figs. 4 and 5, and to the transient thermal impedance curves in Fig. 2.

- 1) Note the pulse duration t_p (for example, 1.7ms).
- 2) Note the time between pulses ($T - t_p$) (for example, 2.9ms).
- 3) Calculate the duty cycle d from the equation $d = t_p/T$ (in this example 0.37).
- 4) Note the peak collector current I_{CM} (for example 300mA).
- 5) Note the peak collector emitter voltage V_{CEM} (for example, 35V).
- 6) Select the SOAR curve with time conditions greater than or equal to the time conditions of the application (in this example, for $d = 0.37$ use $d = 0.5$ and for $t_p = 1.7\text{ms}$ use $t_p = 2.0\text{ms}$).
- 7) Plot the point given by the specific I_{CM} and V_{CEM} values, shown as point Q in Fig. 5.
- 8) The point Q is acceptable if it is contained within the area of the 2ms/0.5 SOAR as shown in this example.

Thermal calculations

The maximum permissible mounting base temperature is now determined as follows:—

- 1) Determine peak power by multiplying I_{CM} by V_{CEM} .
- 2) Calculate the transient thermal impedance for 1.7ms at 0.37 duty cycle.

The equation used is:

$$Z_{th(td)} = \{R_{th} - Z_{th(to)}\}d + Z_{th(to)},$$

Where $Z_{th(td)}$ is the thermal impedance for pulse duration t at duty cycle d , and $Z_{th(to)}$ is the thermal impedance for pulse duration t at duty cycle $d = 0.01$ (from Fig. 2).

- 3) Calculate the difference between the junction and mounting-base temperature from:

$$(T_j - T_{mb}) = Z_{th(td)} \times I_{CM} \times V_{CEM}$$

- 4) Calculate the maximum permissible mounting-base temperature T_{mbmax} from:

$$T_{mbmax} = T_{jmax} - (T_j - T_{mb})$$

- 5) A heatsink which limits the mounting-base temperature to this value is required. The thermal capacity of the heatsink will be such that the transient effect of the power will be averaged. Hence the thermal resistance is calculated using average power. Thus:

$$R_{th(h-a)} = \frac{T_{mbmax} - T_{amb}}{I_{CM} \times V_{CEM} \times d} - R_{th(mb-h)} \text{ degC/W,}$$

Where $R_{th(h-a)}$ is the thermal resistance of heatsink to ambient and $R_{th(mb-h)}$ is the contact thermal resistance.

- 6) The physical size of the required heatsink can be determined from heatsink published data or from the nomogram in Appendix 1.

Operating selected outside SOAR

Suppose the application had required an I_{CM} of 400mA instead of 300mA. In this case the point P on Fig. 4 would be given. Point P is outside the 2ms area which indicates that the condition may be unacceptable. Thus a closer approximation to the true conditions is necessary.

- 1) Using linear interpolation between the 1 and 2ms curves at $d = 0.5$ (Fig. 5) draw a SOAR curve for $t_p = 1.7$ ms. If point P is within this area then the conditions are acceptable and the heatsink thermal resistance can be calculated.
- 2) If point P is outside the 1.7ms area, then determine the 1.7ms area on the family of curves for $d = 0.2$ (Fig. 4). A further linear interpolation between the two 1.7ms areas is then needed to approximate to the 1.7ms SOAR at duty cycle of 0.37.
- 3) If point P is outside this area, then the condition is unacceptable, and a different transistor should be considered.

The above method is not absolutely accurate, but the approximation errors involved are allowed for in the published data tolerances. More accurate calculations can be made by going back to first principles, and calculating the multiplying factor for the specific condition. ⁽¹⁾

⁽¹⁾TP 1454 reprinted from MTC No. 122 APRIL 1974

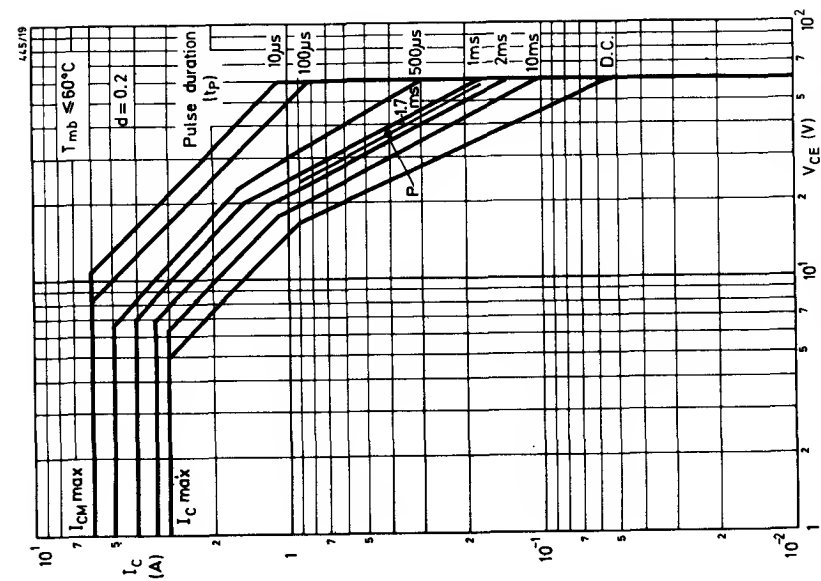


Fig. 4 —Typical SOAR family for $d = 0.2$ (20% duty cycle)

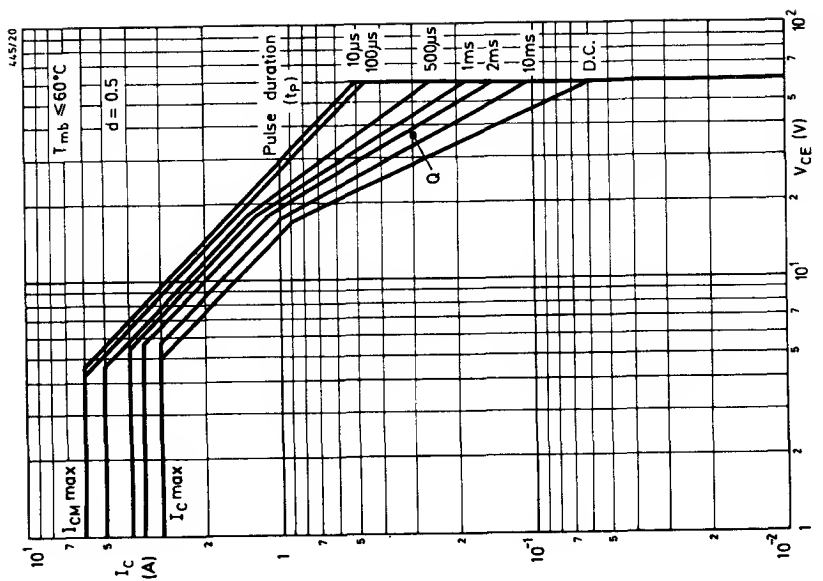


Fig. 5 —Typical SOAR family for $d = 0.5$ (50% duty cycle)

PRACTICAL APPLICATION

This section discusses a typical application in which power transistors are used.

Audio application

The example describes how the output transistors of an audio amplifier are checked for excursions outside the specified SOAR when the amplifier is being tested under a sinewave overdrive condition.

This example describes how the SOAR curves are used to check the suitability of the BD131 power transistors in a television audio amplifier application. The amplifier is a class A design capable of delivering an output of 2W. The circuit configuration is shown in Fig. 6.

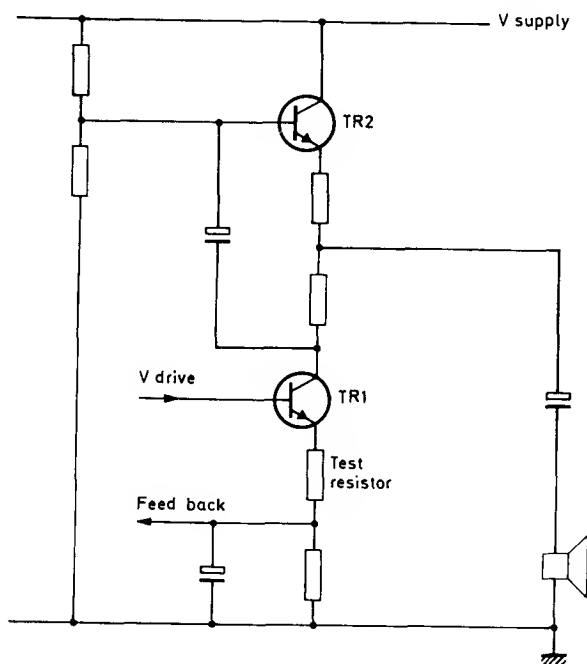


Fig. 6—Circuit configuration of television audio output stage

The amplifier provides the required output power but the second breakdown acceptability has to be checked, and the thermal requirements of the heatsinks are to be calculated.

In this example the SOAR acceptability is considered in the event of the transistors being overdriven by a sinewave signal of period $960\mu\text{s}$. A test resistor of 0.1Ω is

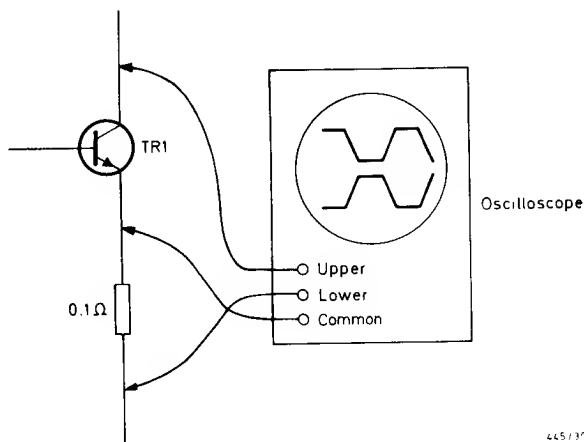


Fig. 7—Method of connecting dual-trace oscilloscope to obtain simultaneous display of I_C and V_{CE}

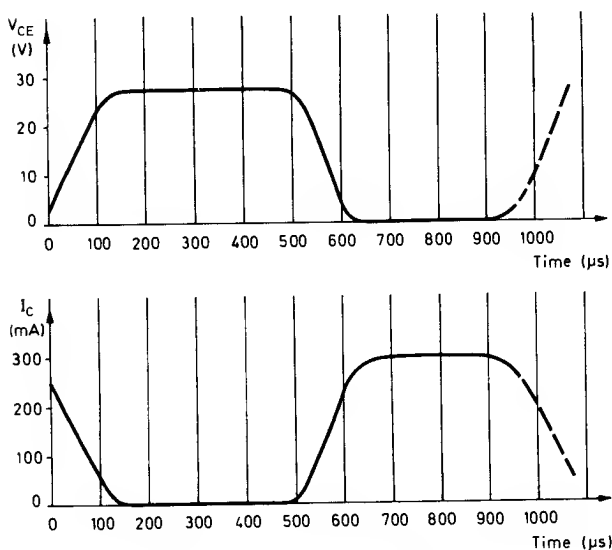


Fig. 8— V_{CE} and I_C characteristics

inserted in the emitter circuit of the lower transistor TR₁. A simultaneous display of the V_{CE} and I_C waveforms is then obtained by connecting the probes of a dual-trace oscilloscope in the manner shown in Fig. 7. The traces of V_{CE} and I_C taken from the oscilloscope are shown in Fig. 8 and the measurements from the waveforms are recorded in Table 1. These readings were recorded every 20 μs through the complete cycle of 960 μs. In the final column of Table 1, values of instantaneous power are calculated and plotted against time in Fig. 9. This curve is then converted into a series of equivalent squarewave pulses having the same peak power values as the actual pulses. The equivalent squarewave pulses are shown by the dashed line and are marked P₁, P₂, and P₃ in Fig. 9.

Each pulse is then checked individually. The duty cycle for each equivalent squarewave pulse is calculated, and the V_{CE} and I_C values recorded over the duration of the pulse are checked on the appropriate SOAR curve.

TABLE 1

Measured values of I_C and V_{CE} and derived P_(tot) obtained
from oscilloscope display

Time (μs)	I _C (mA)	V _{CE} (V)	P _(tot) (W)
0	260	2	0.52
20	220	6	1.32
40	180	12	2.16
60	140	16	2.24
80	90	20	1.80
100	50	25	1.25
120	5	29	0.15
then no important changes until			
500	5	25	0.14
520	40	25	1.00
540	80	20	1.60
560	130	15	1.95
580	180	10	1.80
600	220	5	1.10
620	260	1	0.26
until			
940	280	1	0.28
960	260	2	0.52

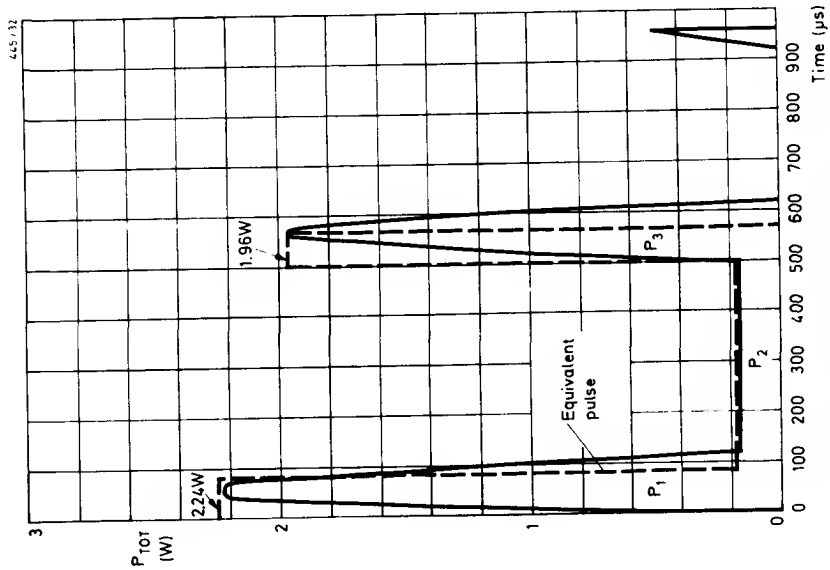


Fig. 9— P_{tot} against time characteristic showing equivalent squarewave pulses

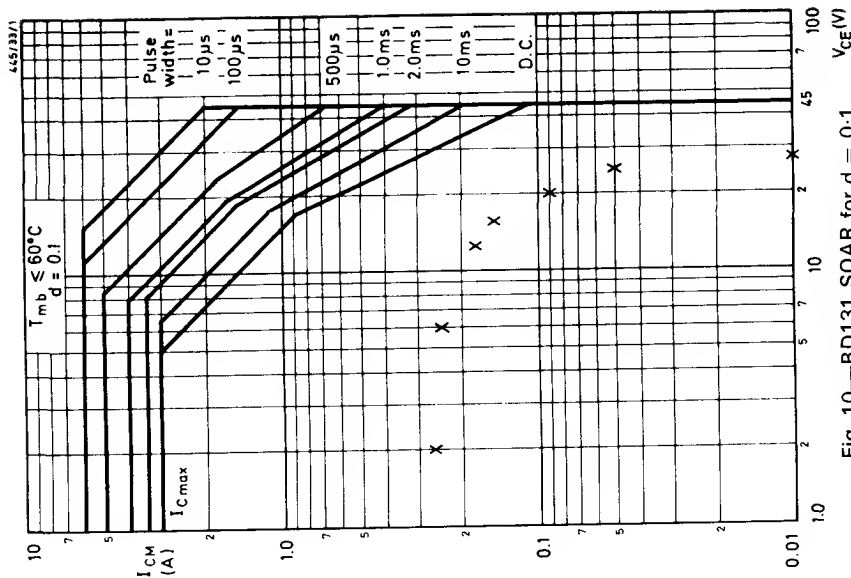


Fig. 10—BD131 SOAR for $d = 0.1$
(acceptability check for pulse P_1)

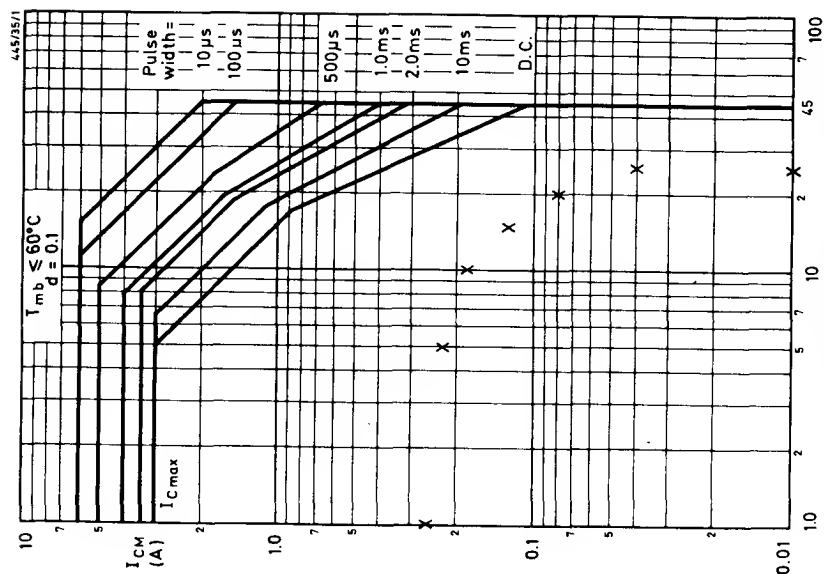


Fig. 12—BD131 SOAR for $d = 0.1$
(acceptability check for pulse P_3)

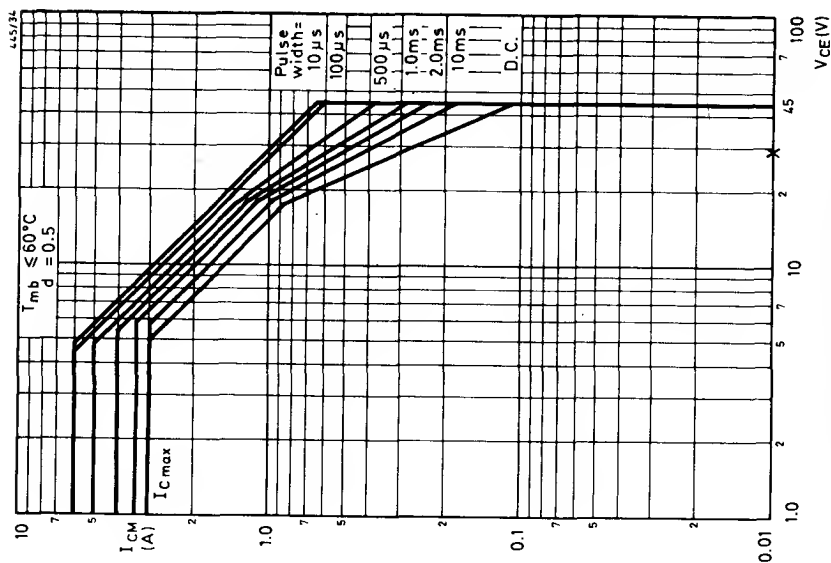


Fig. 11—BD131 SOAR for $d = 0.5$
(acceptability check for pulse P_2)

Consider pulse P_1 : the equivalent pulse time t_{p1} is $82.5\mu s$ and the total cycle time T is $960\mu s$. Therefore the duty cycle d_1 is $82.5/960$ or 0.086 . The V_{CE} and I_C values recorded up to the end of the pulse time t_{p1} are then plotted on the SOAR curve for $d = 0.1$ as shown in Fig. 10. The locus of this plot falls well within the $t_p = 100\mu s$ limit, therefore this condition is acceptable. In figs. 10 to 12, the $5mA$ point is plotted on the $10mA$ line for convenience, this makes no difference to the result.

The same procedure is followed for checking the acceptability of pulses P_2 and P_3 . For P_2 the duty cycle is $420/960$ or 0.44 ; thus the V_{CE} and I_C measurements recorded for pulse P_2 are plotted on the SOAR curve for $d = 0.5$ as shown in Fig. 11. For P_3 the duty cycle is $70/960$ or 0.073 , so the V_{CE} and I_C measurements recorded for pulse P_3 are again plotted on the SOAR curve for $d = 0.1$ as in Fig. 12.

In all three cases the pulse conditions are acceptable since not even the d.c. SOAR limits are exceeded. Thus, the transistor will not fail through second breakdown even when the amplifier is continuously overdriven.

Heatsink calculations

The heatsinks have to be designed to keep the junction temperature below the rating of $150^\circ C$. The known thermal restraints are the standard ambient temperature of $60^\circ C$ allowed for in television enclosures, and the thermal impedances associated with the BD131. The thermal impedance curves for the BD131 are shown in Fig. 13, and the contact thermal resistance $R_{th(mb-h)}$ is 1 degC/W .

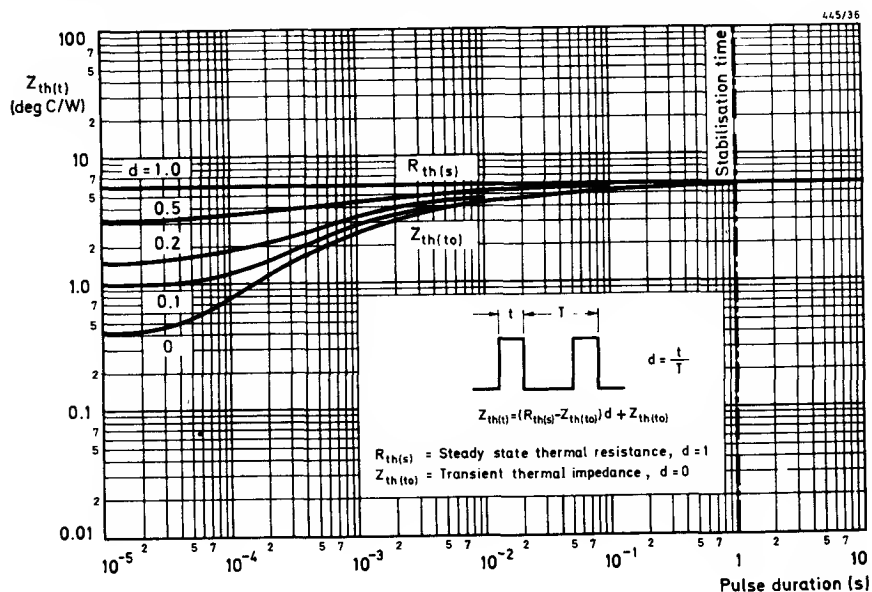


Fig. 13—Thermal impedance curves for BD131

The calculations used to determine the size of the required heatsinks involve average power values, as follows:

$$R_{th(h-a)} = \frac{T_{mbmax} - T_a}{P_{av}} - R_{th(mb-h)}, \quad \dots (1)$$

where: $T_{mbmax} = T_{jmax} - (T_j - T_{mb})_{max}. \quad \dots (2)$

Therefore: $R_{th(h-a)} = \left(\frac{T_{jmax} - (T_j - T_{mb})_{max} - T_a}{P_{av}} \right) - R_{th(mb-h)} \quad \dots (3)$

Two average powers have to be considered; that during the overload condition and that during the quiescent state. Since this is a class A amplifier, 2W will be dissipated in each of the output transistors during the quiescent condition, and this will be the d.c. bias condition. Under the overload condition the average power value is calculated as follows:

average heat input per cycle

$$= [(t_{p1} \times P_1) + (t_{p2} \times P_2) + (t_{p3} \times P_3)] / T, \quad \dots (4)$$

$$= [(82.5 \times 2.24) + (420 \times 0.15) + (70 \times 1.96)] / 960 = \frac{385 \mu s W}{960 \mu s} = 0.4 W.$$

The calculation of heatsink sizes should be determined under worst-case conditions. This occurs when the quiescent state is followed by the overload conditions. Since the average overload power is less than the quiescent power the first cycle of overload will define the $(T_j - T_{mb})_{max}$.

The maximum value of $(T_j - T_{mb})$ is to be the greater of the two values given by the equations (5) and (6) below.

$$(T_j - T_{mb})_{max} = P_Q \times R_{th} + (P_1 - P_Q) Z_{th} t_{p1}, \quad \dots (5)$$

$$\text{and } (T_j - T_{mb})_{max} = P_Q \times R_{th} + (P_1 - P_Q) Z_{th} (t_{p1} + t_{p2} + t_{p3})$$

$$- (P_1 - P_2) Z_{th} (t_{p2} + t_{p3}) + (P_3 - P_2) Z_{th} t_{p3}, \quad \dots (6)$$

where:

$$\text{quiescent power } P_Q = 2W$$

$$P_1 = 2.24W$$

$$P_2 = 0.15W$$

$$P_3 = 1.96W$$

$$t_{p1} = 82.5 \mu s$$

$$t_{p1} + t_{p2} + t_{p3} = 572.5 \mu s$$

$$t_{p2} + t_{p3} = 490.0 \mu s$$

$$t_{p3} = 70 \mu s$$

$$R_{th} = 6 \text{ degC/W}$$

$$Z_{th} t_{p1} = 0.72 \text{ degC/W}$$

$$Z_{th} (t_{p1} + t_{p2} + t_{p3}) = 2.0 \text{ degC/W}$$

$$Z_{th} (t_{p2} + t_{p3}) = 1.8 \text{ degC/W}$$

$$Z_{th} t_{p3} = 0.63 \text{ degC/W}.$$

Thus, Eq. 5 becomes:

$$(T_j - T_{mb})_{\max} = (2 \times 6) + (0.24 \times 0.72) = (12 + 0.2) = 12.2 \text{ degC}.$$

Eq. 6 becomes:

$$\begin{aligned} (T_j - T_{mb})_{\max} &= (2 \times 6) + (0.24 \times 2) - (2.09 \times 1.8) + (1.81 \times 0.63), \\ &= 12 + 0.48 - 3.76 + 1.14 = 9.9 \text{ degC}. \end{aligned}$$

Therefore the maximum value of $(T_j - T_{mb})$ is 12.2 degC from Eq. 5.

Thus Eq. 3 becomes:

$$R_{th(h-a)} = \left(\frac{150 - 12.2 - 60}{2} \right) - 1 = 37.9 \text{ degC/W}.$$

Therefore the maximum value of $(T_j - T_{mb})$ is 12.2 degC from Eq. 5.

Therefore heatsinks used for the BD131 transistors in this application should each have a thermal resistance of 37 degC/W or less. The foregoing calculations assume a contact thermal resistance value of 1 degC/W, which is true only if a heat-sink mounting compound is used.

APPENDIX I

Transistor heatsink sizes

The heatsink size for any transistor can be found from the nomogram shown in Fig. 14 provided that the power dissipation is no greater than 100W, and that the heat is dissipated by free convection. This nomogram should not be used where forced air cooling is employed, or where heatsink material other than aluminium is desired. The nomogram is operated as follows, with reference to the simplified curves in Fig. 15.

- 1) Calculate the worst-case dissipation P_{totmax} and hence the thermal resistance of heatsink to ambient $R_{th(h-a)}$. Thus:

$$R_{th(h-a)} = \frac{T_{mb\max} - T_{amb}}{P_{\text{tot}}} - R_{th(mb-h)}$$

- 2) Enter the nomogram in section I of Fig. 15. Move horizontally to the left until the appropriate orientation (either horizontal or vertical) and the appropriate surface finish is reached.
- 3) Move vertically upwards to intersect appropriate power dissipation curve (P_{tot}) in section II.
- 4) Move horizontally to intersect the curve in section III for the desired thickness of sheet aluminium heatsink. If an extrusion is required, move vertically upwards

from the point of intersection on the chosen extrusion curve and read off the required length on the top horizontal scale. (The 30D and 40D are shown in outline in Fig. 16. These types belong to the family of extrusions which has been used with Mullard power devices requiring special heatsink considerations, such as thyristor stacks and power rectifiers. Similar curves for alternative extrusions could also be plotted in section III using the heatsink manufacturer's data relating $R_{th(h-a)}$ and power, and length).

- 5) Move vertically down from point A in section III to intersect with the appropriate curve for the transistor encapsulation style.
- 6) Move horizontally to the left and read off the required area of one side of flat aluminium heatsink.
- 7) The heatsink dimensions of height to width should not exceed the ratio 1.25:1.

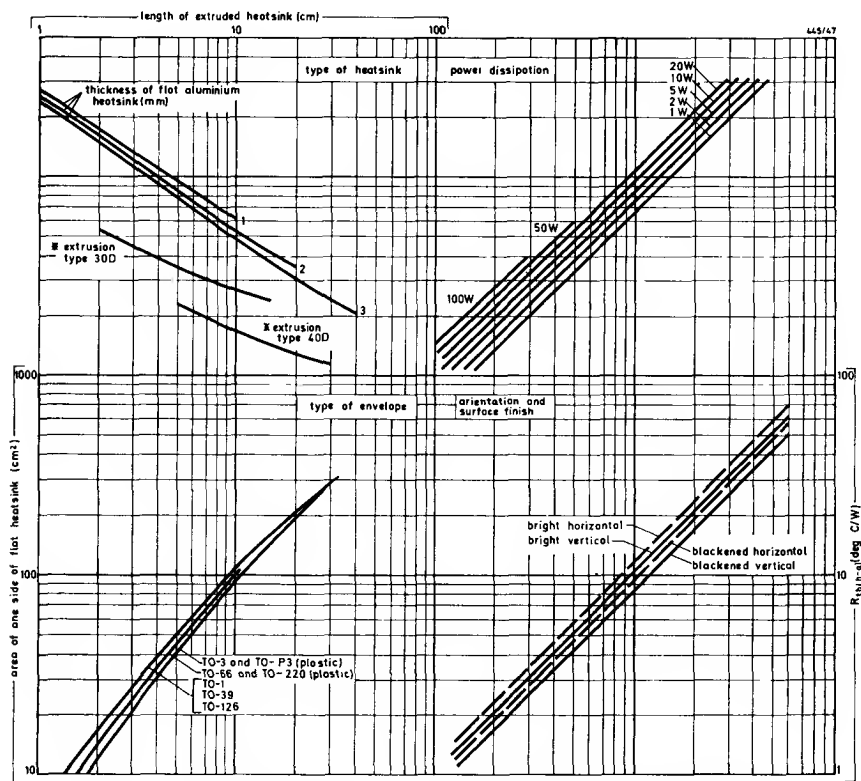


Fig. 14—Heatsink nomogram. * (For outlines of extrusions see Fig. 16)

length of extruded
heatsink (cm)

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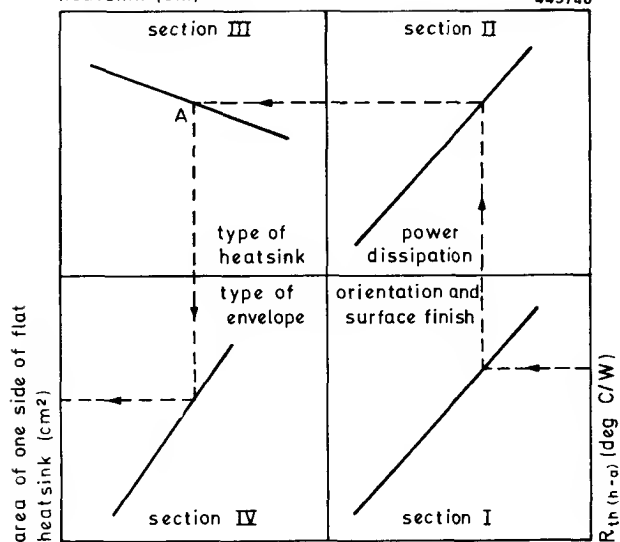
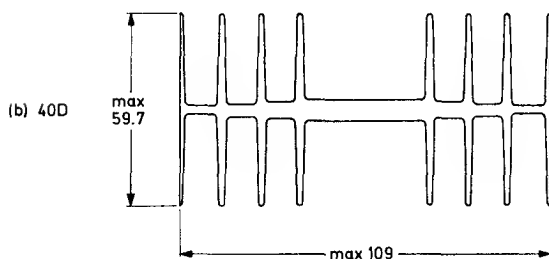
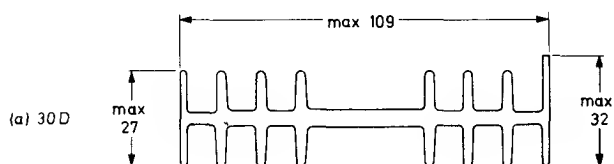


Fig. 15—Simplified nomogram



All dimensions in mm

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Fig. 16—Outlines of extrusions: (a) 30D, (b) 40D

Mullard

TRANSISTORS





DUAL N-CHANNEL FIELD EFFECT TRANSISTORS

BFQ10
to
BFQ16

Dual n-channel silicon planar epitaxial junction field-effect transistors in TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at $T_{amb} = 25^{\circ}\text{C}$; $I_D = 200 \mu\text{A}$; $V_{DG} = 15 \text{ V}$

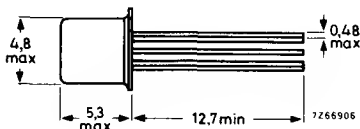
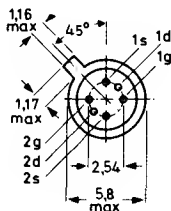
		BFQ10	11	12	13	14	15	16	
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left \frac{d \Delta V_{GS}}{dT} \right $	< 5	5	10	20	20	40	50	$\mu\text{V}/^{\circ}\text{C}$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0,98	0,98	0,98	0,98	0,98	0,95	0,95	
		< 1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance	$\left \Delta \frac{1}{g_{fs}} \right $	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 10	30	30	30	30	30	100	$\mu\text{V}/\text{V}$
Common mode rejection ratio	CMRR	> 100	90	90	90	90	90	80	dB

MECHANICAL DATA

Dimensions in mm

TO-71

All leads insulated from the case



Mullard

RATINGS Limiting values in accordance with the Absolute Maximum System

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V

Currents

Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA

Power dissipation

Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	250	mW
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Temperatures

Storage temperature	T_{stg}	-65 to +200	$^{\circ}\text{C}$
Junction temperature	T_j	max. 200	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	$^{\circ}\text{C}/\text{mW}$
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DUAL N-CHANNEL FIELD EFFECT TRANSISTORS

BFQ10
to
BFQ16

CHARACTERISTICS (total device)

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

Measured at: $I_D = 200\ \mu\text{A}$; $V_{DG} = 15\ \text{V}$ except for drain current ratio.

Drain current ratio 1)		BFQ10	11	12	13	14	15	16	
$V_{DG} = 15\ \text{V}$; $V_{GS} = 0$	$\frac{I_{1D-1SS}}{I_{2D-2SS}}$	$> 0,97$	0,95	0,95	0,95	0,92	0,90	0,80	
		$< 1,03$	1,05	1,05	1,05	1,08	1,10	1,20	
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left \frac{d \Delta V_{GS}}{dT} \right $	< 5	5	10	20	20	40	50	$\mu\text{V}/^{\circ}\text{C}$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	$> 0,98$	0,98	0,98	0,98	0,98	0,95	0,95	
		$< 1,02$	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance 2)	$\left \Delta \frac{1}{g_{fs}} \right $	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor 3)	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 10	30	30	30	30	30	100	$\mu\text{V}/\text{V}$
Common mode rejection ratio 4)	CMRR	> 100	90	90	90	90	90	80	dB

1) Measured under pulse conditions.

2) The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{g_{fs}} = \frac{d \Delta V_{GS}}{d I_D} \text{ at } V_{DG} = \text{constant} \right)$$

3) The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{g_{os}}{g_{fs}} = \frac{d \Delta V_{GS}}{d V_{DG}} \text{ at } I_D = \text{constant} \right)$$

4) Common mode rejection ratio

$$\text{CMRR (in dB)} = -20 \log \left| \Delta \frac{g_{os}}{g_{fs}} \right|$$

Mullard

CHARACTERISTICS (Individual transistor) $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specifiedGate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$

$-I_{GSS} < 100\text{ pA}$

$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 125\text{ }^{\circ}\text{C}$

$-I_{GSS} < 20\text{ nA}$

Gate current

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}; T_{amb} = 125\text{ }^{\circ}\text{C}$

$I_G < 10\text{ nA}$

Drain current

$V_{DS} = 15\text{ V}; V_{GS} = 0$

$I_{DSS} 0,5\text{ to }10\text{ mA }^1)$

Gate-source voltage

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$-V_{GS} < 2,7\text{ V}$

Gate-source cut-off voltage

$I_D = 1\text{ nA}; V_{DG} = 15\text{ V}$

$-V_{(P)GS} 0,5\text{ to }3,5\text{ V}$

Transfer conductance at $f = 1\text{ kHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$g_{fs} > 1,0\text{ mA/V}$

Output conductance at $f = 1\text{ kHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$g_{os} < 5\text{ }\mu\text{A/V}$

Input capacitance at $f = 1\text{ MHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$C_{is} < 8\text{ pF }^2)$

Feedback capacitance at $f = 1\text{ MHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$C_{rs} < 1,0\text{ pF }^2)$

Equivalent noise voltage

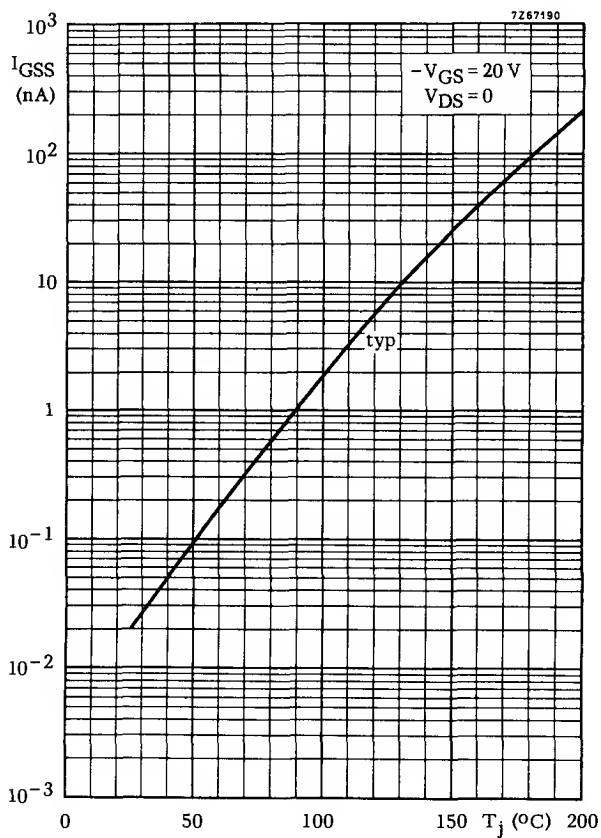
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$
 $B = 0,6\text{ to }100\text{ Hz}$

$V_n < 0,5\text{ }\mu\text{V}$

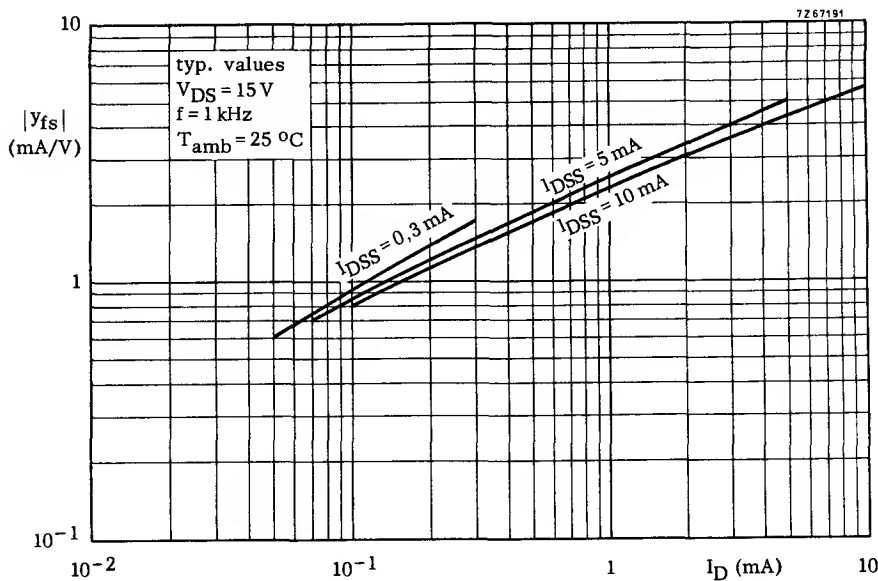
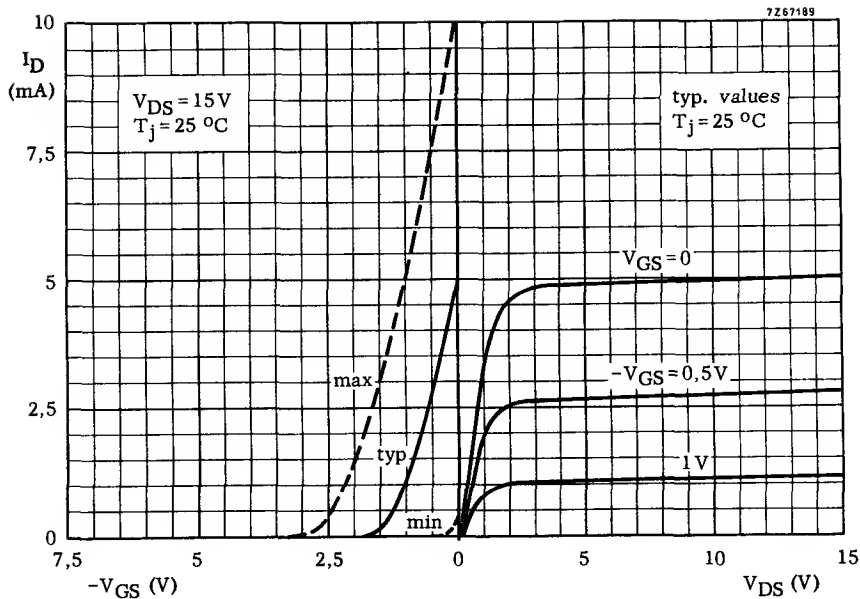
¹⁾ Measured under pulse conditions.²⁾ Measured with case grounded.

**DUAL N-CHANNEL
FIELD EFFECT TRANSISTORS**

**BFQ10
to
BFQ16**



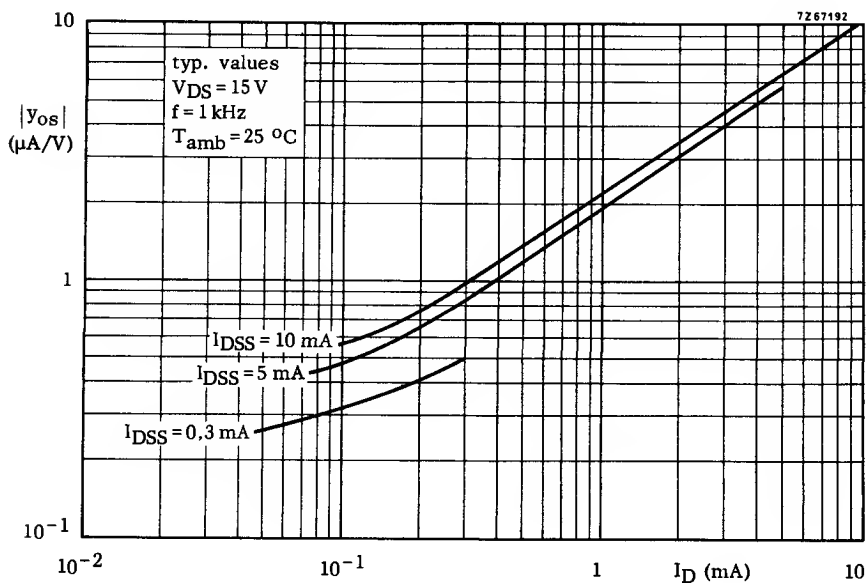
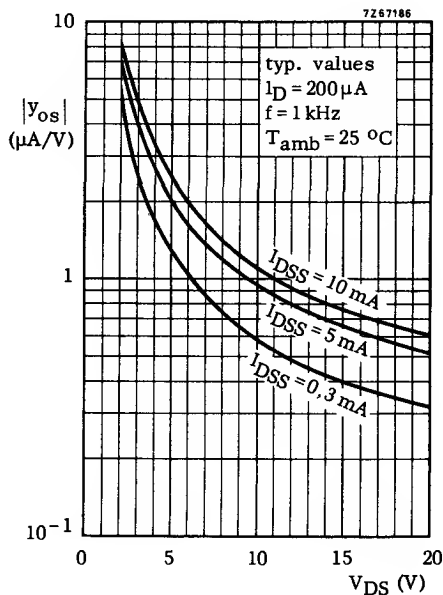
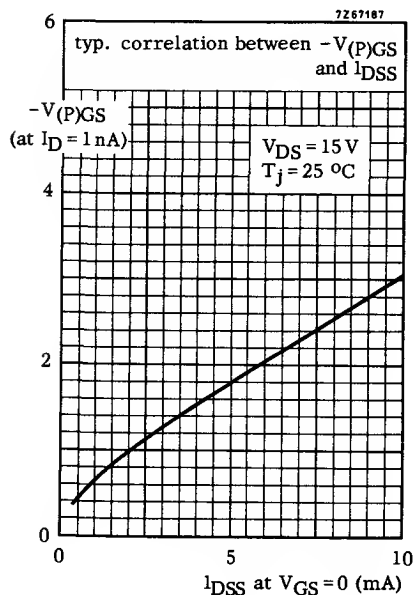
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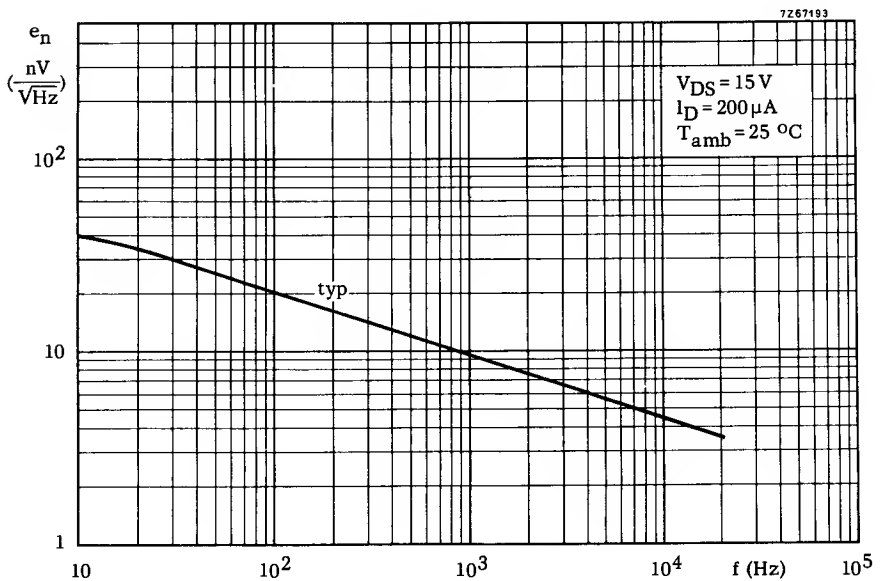
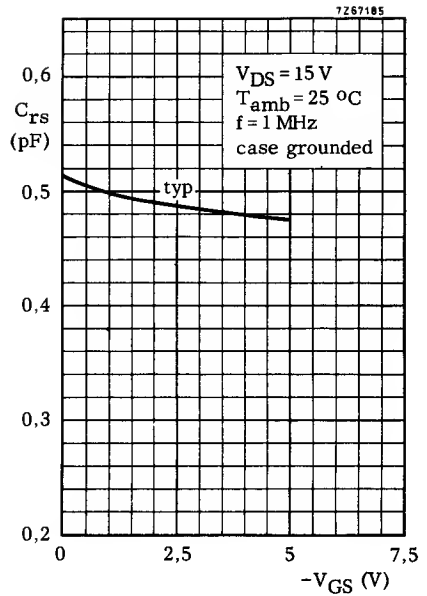
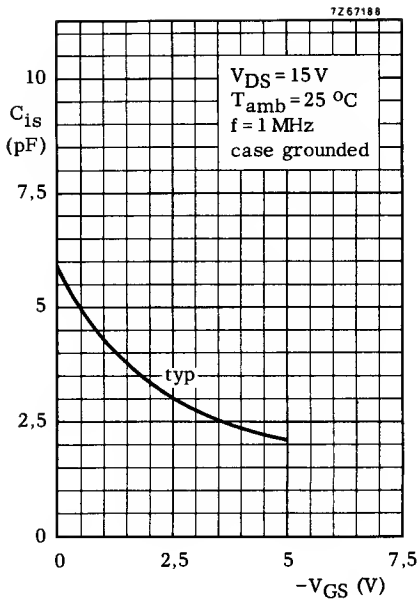
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DUAL N-CANNEL FIELD EFFECT TRANSISTORS

BFQ10
to
BFQ16



Mullard



N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

BFR29

Depletion type, insulated gate, field effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the l.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

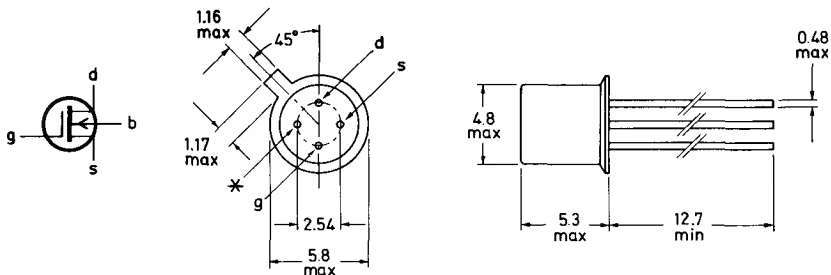
QUICK REFERENCE DATA

V_{DB} max.	30	V
$\pm V_{GB}$ max.	10	V
I_{DSS} ($V_{DS} = 15V$, $V_{GS} = 0$)	10 to 40	mA
$ y_{fs} $ min. ($I_D = 5mA$, $V_{DS} = 15V$, $f = 1kHz$)	6.0	mA/V
$-C_{rs}$ max. ($I_D = 5mA$, $V_{DS} = 15V$, $f = 1MHz$)	0.7	pF
N max. ($I_D = 5mA$, $V_{DS} = 15V$, $f = 200MHz$, $G_S = 1mA/V$, $B_S = \text{optimum}$)	5.0	dB
V_n/\sqrt{B} typ. ($I_D = 5mA$, $V_{DS} = 15V$, $f = 1kHz$)	100	nV/ \sqrt{Hz}

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB4-3

J. E. D. E. C. TO-72



* Substrate connected to envelope

All dimensions in mm

D 3925

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conductive rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DB} max.	Drain-substrate voltage	30	V
V_{SB} max.	Source-substrate voltage	30	V
$\pm V_{GB}$ max.	Gate-substrate voltage (continuous)	10	V
$\pm V_{G-N}$ max.	Repetitive peak gate voltage (gate to all other terminals) $V_{SB} = V_{DB} = 0, f > 100\text{Hz}$	15	V
I_D max.	Drain current (d.c.)	20	mA
I_{DM} max.	Peak drain current $t_r = 20\text{ms}, d = 0, 1$	50	mA
P_{tot} max.	Total power dissipation $T_{amb} \leq 25^\circ\text{C}$	200	mW

Temperature

T_{stg}	Storage temperature	-65 to +125	$^\circ\text{C}$
T_j max.	Junction temperature	125	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance, junction to ambient, in free air	0.5	degC/mW
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

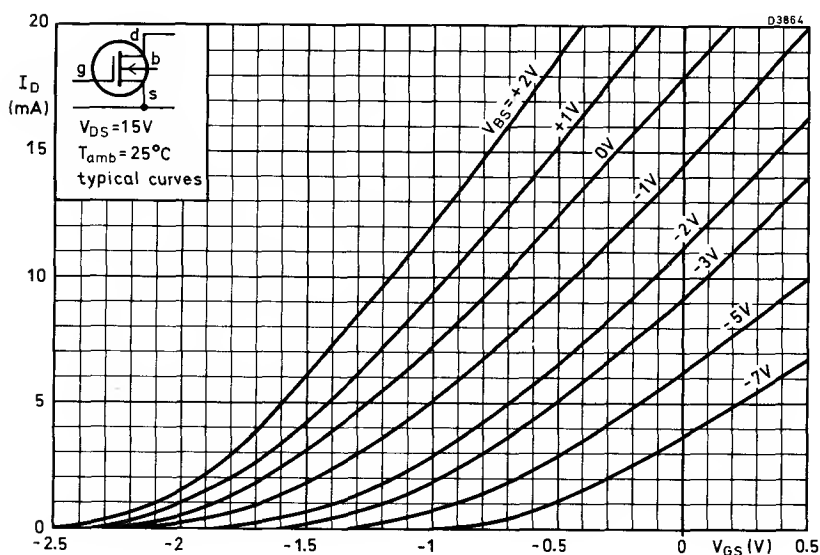
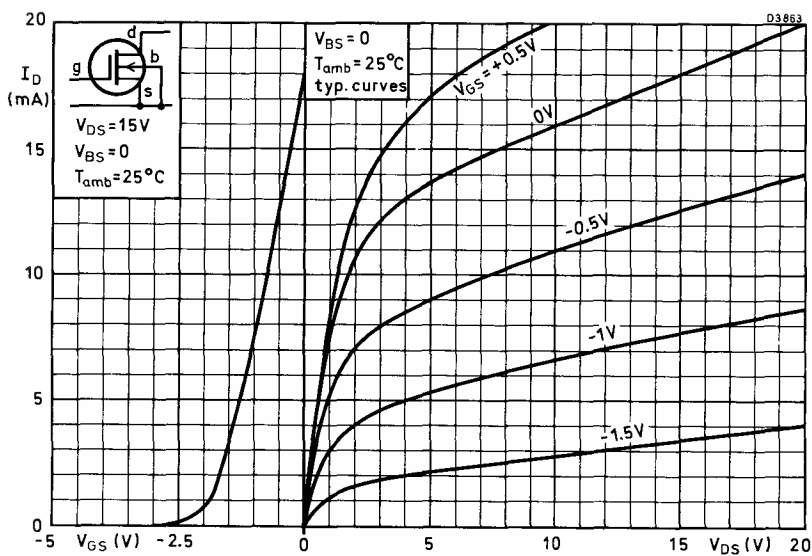
		Min.	Typ.	Max.	
	Gate current, $V_{BS} = 0$				
$-I_{GSS}$	$-V_{GS} = 10\text{V}, V_{DS} = 0$	-	-	10	pA
I_{GSS}	$V_{GS} = 10\text{V}, V_{DS} = 0$	-	-	10	pA
$-I_{GSS}$	$-V_{GS} = 10\text{V}, V_{DS} = 0, T_j = 125^\circ\text{C}$	-	-	200	pA
I_{GSS}	$V_{GS} = 10\text{V}, V_{DS} = 0, T_j = 125^\circ\text{C}$	-	-	200	pA
	Substrate current, $V_{GB} = 0$				
$-I_{BDO}$	$-V_{BD} = 30\text{V}, I_S = 0$	-	-	10	μA
$-I_{BSO}$	$-V_{BS} = 30\text{V}, I_D = 0$	-	-	10	μA
I_{DSS}	Drain current $V_{DS} = 15\text{V}, V_{GS} = 0$	10	-	40	mA
$-V_{GS}$	Gate-source voltage $I_D = 100\text{nA}, V_{DS} = 15\text{V}$	0.5	-	3.5	V

N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

BFR29

ELECTRICAL CHARACTERISTICS (contd.)

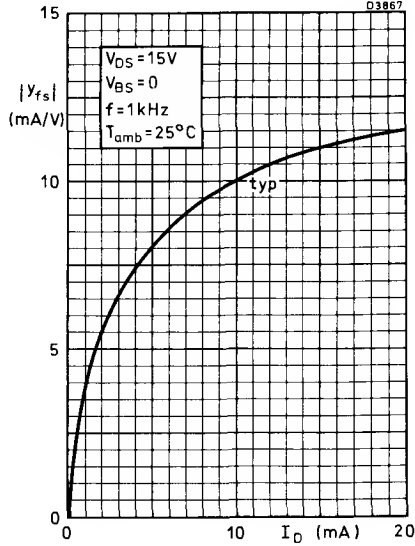
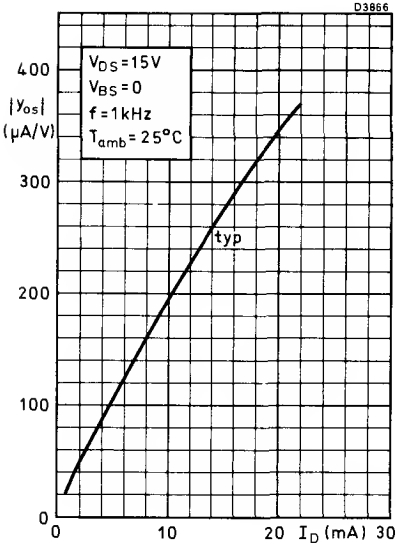
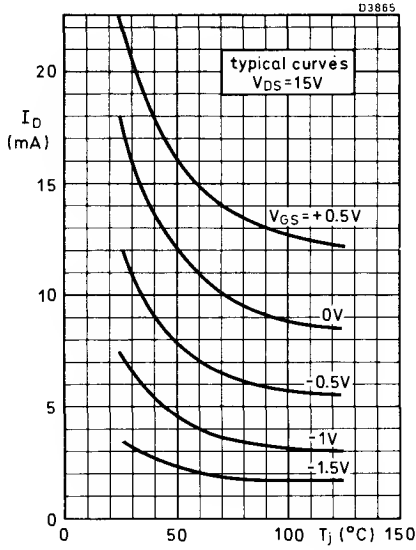
		Min.	Typ.	Max.	
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 100nA, V_{DS} = 15V$	-	-	4.0	V
N	Noise figure at $f = 200MHz$ $I_D = 5mA, V_{DS} = 15V, T_{amb} = 25^{\circ}C$ $G_S = 1mA/V, B_S = \text{optimum}$	-	-	5.0	dB
V_n / \sqrt{B}	Equivalent noise voltage, $T_{amb} = 25^{\circ}C$ $I_D = 5mA, V_{DS} = 15V, f = 120Hz$	-	300	-	nV / \sqrt{Hz}
	$f = 1kHz$	-	100	-	nV / \sqrt{Hz}
	$f = 10kHz$	-	35	-	nV / \sqrt{Hz}
y-parameters					
$I_D = 5mA, V_{DS} = 15V, T_{amb} = 25^{\circ}C$					
$ y_{fs} $	Transfer admittance at $f = 1kHz$	6.0	-	-	mA/V
$ y_{os} $	Output admittance at $f = 1kHz$	-	-	0.4	mA/V
C_{is}	Input capacitance at $f = 1MHz$	-	-	5.0	pF
$-C_{rs}$	Feedback capacitance at $f = 1MHz$	-	-	0.7	pF
C_{os}	Output capacitance at $f = 1MHz$	-	-	3.0	pF



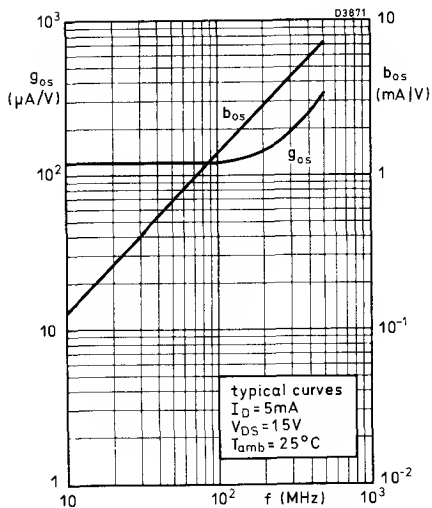
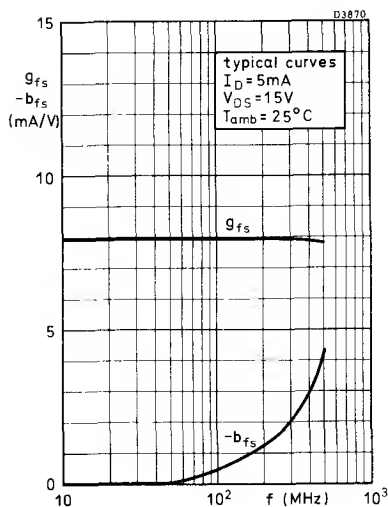
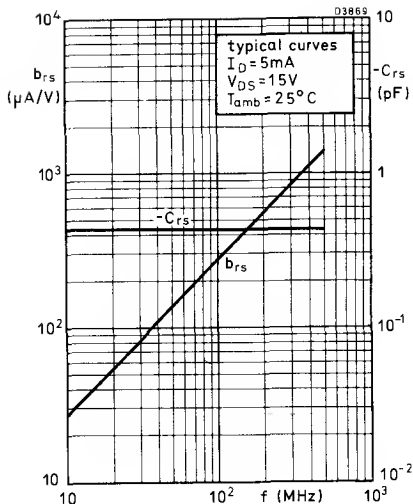
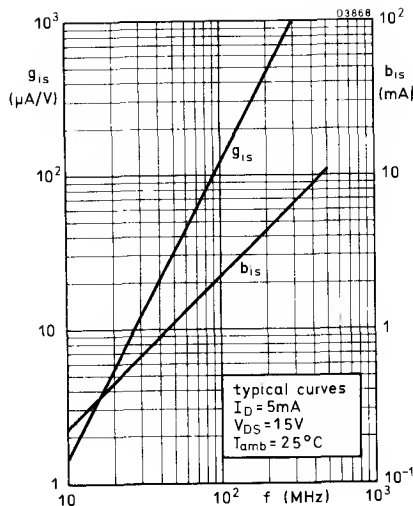
Mullard

N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

BFR29

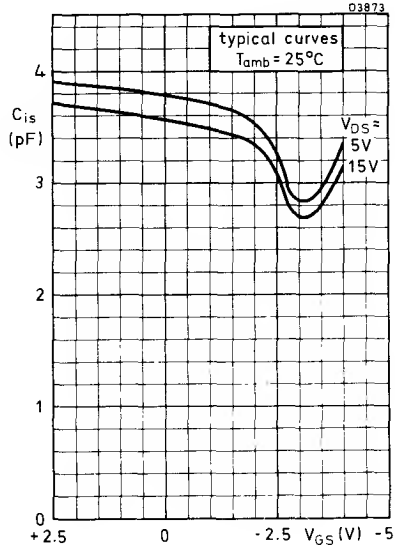
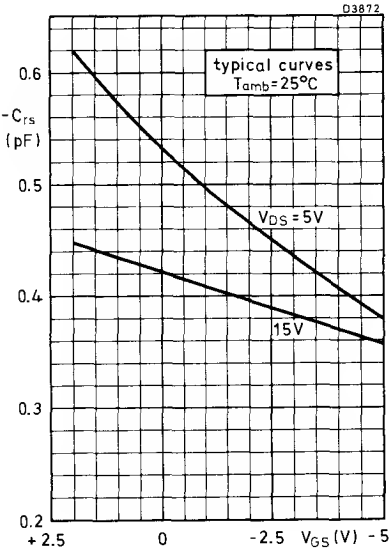


Mullard



N-CHANNEL INSULATED GATE
FIELD EFFECT TRANSISTOR

BFR29

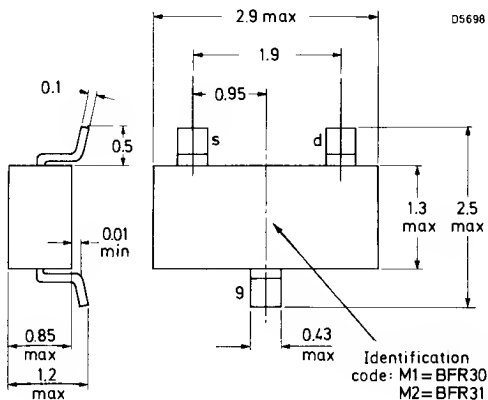


BFR30
BFR31

QUICK REFERENCE DATA

$\pm V_{DS}$	max.	25	V	
$-V_{GSO}$	max.	25	V	
P_{tot}	max. ($T_{amb} \leq 25^{\circ}C$)	200	mW	
		BFR30	BFR31	
I_{DSS} ($V_{DS} = 10V$, $V_{GS} = 0$)	min.	4.0	1.0	mA
	max.	10	5.0	mA
$ y_{fs} $ ($I_D = 1mA$, $V_{DS} = 10V$, $f = 1kHz$)	min.	1.0	1.5	mA/V
	max.	4.0	4.5	mA/V

OUTLINE AND DIMENSIONS



Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$	max.	Drain-source voltage	25	V
V_{DGO}	max.	Drain-gate voltage (open source)	25	V
$-V_{GSO}$	max.	Gate-source voltage (open drain)	25	V
I_D	max.	Drain current	10	mA
I_G	max.	Gate current	5.0	mA
P_{tot}	max.	Power dissipation ($T_{amb} \leq 25^{\circ}\text{C}$) mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	200	mW

Temperature

T_{stg}		Storage temperature	-65 to +150	$^{\circ}\text{C}$
T_j	max.	Junction temperature	150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

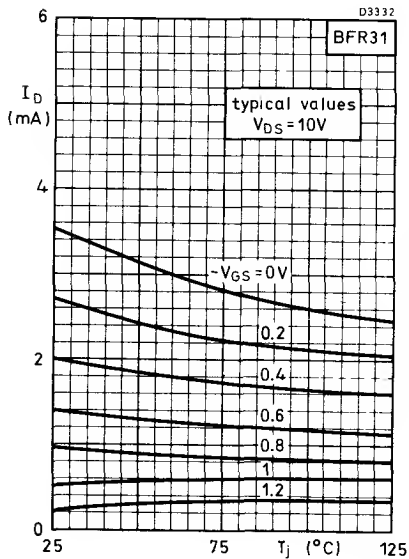
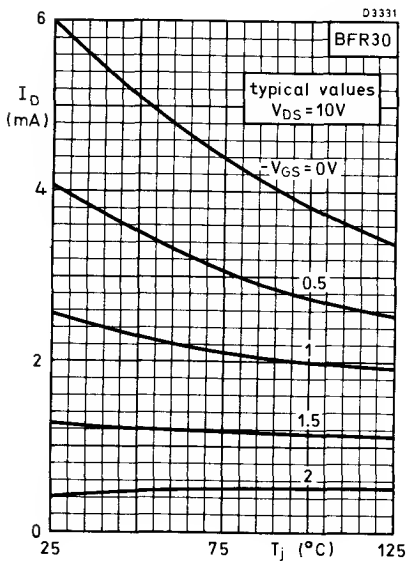
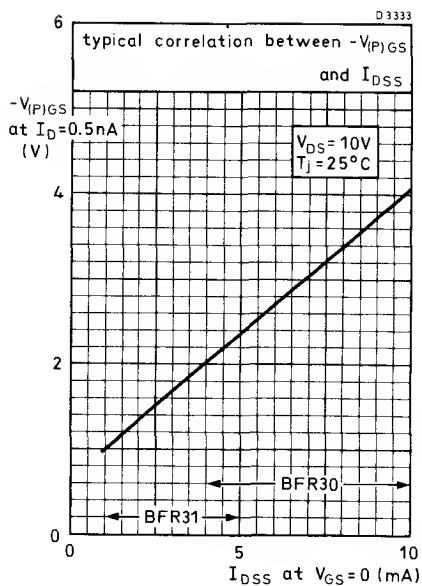
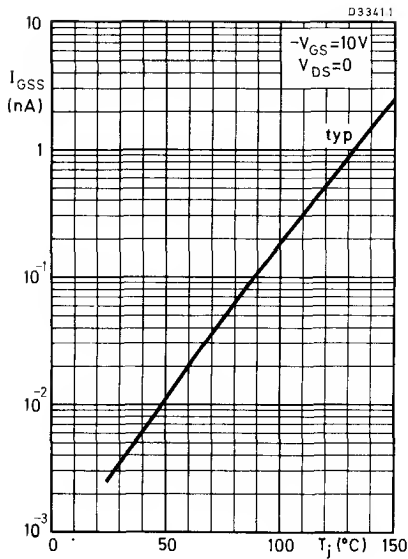
$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	0.62	$^{\circ}\text{C/mW}$
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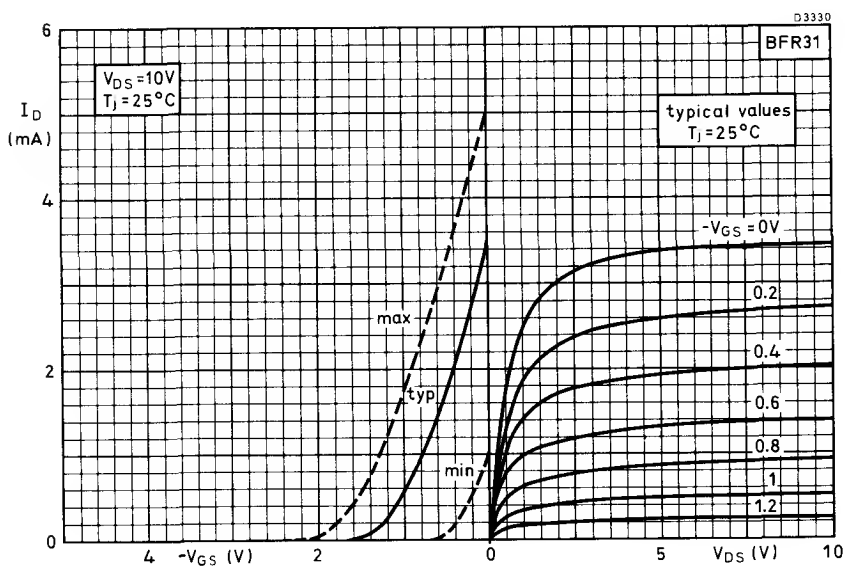
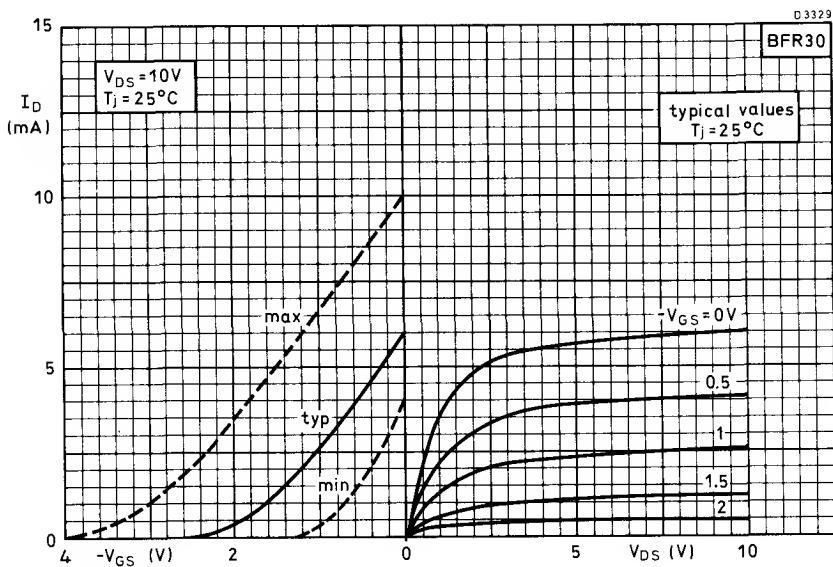
ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

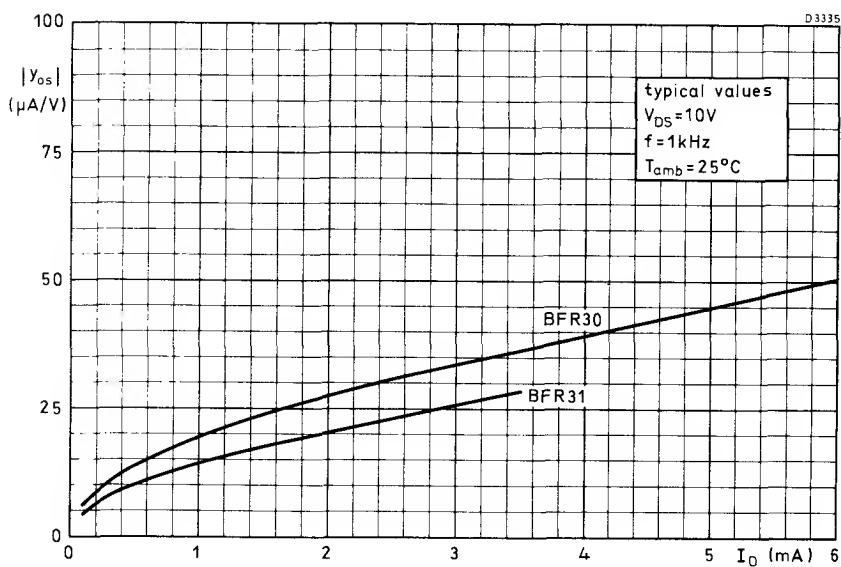
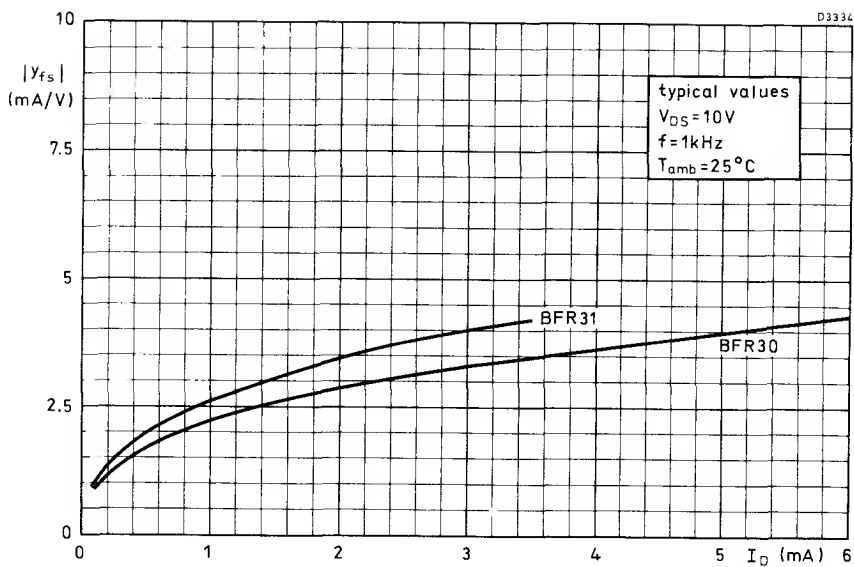
			Min.	Max.	
$-I_{GSS}$	Gate cut-off current $-V_{GS} = 10\text{V}, V_{DS} = 0$		-	0.2	nA
I_{DSS}	Drain current $V_{DS} = 10\text{V}, V_{GS} = 0$	BFR 30	4.0	10	mA
		BFR 31	1.0	5.0	mA
$-V_{GS}$	Gate-source voltage $I_D = 1\text{mA}, V_{DS} = 10\text{V}$	BFR 30	0.7	3.0	V
		BFR 31	0	1.3	V
	$I_D = 50\mu\text{A}, V_{DS} = 10\text{V}$	BFR 30	-	4.0	V
		BFR 31	-	2.0	V
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 0.5\text{nA}, V_{DS} = 10\text{V}$	BFR 30	-	5.0	V
		BFR 31	-	2.5	V

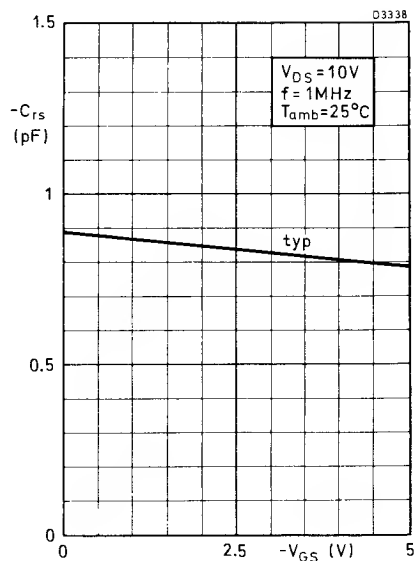
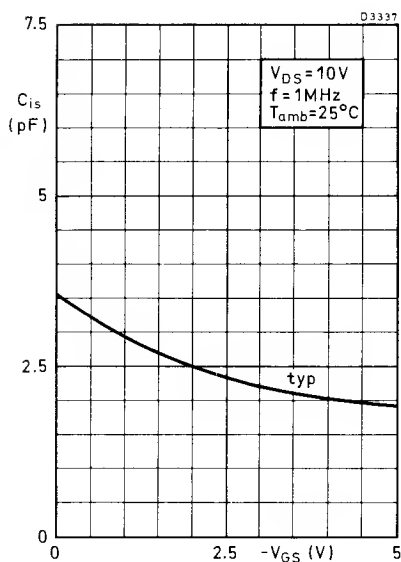
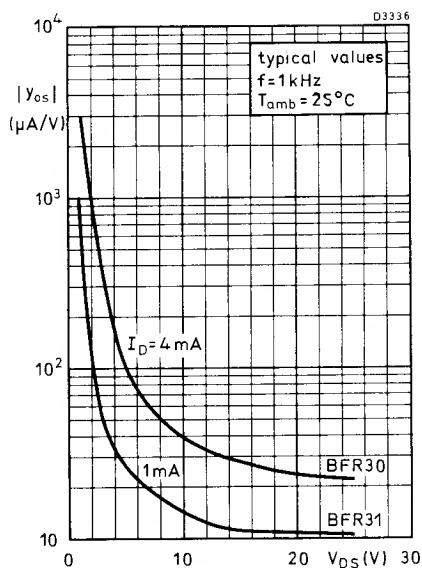
ELECTRICAL CHARACTERISTICS (contd.)

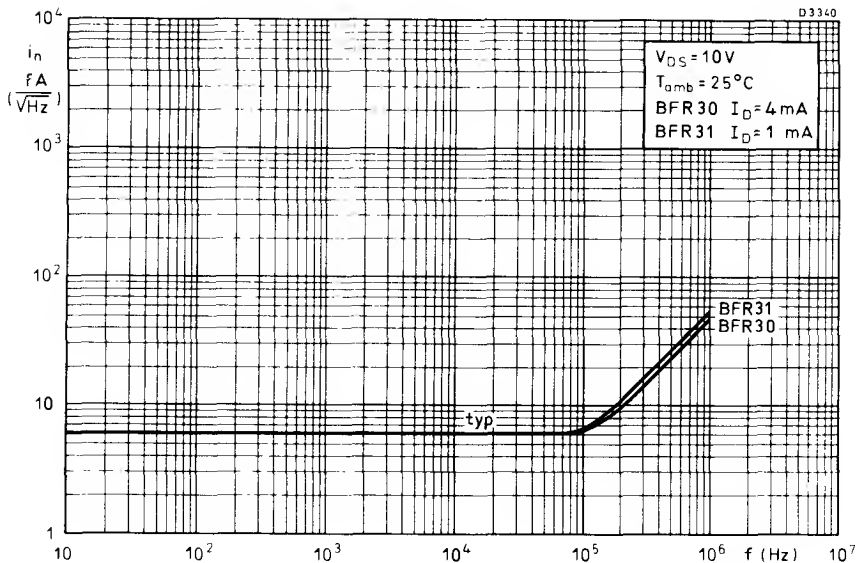
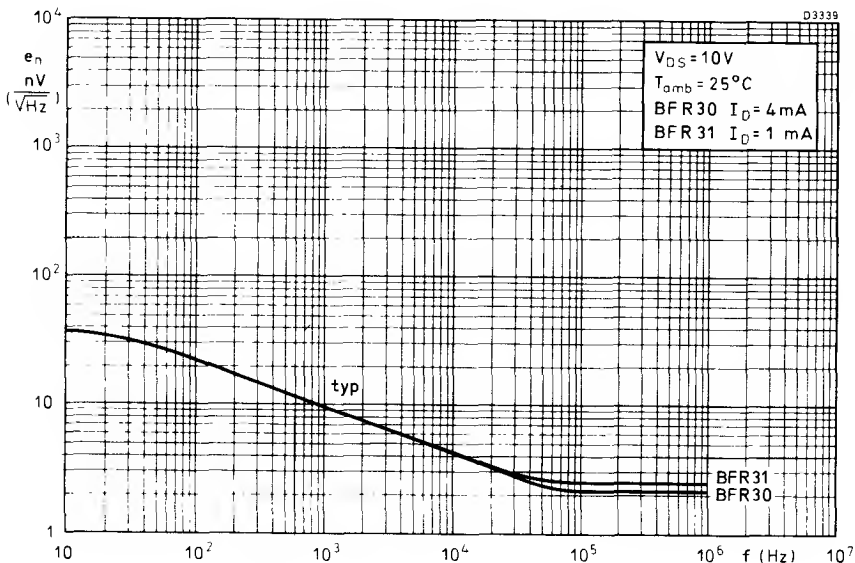
			Min.	Max.	
y-parameters, $T_{amb} = 25^{\circ}\text{C}$					
$ y_{fs} $	Transfer admittance at $f = 1\text{kHz}$ $I_D = 1\text{mA}, V_{DS} = 10\text{V}$	BFR30	1.0	4.0	mA/V
		BFR31	1.5	4.5	mA/V
	$I_D = 200\mu\text{A}, V_{DS} = 10\text{V}$	BFR30	0.5	-	mA/V
		BFR31	0.75	-	mA/V
$ y_{os} $	Output admittance at $f = 1\text{kHz}$ $I_D = 1\text{mA}, V_{DS} = 10\text{V}$	BFR30	-	40	$\mu\text{A/V}$
		BFR31	-	25	$\mu\text{A/V}$
	$I_D = 200\mu\text{A}, V_{DS} = 10\text{V}$	BFR30	-	20	$\mu\text{A/V}$
		BFR31	-	15	$\mu\text{A/V}$
C_{is}	Input capacitance at $f = 1\text{MHz}$ $I_D = 1\text{mA}, V_{DS} = 10\text{V}$		-	4.0	pF
			-	4.0	pF
C_{rs}	Feedback capacitance at $f = 1\text{MHz}$, $I_D = 1\text{mA}, V_{DS} = 10\text{V}, T_{amb} = 25^{\circ}\text{C}$		-	1.5	pF
			-	1.5	pF
V_n	Equivalent noise voltage $I_D = 200\mu\text{A}, V_{DS} = 10\text{V}$ $B = 0.6 \text{ to } 100\text{Hz}$		-	0.5	μV











N-P-N multi-emitter silicon transistors in capstan envelopes. The transistors have extremely good intermodulation properties and high power gain.

The devices are intended for:

- Final and driver stages of channel and band aerial amplifiers with high output power for band I, II, III and IV/V (40 to 860MHz).
- Final and driver stages of wideband amplifiers (40 to 230MHz).
- Final stages of the wideband vertical amplifier in high speed oscilloscopes.
- Frequency multiplier and oscillator circuits.

QUICK REFERENCE DATA

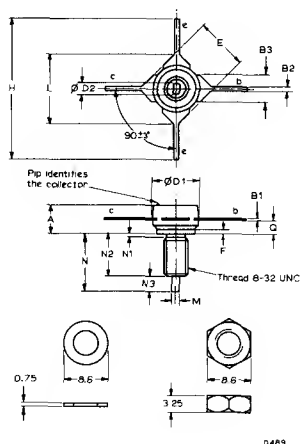
V _{CBOM} max. (peak value)	40	V	
V _{CEO} max.	25	V	
I _{CM} max.	500	mA	
P _{tot} max. (T _{mb} ≤ 60°C, f ≥ 1MHz)	3.5	W	
T _j max.	150	°C	
	BFR63	BFR64	
f _T min. (f = 500MHz, I _C = 75mA, V _{CE} = 20V)	1000	1200	MHz
P _o typ. (f = 200MHz, I _C = 70mA, V _{CE} = 20V, d _{im} = -30dB)	150	150	mW
G _p typ. (f = 200MHz, I _C = 70mA, V _{CE} = 20V)	16	16	dB

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

For details see page 2

OUTLINE AND DIMENSIONS



Millimetres

	Min.	Max.
A	5.25	5.75
B1	0.107	0.147
B2	0.7	1.1
B3	5.60	5.85
ØD1	9.0	9.6
ØD2	2.7	2.9
E	10.5	10.7
F	1.0	1.5
H	25.0	29.0
L	14 nom.	
M	1.4	1.6
N	11.2	12.0
N1	-	1.6
N2	7.5	8.5
N3	2.93	3.68
Q	2.85	3.00

Diameter of hole in heatsink: max 4.17mm

Torque on nut

min. 7.5kg cm (0.75N m)

max. 8.5kg cm (0.85N m)

When locking is required, an adhesive instead of a lock washer is preferred.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFR63
BFR64

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak value, $I_C = 100\mu A$)	40	V
V_{CERM} max. (peak value, $R_{BE} = 10\Omega$, $I_C = 10mA$)	40	V
V_{CEO} max. ($I_C = 10mA$)	25	V
V_{EBO} max. ($I_E = 100\mu A$)	3.5	V
I_C max.	200	mA
I_{CM} max. (peak value, $f > 1.0MHz$)	500	mA
P_{tot} max. ($T_{mb} \leq 60^\circ C$, $f \geq 1.0MHz$)	3.5	W

Temperature

T_{stg}	-40 to +150	$^\circ C$
T_j max.	150	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	25	degC/W
$R_{th(mb-h)}$	0.5	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 20V$	-	-	10	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100mA$, $I_B = 10mA$	-	-	0.75	V
h_{FE}	Static forward current transfer ratio $I_C = 50mA$, $V_{CE} = 5V$	25	-	-	
	$I_C = 150mA$, $V_{CE} = 5V$	25	-	-	
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 20V$, $f = 1.0MHz$	-	-	4.5	pF
$-C_{re}$	Feedback capacitance $I_C = 10mA$, $V_{CE} = 20V$, $f = 1.0MHz$, $T_{mb} = 25^\circ C$	-	1.7	-	pF
N	Noise figure $I_C = 40mA$, $V_{CE} = 20V$, $f = 200MHz$, $R_S = 75\Omega$, $T_{mb} = 25^\circ C$	-	6.0	-	dB

Mullard

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
f_T	Transition frequency at $f = 500\text{MHz}$					
	$I_C = 15\text{mA}$, $V_{CE} = 20\text{V}$	BFR64	-	1000	-	MHz
	$I_C = 75\text{mA}$, $V_{CE} = 20\text{V}$	BFR63	1000	-	-	MHz
		BFR64	1200	-	-	MHz
	$I_C = 150\text{mA}$, $V_{CE} = 20\text{V}$	BFR63	-	1100	-	MHz
		BFR64	-	1200	-	MHz
P_o	*Output power at $f = 200\text{MHz}$, $T_{mb} = 25^\circ\text{C}$					
	$I_C = 70\text{mA}$, $V_{CE} = 20\text{V}$, v.s.w.r. at output < 2					
	$f_p = 202\text{MHz}$, $f_q = 205\text{MHz}$, $d_{im} = -30\text{dB}$					
	measured at $f_{(2q-p)} = 208\text{MHz}$ (channel 9)					
		BFR63	-	150	-	mW
P_o		BFR64	130	150	-	mW
	**Output power at $f = 800\text{MHz}$, $T_{mb} = 25^\circ\text{C}$					
	$I_C = 70\text{mA}$, $V_{CE} = 20\text{V}$, v.s.w.r. at output < 2					
	$f_p = 798\text{MHz}$, $f_q = 802\text{MHz}$, $d_{im} = -30\text{dB}$					
	measured at $f_{(2q-p)} = 806\text{MHz}$ (channel 62)					
G_p		BFR64	70	90	-	mW
	Power gain (not neutralised)					
	$I_C = 70\text{mA}$, $V_{CE} = 20\text{V}$, $T_{mb} = 25^\circ\text{C}$,					
	$f = 200\text{MHz}$	BFR63	-	16	-	dB
		BFR64	15	16	-	dB
G_p	$f = 800\text{MHz}$	BFR64	-	6.5	-	dB

*See test circuit etc. on Page 5

**See test circuit etc. on Page 6

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

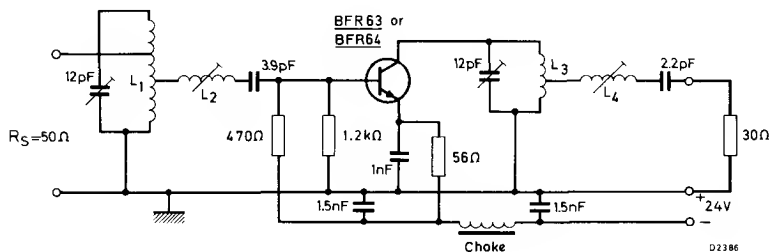
Devices requiring disposal may be returned to the Mullard Service Dept. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from the Service Department, Mullard Limited, New Road, Mitcham, Surrey.

ELECTRICAL CHARACTERISTICS (contd.)

Intermodulation characteristics

- Output power at $f = 200\text{MHz}$, $T_{mb} = 25^\circ\text{C}$
 $I_C = 70\text{mA}$, $V_{CE} = 20\text{V}$, v.s.w.r. at output < 2 ,
 $f_p = 202\text{MHz}$, $f_q = 205\text{MHz}$, $d_{im} = -30\text{dB}$,
 measured at $f_{(2q-p)} = 208\text{MHz}$ (channel 9)

Test circuit



$L_1 = 3$ turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.

$L_2 = 5.5$ turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.

$L_3 = 3$ turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.

$L_4 = 5.5$ turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

Basis of adjustment

Intermodulation distortion at $d_{im} = -30\text{dB}$ is caused by clipping in h.f. output current and voltage.

The maximum undistorted output power is attained when

- Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek}) / I_C$$

Where V_{cek} is the high frequency knee voltage

ELECTRICAL CHARACTERISTICS (contd.)

Basic of adjustment (contd.)

(b) The h.f. collector current is as low as possible; this occurs if

$$-C_{\text{load}} = +C_{\text{oe}}$$

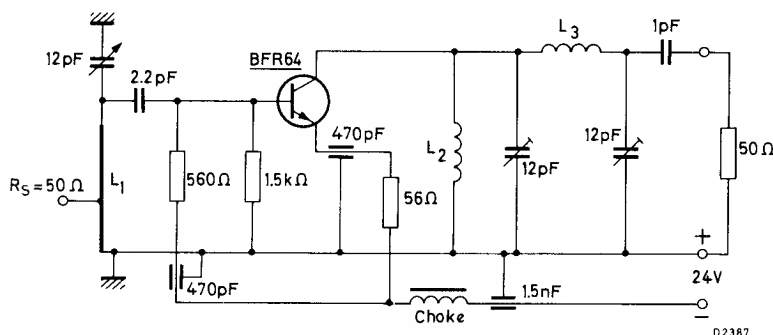
Where C_{oe} is the output capacitance of the transistor with short-circuited input. Experimentally obtained values of R_{load} and C_{load} , for maximum output power at an intermodulation factor of -30dB, are:

$$R_{\text{load}} = 220\Omega, C_{\text{load}} = -4\text{pF}$$

Procedure

1. Remove the transistor and connect a dummy load, consisting of a 220Ω resistor in parallel with a 4pF capacitor, between the collector and the emitter connections of the output circuit.
 2. Tune and match the output circuit for zero reflection at 205MHz (i.e. v.s.w.r.=1).
 3. Replace the dummy load by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L_2 , this will not disturb the bandpass curve.
2. Output power at $f = 800\text{MHz}$, $T_{\text{mb}} = 25^\circ\text{C}$
 $I_{\text{C}} = 70\text{mA}$, $V_{\text{CE}} = 20\text{V}$, v.s.w.r. at output < 2 ,
 $f_{\text{p}} = 798\text{MHz}$, $f_{\text{q}} = 802\text{MHz}$, $d_{\text{im}} = -30\text{dB}$,
 measured at $f_{(2q-p)} = 806\text{MHz}$ (channel 62)

Test circuit



$L_1 = 25 \times 7 \times 0.85\text{mm}$ silver plated copper strip, input tap at 5mm from earth.

$L_2 = 13$ turns of 0.6mm enamelled copper wire, int. dia. 8mm .

$L_3 = 1.5$ turns of 1.3mm copper wire, int. dia. 8mm .

ELECTRICAL CHARACTERISTICS (contd.)

Basis of adjustment

At 800MHz a dummy load cannot be used to adjust for optimum collector load, because at these frequencies the impedance transformations of the dummy load are too high.

A small signal with a frequency of the midchannel 802MHz is fed to the input. The signal is increased until clipping occurs, that is until the output power no longer increases linearly with increasing input signal. Care should be taken not to allow the voltage swing to exceed the V_{CEr} value as this may result in the destruction of the transistor by second breakdown.

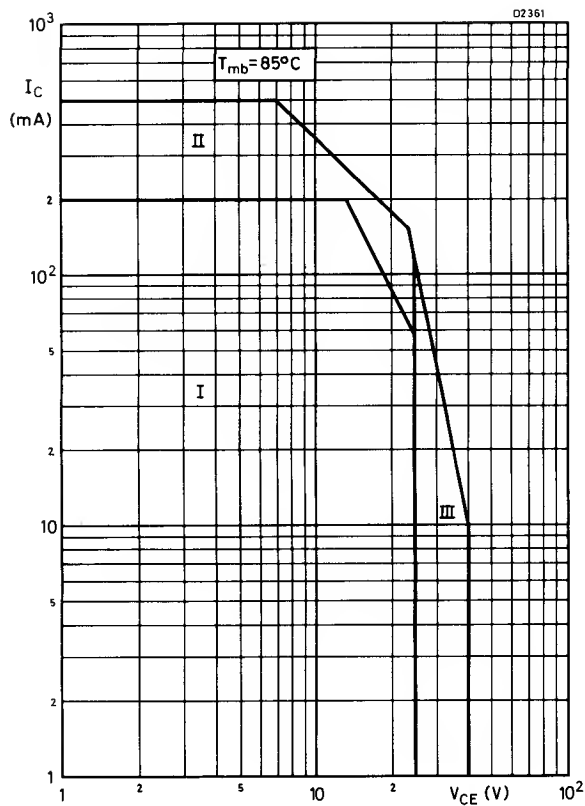
The output circuit is then tuned to eliminate clipping.

The output P_o is given by

$$P_o = I_C(V_{CE} - V_{cek})/2 = 480mW$$

where V_{cek} is the high frequency knee voltage

Keeping the input signal as small as possible at $P_o = 480mW$, the output circuit is adjusted for minimum intermodulation. The input circuit is then adjusted for maximum gain and good bandpass curve. The v.s.w.r. is found to be ≤ 2 over the whole channel.

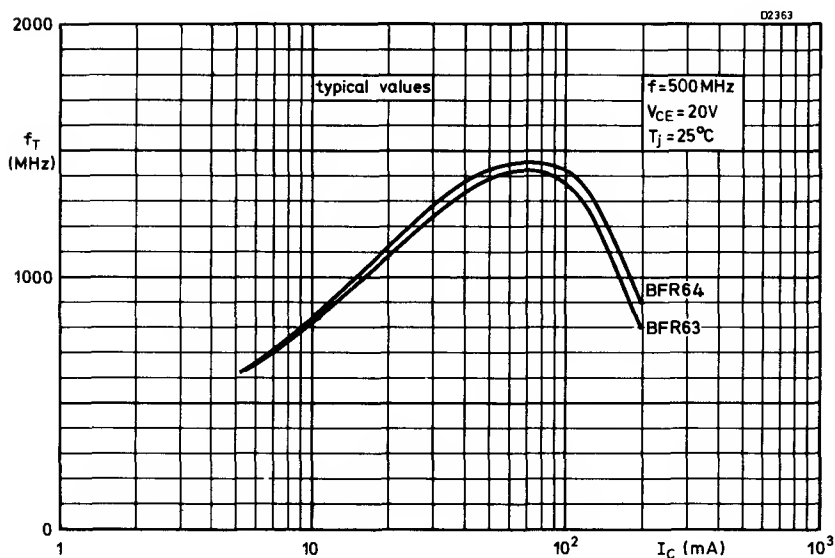
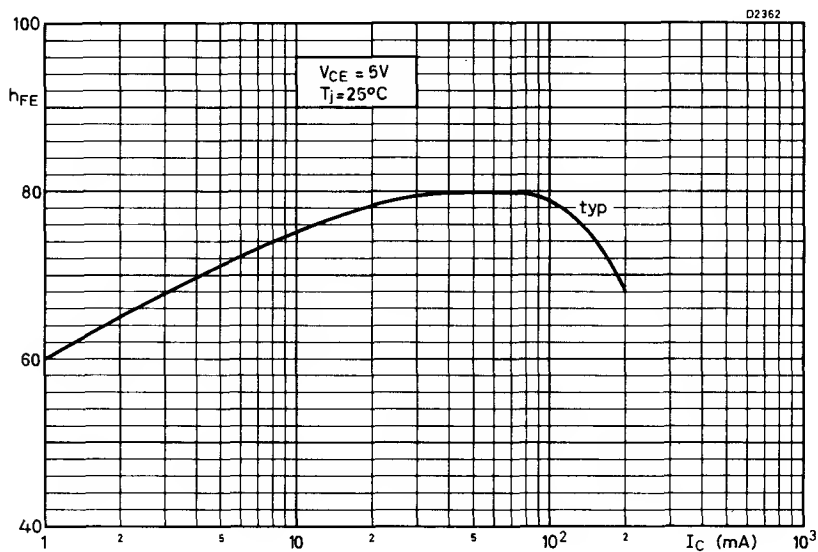


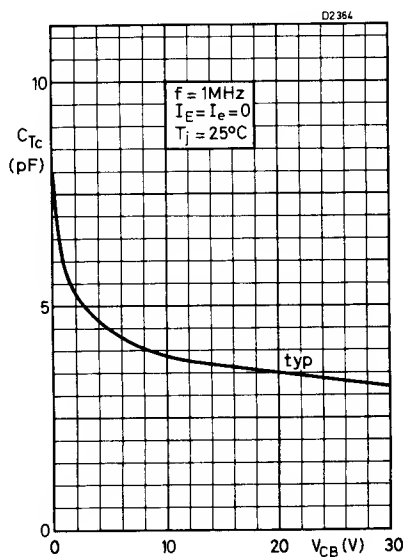
Safe Operating Areas with the transistor forward biased

I Region of permissible d.c. operation

II Permissible extension for repetitive pulsed operation; $f > 1\text{MHz}$

III Repetitive pulsed operation in this region is allowed, provided $R_{BE} < 10\Omega$ and $f > 1\text{MHz}$





N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

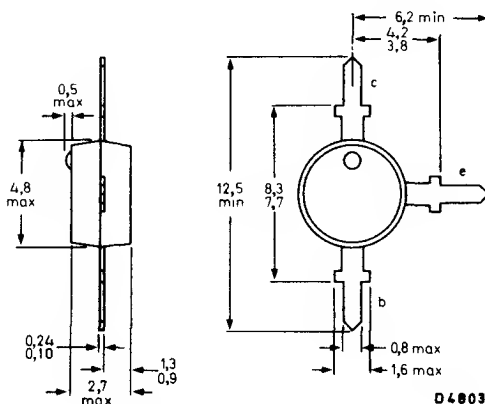
BFR90

Silicon planar epitaxial n-p-n transistor in a plastic T-package. It is primarily intended for use in u.h.f. and microwave amplifiers such as aerial amplifiers, radar systems, oscilloscopes, spectrum analysers etc. The transistor features very low intermodulation distortion, high power gain and excellent wideband properties combined with very high transition frequency and a low noise figure.

QUICK REFERENCE DATA

V_{CBO} max.	20	V
V_{CEO} max.	15	V
I_C max.	25	mA
P_{tot} max. ($T_{amb} \leq 60^\circ\text{C}$)	180	mW
T_J max.	150	$^\circ\text{C}$
f_T typ. ($I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $f = 500\text{MHz}$)	5.0	GHz
$-C_{re}$ typ. ($I_C = 2\text{mA}$, $V_{CE} = 10\text{V}$, $f = 1\text{MHz}$)	0.4	pF
N typ. ($I_C = 2\text{mA}$, $V_{CE} = 10\text{V}$, $f = 500\text{MHz}$)	2.4	dB
G_{UM} typ. ($I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $f = 500\text{MHz}$)	19.5	dB
d_{im} typ. ($I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $R_L = 75\Omega$ $V_o = 150\text{mV}$, $f_{(p+q-r)} = 493.25\text{MHz}$)	-60	dB

OUTLINE AND DIMENSIONS



All dimensions in mm

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	20	V
V_{CEO} max.	15	V
V_{EBO} max.	2.0	V
I_C max.	25	mA
P_{tot} max. ($T_{amb} \leq 60^\circ\text{C}$)	180	mW

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
T_j max.	150	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	in free air, mounted on a glass-fibre print of $40 \times 25 \times 1\text{mm}$ (see fig. 1)	0.5	$^\circ\text{C/mW}$
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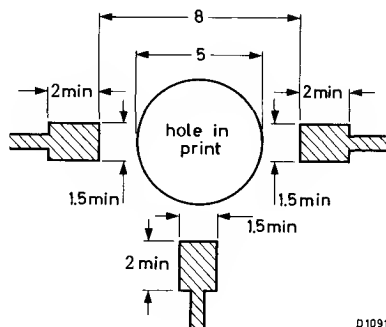


Fig. 1

Requirements for a glass-fibre print

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFR90

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0, V_{\text{CB}} = 10\text{V}$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_C = 14\text{mA}, V_{\text{CE}} = 10\text{V}$	25	50	-	
f_{T}	*Transition frequency $I_C = 14\text{mA}, V_{\text{CE}} = 10\text{V}, f = 500\text{MHz}$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_c = 0, V_{\text{CB}} = 10\text{V}, f = 1.0\text{MHz}$	-	0.5	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0, V_{\text{EB}} = 0.5\text{V}, f = 1.0\text{MHz}$	-	0.8	-	pF
$-C_{\text{re}}$	Feedback capacitance at $T_{\text{amb}} = 25^\circ\text{C}$ $I_C = 2.0\text{mA}, V_{\text{CE}} = 10\text{V}, f = 1.0\text{MHz}$	-	0.4	-	pF
N	Noise figure at optimum source impedance and $T_{\text{amb}} = 25^\circ\text{C}$ $I_C = 2.0\text{mA}, V_{\text{CE}} = 10\text{V}, f = 500\text{MHz}$	-	2.4	-	dB
G_{UM}	Maximum unilateralized stage gain at $T_{\text{amb}} = 25^\circ\text{C}$ Calculated from s-parameters: $G_{\text{UM}} = 10 \log \frac{ s_{\text{fe}} ^2}{(1 - s_{\text{ic}} ^2)(1 - s_{\text{oe}} ^2)}$				
	$I_C = 14\text{mA}, V_{\text{CE}} = 10\text{V}, f = 500\text{MHz}$	-	19.5	-	dB

*Measured under pulsed conditions.

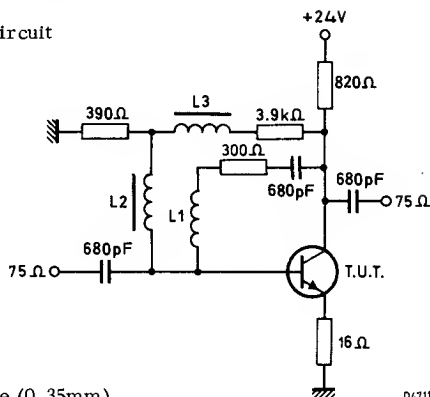
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Min. Typ. Max.

 d_{im} Intermodulation distortion at $T_{amb} = 25^{\circ}C$ $I_C = 14mA, V_{CE} = 10V, R_L = 75\Omega, V.S.W.R < 2$ $V_p = V_o = 150mV$ at $f_p = 495.25MHz$ $V_q = V_o - 6dB$ at $f_q = 503.25MHz$ $V_r = V_o - 6dB$ at $f_r = 505.25MHz$ measured at $f_{(p+q-r)} = 493.25MHz$

- -60 - dB

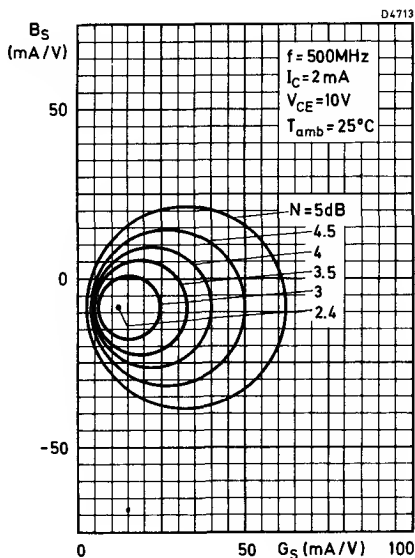
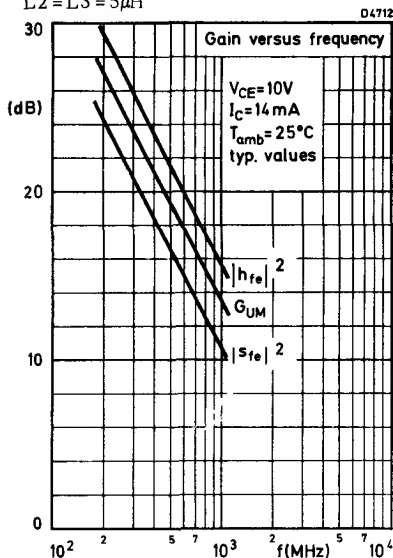
Intermodulation test circuit



D4711

L1 = 4 turns of Cu wire (0.35mm),
winding pitch 1mm, int. dia. 4mm

L2 = L3 = 5μH

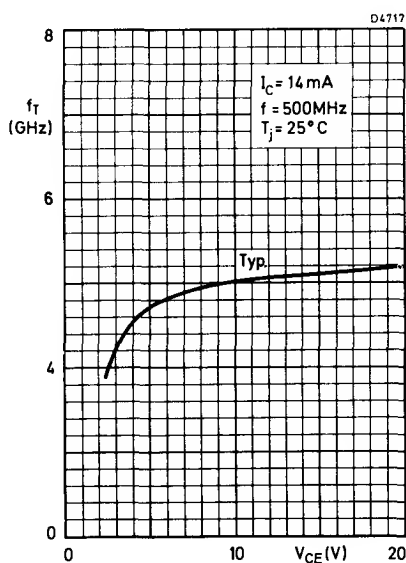
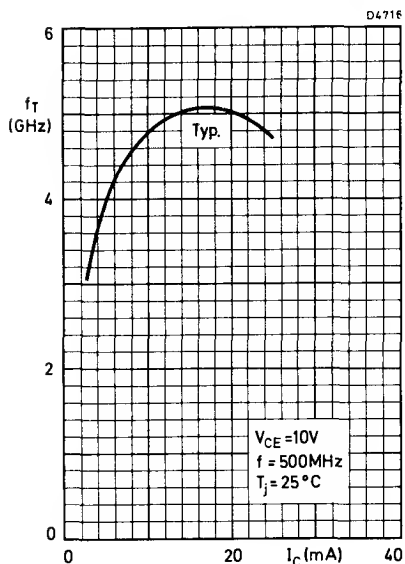
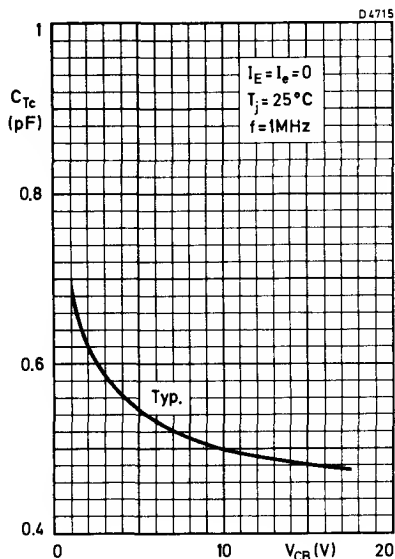
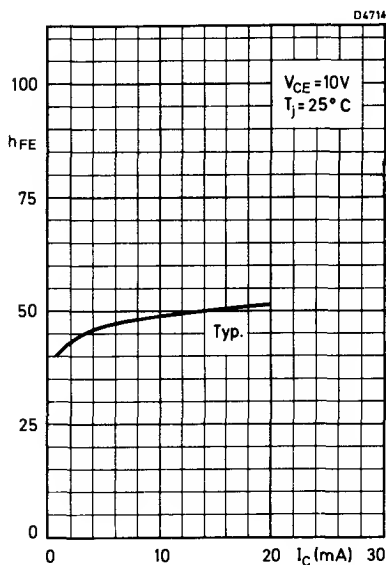


Constant noise figure circles

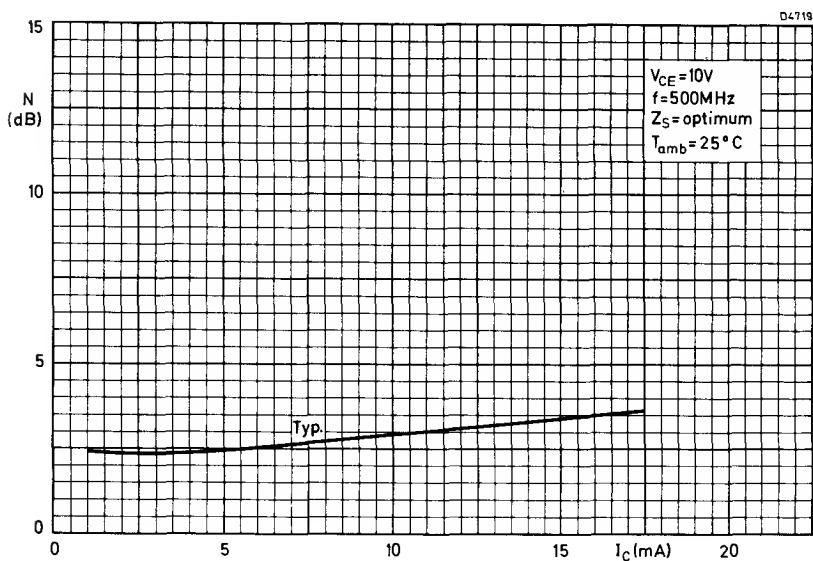
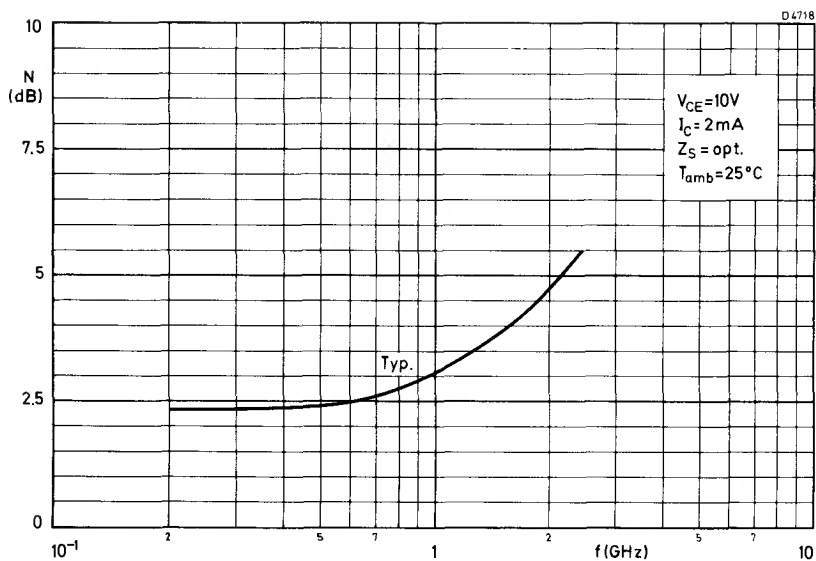
Mullard

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFR90



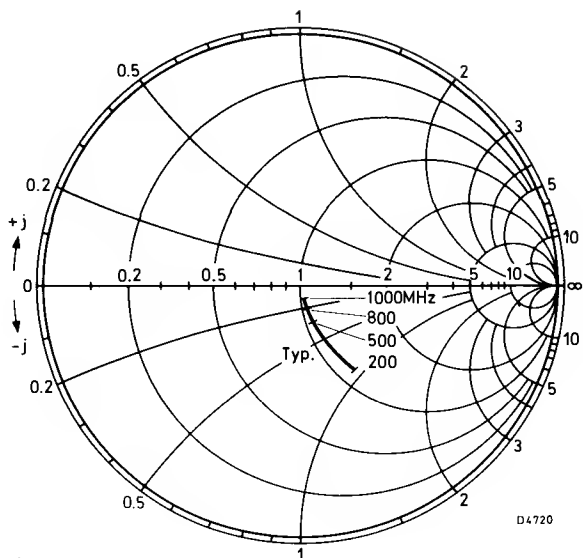
Mullard



N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

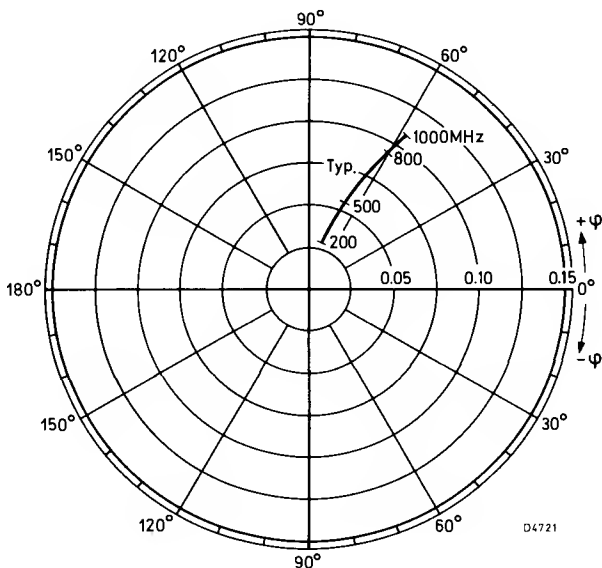
BFR90

$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



Input impedance derived from
input reflection coefficient s_{ie}
coordinates in ohm $\times 50$

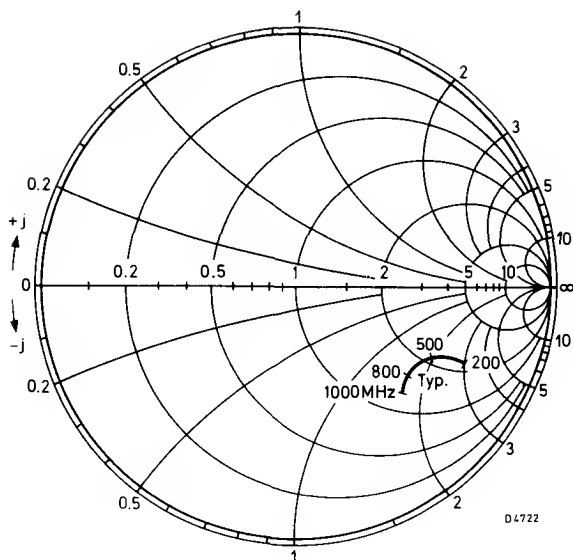
$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



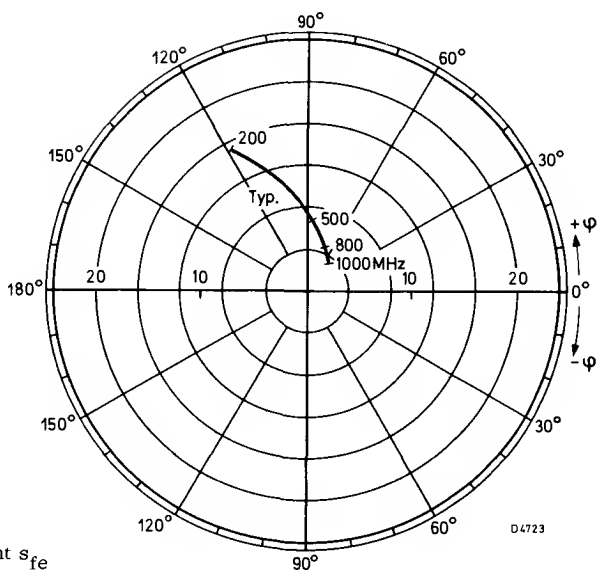
Feedback coefficient s_{re}

Mullard

$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

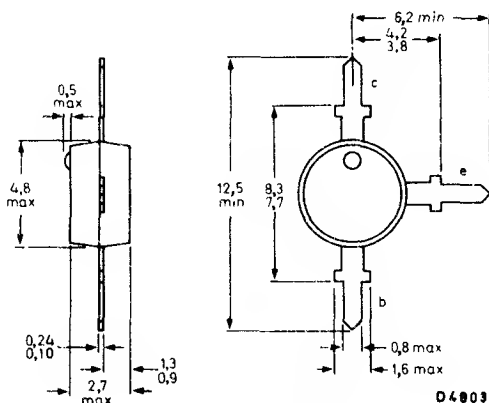
BFR91

Silicon planar epitaxial n-p-n transistor in a plastic T-package. It is primarily intended for use in u.h.f. and microwave amplifiers such as aerial amplifiers, radar systems, oscilloscopes, spectrum analysers etc. The transistor features very low intermodulation distortion, high power gain and excellent wideband properties combined with very high transition frequency and a low noise figure.

QUICK REFERENCE DATA

V_{CBO} max.	15	V
V_{CEO} max.	12	V
I_C max.	35	mA
P_{tot} max. ($T_{amb} \leq 60^\circ\text{C}$)	180	mW
T_j max.	150	$^\circ\text{C}$
f_T typ. ($I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$)	5.0	GHz
C_{re} typ. ($I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$, $f = 1\text{MHz}$)	0.8	pF
N typ. ($I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$)	1.9	dB
G_{UM} typ. ($I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$)	16.5	dB
d_{im} typ. ($I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $R_L = 75\Omega$)		
$V_o = 300\text{mV}$, $f_{(p+q-r)} = 493.25\text{MHz}$	-60	dB

OUTLINE AND DIMENSIONS



All dimensions in mm

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	15	V
V_{CEO} max.	12	V
V_{EBO} max.	2.0	V
I_C max.	35	mA
P_{tot} max. ($T_{amb} \leq 60^\circ C$)	180	mW

Temperature

T_{stg}	-65 to +150	$^\circ C$
T_j max.	150	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	in free air, mounted on a glass-fibre print of $40 \times 25 \times 1$ mm (see fig. 1)	0.5	$^\circ C/mW$
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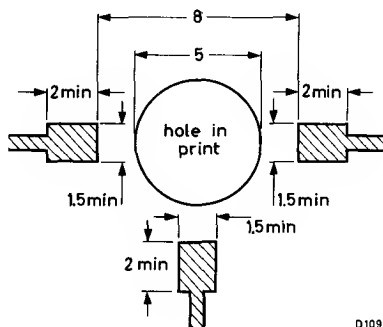


Fig. 1

Requirements for a glass-fibre print

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

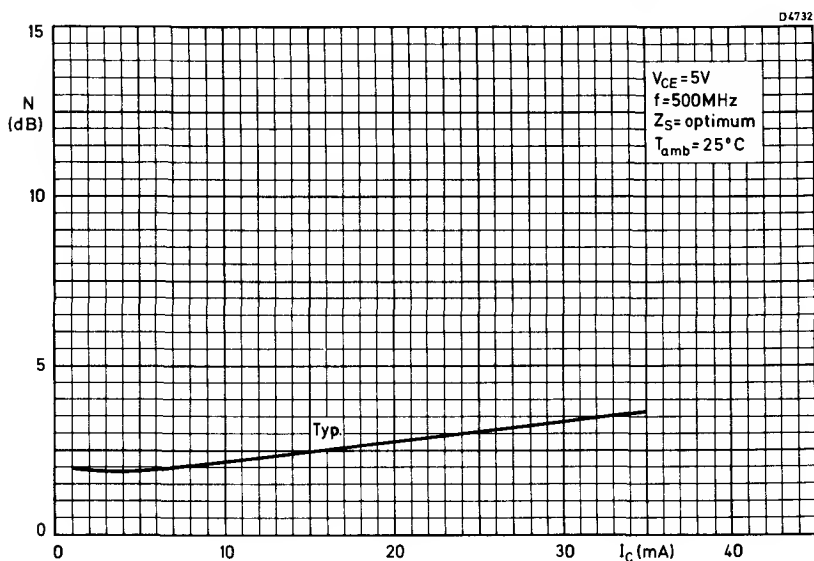
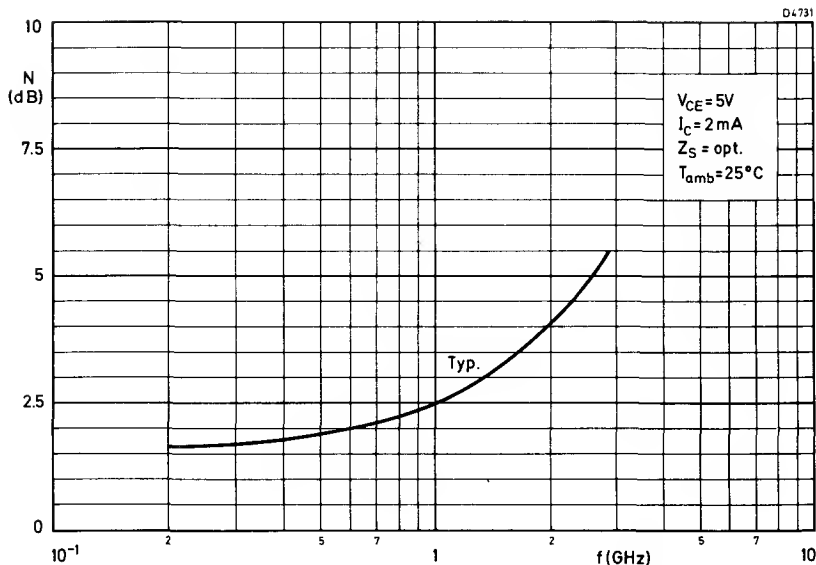
BFR91

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_{\text{E}} = 0, V_{\text{CB}} = 5.0\text{V}$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_{\text{C}} = 30\text{mA}, V_{\text{CE}} = 5.0\text{V}$	25	50	-	
f_{T}	*Transition frequency $I_{\text{C}} = 30\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 500\text{MHz}$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_{\text{E}} = I_{\text{e}} = 0, V_{\text{CB}} = 10\text{V}, f = 1.0\text{MHz}$	-	0.7	-	pF
C_{Te}	Emitter capacitance $I_{\text{C}} = I_{\text{c}} = 0, V_{\text{EB}} = 0.5\text{V}, f = 1.0\text{MHz}$	-	1.8	-	pF
C_{re}	Feedback capacitance at $T_{\text{amb}} = 25^{\circ}\text{C}$ $I_{\text{C}} = 2.0\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 1.0\text{MHz}$	-	0.8	-	pF
N	Noise figure at optimum source impedance and $T_{\text{amb}} = 25^{\circ}\text{C}$ $I_{\text{C}} = 2.0\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 500\text{MHz}$	-	1.9	-	dB
G_{UM}	Maximum unilateralized stage gain at $T_{\text{amb}} = 25^{\circ}\text{C}$ Calculated from s-parameters: $G_{\text{UM}} = 10 \log \frac{ s_{\text{fe}} ^2}{(1 - s_{\text{ie}} ^2)(1 - s_{\text{oe}} ^2)}$				
	$I_{\text{C}} = 30\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 500\text{MHz}$	-	16.5	-	dB

*Measured under pulsed conditions.

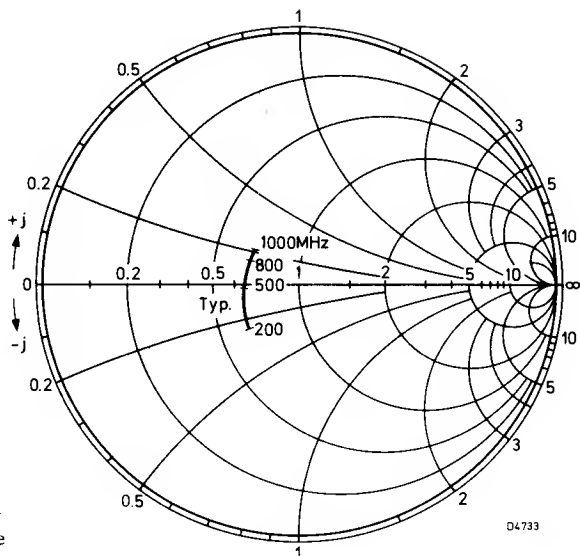
Mullard



N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

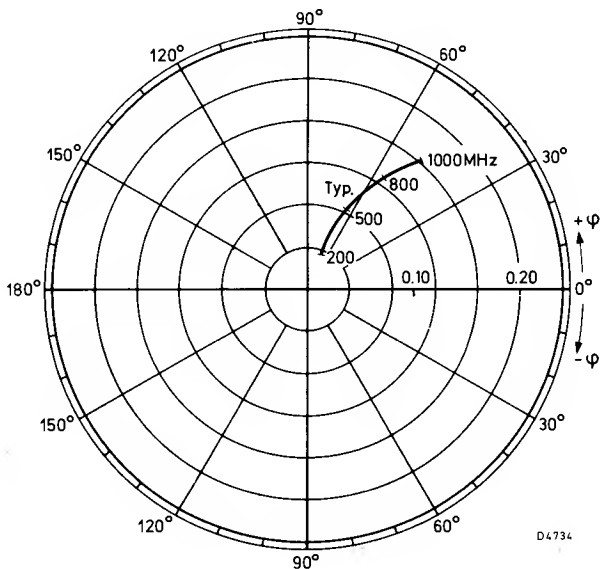
BFR91

$V_{CE} = 5V$
 $I_C = 30mA$
 $T_{amb} = 25^{\circ}C$



Input impedance derived from
input reflection coefficient s_{ie}
coordinates in ohm $\times 50$

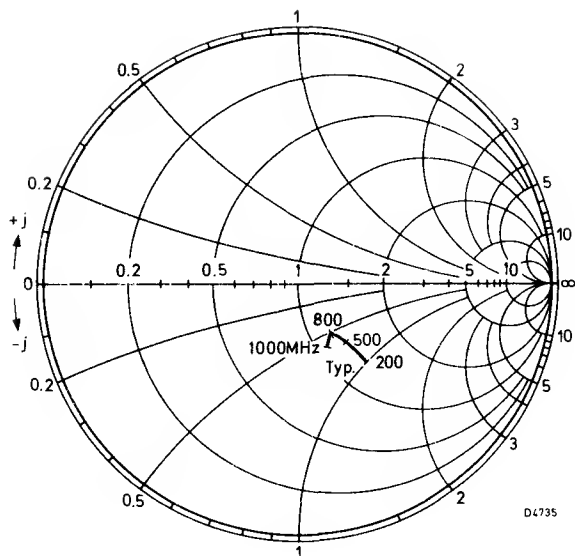
$V_{CE} = 5V$
 $I_C = 30mA$
 $T_{amb} = 25^{\circ}C$



Feedback coefficient s_{re}

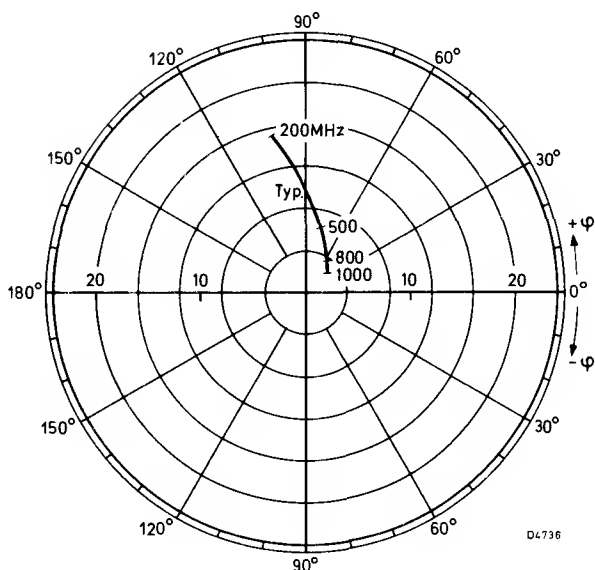
Mullard

$V_{CE} = 5V$
 $I_C = 30mA$
 $T_{amb} = 25^{\circ}C$



Output impedance derived from
 output reflection coefficient s_{oe}
 coordinates in $ohm \times 50$

$V_{CE} = 5V$
 $I_C = 30mA$
 $T_{amb} = 25^{\circ}C$



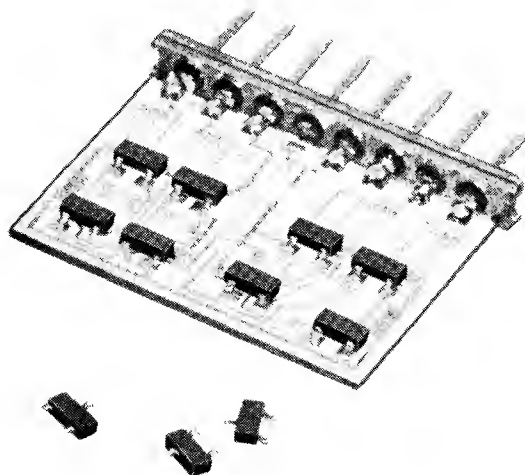
Forward transfer coefficient s_{fe}

Silicon n-p-n planar epitaxial transistor in a micro-miniature plastic envelope. It is primarily intended for use in u.h.f. and microwave amplifiers in thick and thin film circuits, such as in aerial amplifiers, radar systems, oscilloscopes, spectrum analysers, etc.

QUICK REFERENCE DATA

V_{CBO} max.	20	V
V_{CEO} max.	15	V
I_C max.	25	mA
P_{tot} max. ($T_{amb} \leq 60^\circ\text{C}$)	180	mW
T_j max.	150	$^\circ\text{C}$
f_T typ. ($I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $f = 500\text{MHz}$)	5.0	GHz
$-C_{re}$ typ. ($I_C = 2\text{mA}$, $V_{CE} = 10\text{V}$, $f = 1\text{MHz}$)	0.7	pF
N typ. ($I_C = 2\text{mA}$, $V_{CE} = 10\text{V}$, $f = 500\text{MHz}$)	2.4	dB
G_{UM} typ. ($I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $f = 500\text{MHz}$)	18	dB
d_{im} typ. ($I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $R_L = 75\Omega$, $V_o = 150\text{mV}$, $f(p+q-r) = 493.25\text{MHz}$, see also page 4)	-60	dB

OUTLINE AND DIMENSIONS - For details see page 2

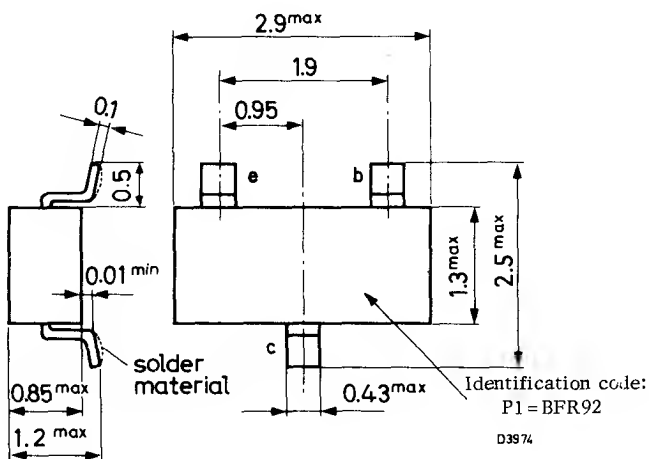


$2\frac{1}{2} \times$ actual size

OUTLINE AND DIMENSIONS

All dimensions in millimetres

Plan view from above



RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	20	V
V_{CEO} max.	15	V
V_{EBO} max.	2.0	V
I_C max.	25	mA
P_{tot} max., $T_{amb} \leq 60^{\circ}\text{C}$, mounted on a ceramic substrate of $15 \times 10 \times 0.5\text{mm}$	180	mW

Temperature

T_{stg}	-65 to +150	$^{\circ}\text{C}$
$T_{i \text{ max.}}$	150	$^{\circ}\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $15 \times 10 \times 0.5\text{mm}$	0.50 $^{\circ}\text{C}/\text{mW}$
-----------------	--	-----------------------------------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_{\text{E}} = 0, V_{\text{CB}} = 10\text{V}$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_{\text{C}} = 14\text{mA}, V_{\text{CE}} = 10\text{V}$	25	50	-	
f_{T}	*Transition frequency $I_{\text{C}} = 14\text{mA}, V_{\text{CE}} = 10\text{V}, f = 500\text{MHz}$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_{\text{E}} = I_{\text{e}} = 0, V_{\text{CB}} = 10\text{V}, f = 1.0\text{MHz}$	-	0.75	-	pF
C_{Te}	Emitter capacitance $I_{\text{C}} = I_{\text{c}} = 0, V_{\text{EB}} = 0.5\text{V}, f = 1.0\text{MHz}$	-	0.8	-	pF
$-C_{\text{re}}$	Feedback capacitance, $T_{\text{amb}} = 25^\circ\text{C}$ $I_{\text{C}} = 2.0\text{mA}, V_{\text{CE}} = 10\text{V}, f = 1.0\text{MHz}$	-	0.7	-	pF
N	†Noise figure at optimum source impedance, $T_{\text{amb}} = 25^\circ\text{C}$ $I_{\text{C}} = 2.0\text{mA}, V_{\text{CE}} = 10\text{V}, f = 500\text{MHz}$	-	2.4	-	dB
G_{UM}	Max. unilateralized stage gain at $T_{\text{amb}} = 25^\circ\text{C}$, calculated from s-parameters: $G_{\text{UM}} = 10 \log \frac{ s_{\text{fe}} ^2}{(1 - s_{\text{ie}} ^2)(1 - s_{\text{oe}} ^2)}$ $I_{\text{C}} = 14\text{mA}, V_{\text{CE}} = 10\text{V}, f = 500\text{MHz}$	-	18	-	dB

*Measured under pulsed conditions.

†Crystal mounted in a BFR90 envelope.

d_{lm} Intermodulation distortion at $T_{amb} = 25^{\circ}\text{C}$ $I_C = 14\text{mA}$, $V_{CE} = 10\text{V}$, $R_L = 75\Omega$, V.S.W.R. < 2

Min.

Typ.

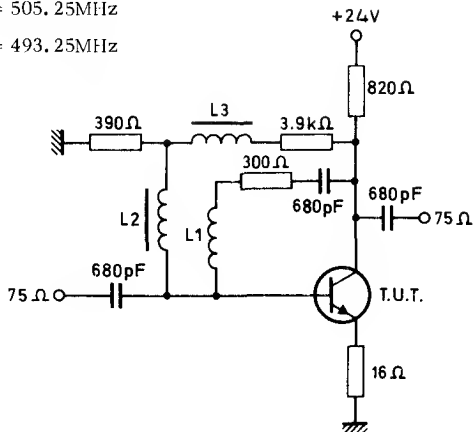
Max.

-60

dB

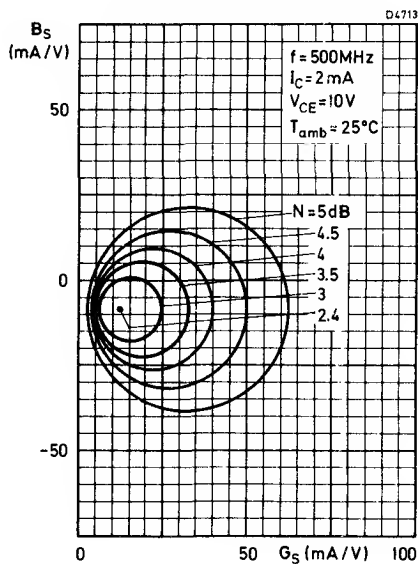
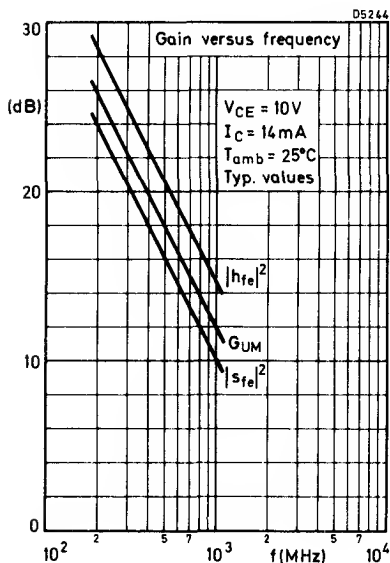
 $V_p = V_o = 150\text{mV}$ at $f_p = 495.25\text{MHz}$ $V_q = V_o - 6\text{dB}$ at $f_q = 503.25\text{MHz}$ $V_r = V_o - 6\text{dB}$ at $f_r = 505.25\text{MHz}$ Measured at $f_{(p+q-r)} = 493.25\text{MHz}$

Intermodulation test circuit:



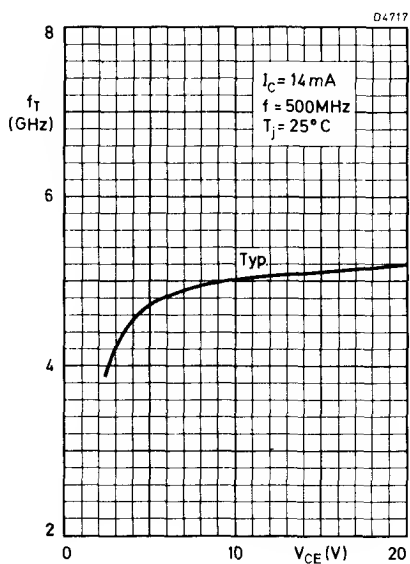
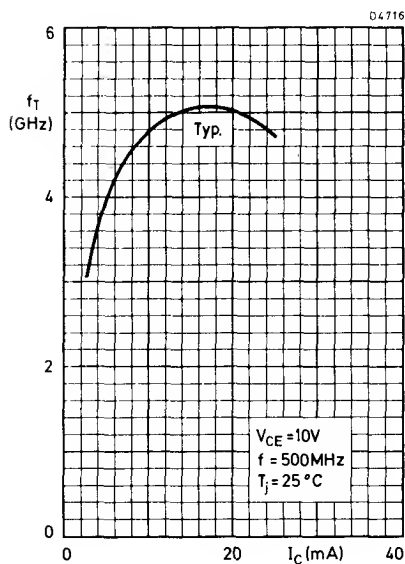
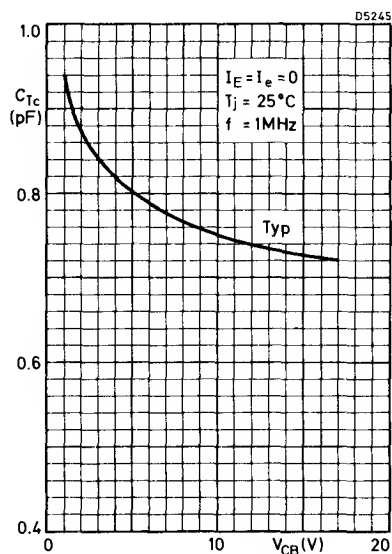
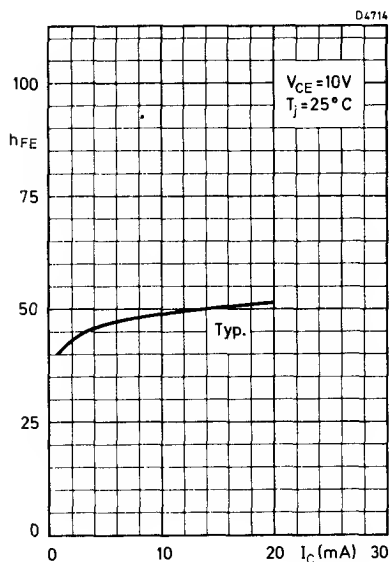
$L1 = 4$ turns of Cu wire (0.35mm),
winding pitch 1mm, int. dia. 4mm
 $L2 = L3 = 5\mu\text{H}$

Circles of constant noise figure

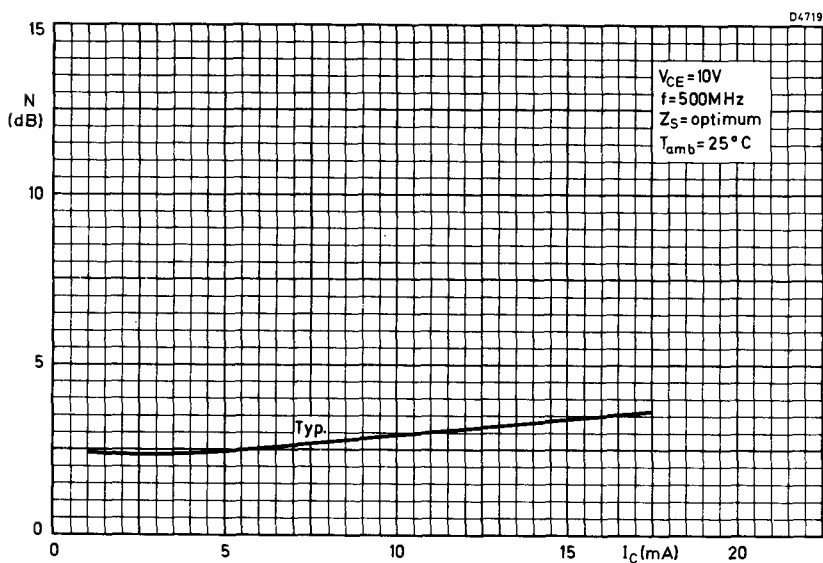
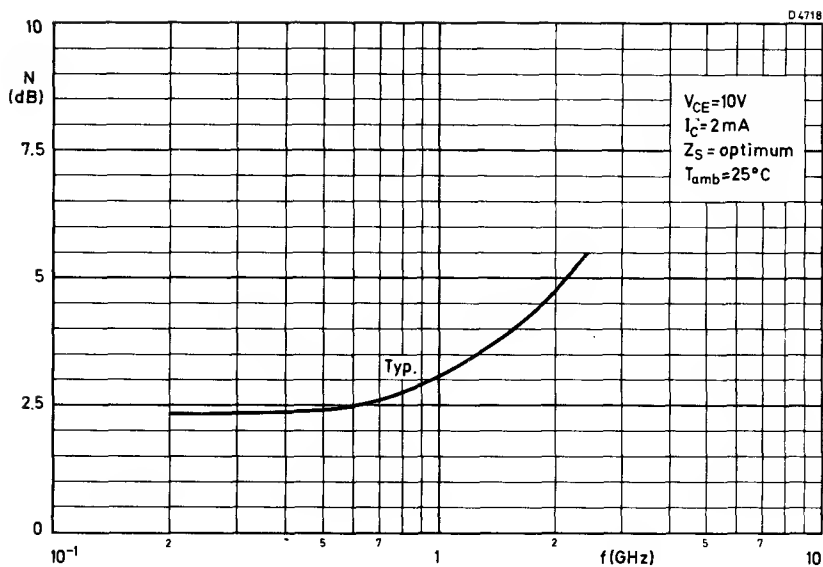


**μ min. N-P-N SILICON PLANAR
EPITAXIAL U.H.F. TRANSISTOR**

BFR92



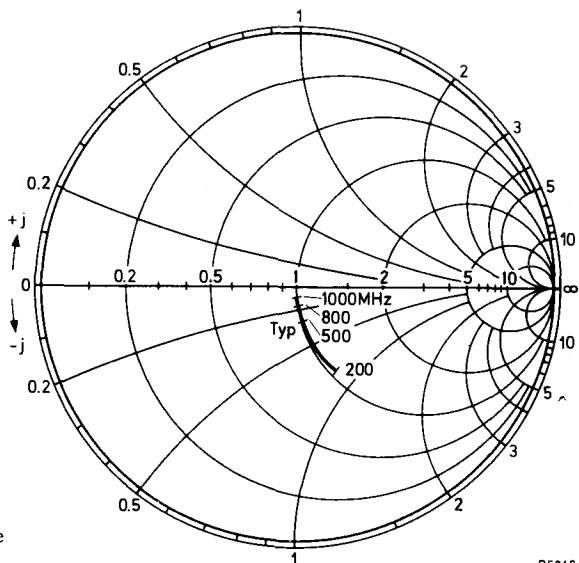
Mullard



**μ min. N-P-N SILICON PLANAR
EPITAXIAL U.H.F. TRANSISTOR**

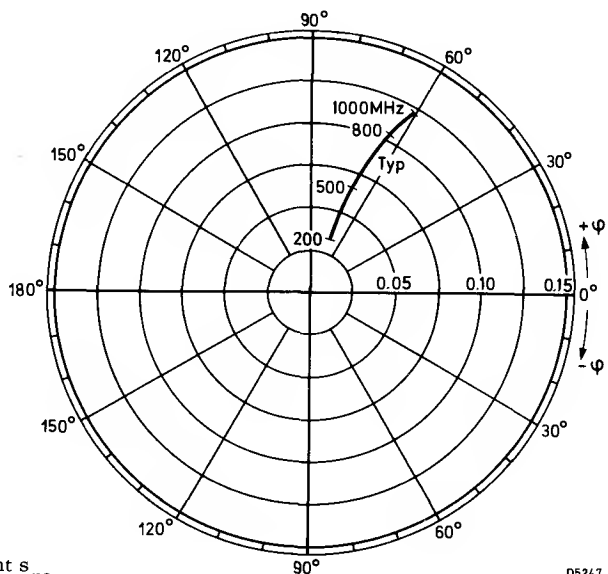
BFR92

$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



Input impedance derived from
 input reflection coefficient s_{ie}
 coordinates in ohm $\times 50$

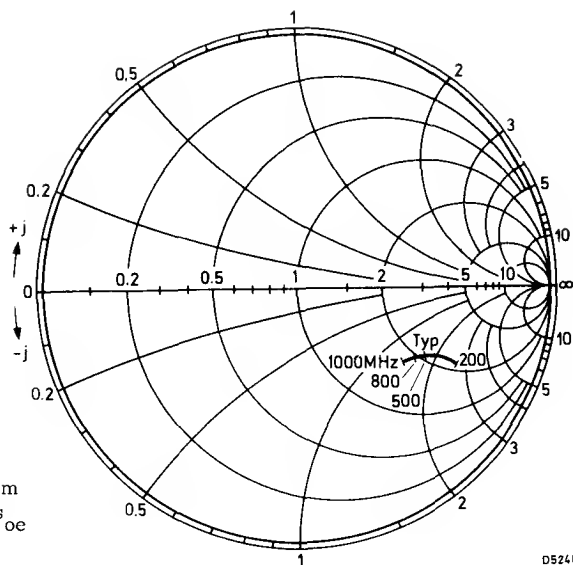
$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



Reverse transfer coefficient s_{re}

Mullard

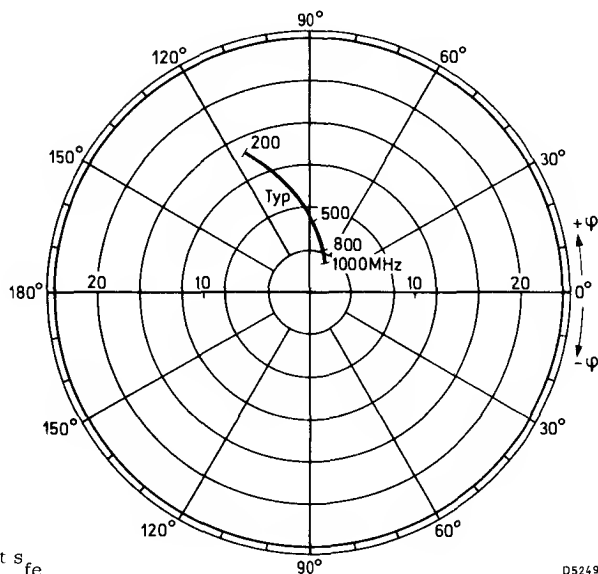
$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



D5248

Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm $\times 50$

$V_{CE} = 10V$
 $I_C = 14mA$
 $T_{amb} = 25^{\circ}C$



D5249

Forward transfer coefficient s_{fe}

μmin. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFR93

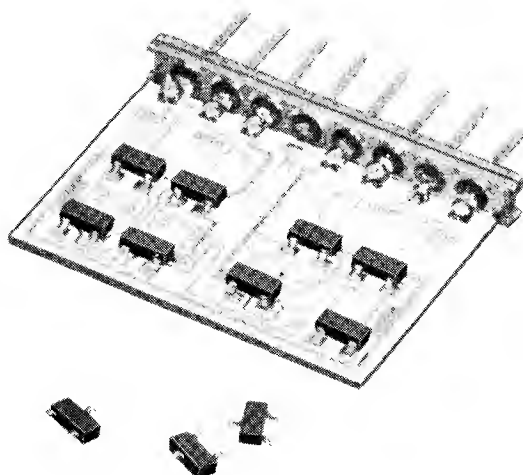
Silicon n-p-n planar epitaxial transistor in a micro-miniature plastic envelope. It is primarily intended for use in u.h.f. and microwave amplifiers in thick and thin film circuits, such as in aerial amplifiers, radar systems, oscilloscopes, spectrum analysers, etc.

QUICK REFERENCE DATA

V_{CBO} max.	15	V
V_{CEO} max.	12	V
I_C max.	35	mA
P_{tot} max. ($T_{amb} \leq 60^\circ\text{C}$)	180	mW
T_j max.	150	$^\circ\text{C}$
f_T typ. ($I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$)	5.0	GHz
$-C_{re}$ typ. ($I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$, $f = 1\text{MHz}$)	0.8	pF
N typ. ($I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$)	1.9	dB
G_{UM} typ. ($I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$)	16.5	dB
d_{im} typ. ($I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $R_L = 75\Omega$, $V_o = 300\text{mV}$ $f_{(p+q-r)} = 493.25\text{MHz}$, see also page 4)	-60	dB

OUTLINE AND DIMENSIONS

For details see page 2



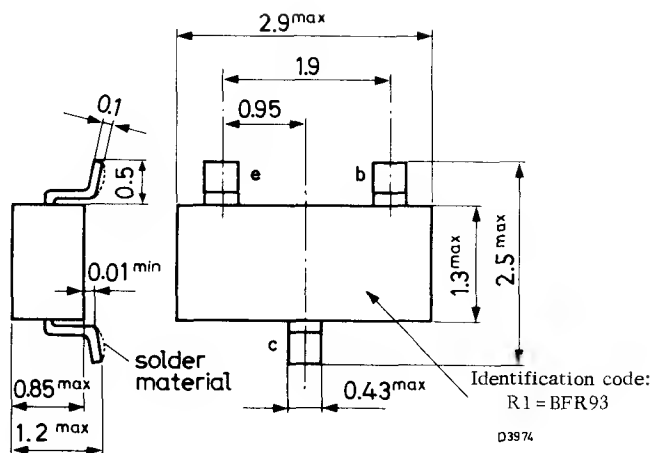
$2\frac{1}{2} \times$ actual size

Mullard

OUTLINE AND DIMENSIONS

All dimensions in millimetres

Plan view from above



RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	15	V
V_{CEO} max.	12	V
V_{EBO} max.	2.0	V
I_C max.	35	mA
P_{tot} max., $T_{amb} \leq 60^\circ\text{C}$, mounted on a ceramic substrate of $15 \times 10 \times 0.5\text{mm}$	180	mW

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
T_j max.	150	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $15 \times 10 \times 0.5\text{mm}$	0.50 $^\circ\text{C/mW}$
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μ min. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFR93

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0, V_{\text{CB}} = 10\text{V}$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_C = 30\text{mA}, V_{\text{CE}} = 5\text{V}$	25	50	-	
f_{T}	*Transition frequency $I_C = 30\text{mA}, V_{\text{CE}} = 5\text{V}, f = 500\text{MHz}$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_c = 0, V_{\text{CB}} = 10\text{V}, f = 1.0\text{MHz}$	-	0.7	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0, V_{\text{EB}} = 0.5\text{V}, f = 1.0\text{MHz}$	-	1.8	-	pF
$-C_{\text{re}}$	Feedback capacitance, $T_{\text{amb}} = 25^\circ\text{C}$ $I_C = 2.0\text{mA}, V_{\text{CE}} = 5\text{V}, f = 1.0\text{MHz}$	-	0.8	-	pF
N	†Noise figure at optimum source impedance, $T_{\text{amb}} = 25^\circ\text{C}$ $I_C = 2.0\text{mA}, V_{\text{CE}} = 5\text{V}, f = 500\text{MHz}$	-	1.9	-	dB
G_{UM}	Max. unilateralized stage gain at $T_{\text{amb}} = 25^\circ\text{C}$, calculated from s-parameters: $G_{\text{UM}} = 10 \log \frac{ s_{\text{fe}} ^2}{(1 - s_{\text{ie}} ^2)(1 - s_{\text{oe}} ^2)}$ $I_C = 30\text{mA}, V_{\text{CE}} = 5\text{V}, f = 500\text{MHz}$	-	16.5	-	dB

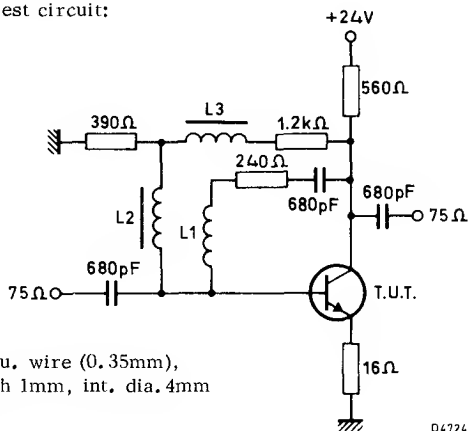
*Measured under pulsed conditions

†Crystal mounted in a BFR91 envelope

Mullard

d_{im} †Intermodulation distortion at $T_{amb} = 25^\circ\text{C}$ $I_C = 30\text{mA}$, $V_{CE} = 5\text{V}$, $R_L = 75\Omega$, V.S.W. R, ≤ 2 - -60 - dB $V_p = V_o = 300\text{mV}$ at $f_p = 495.25\text{MHz}$ $V_q = V_o - 6\text{dB}$ at $f_q = 503.25\text{MHz}$ $V_r = V_o - 6\text{dB}$ at $f_r = 505.25\text{MHz}$ Measured at $f_{(p+q-r)} = 493.25\text{MHz}$

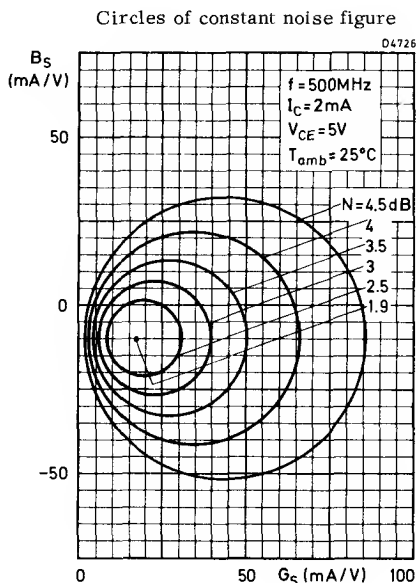
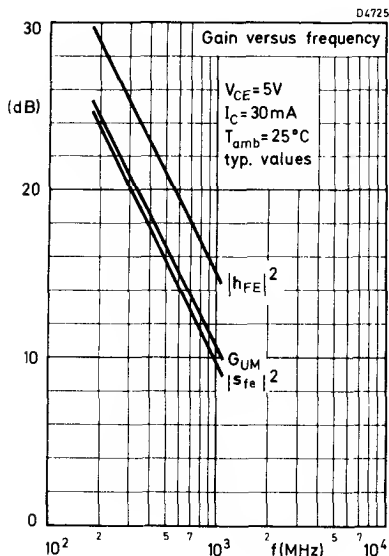
Intermodulation test circuit:

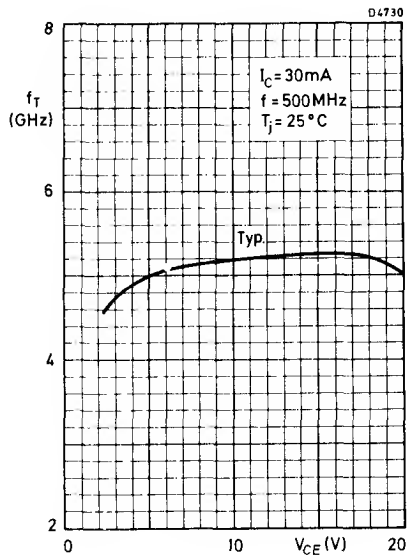
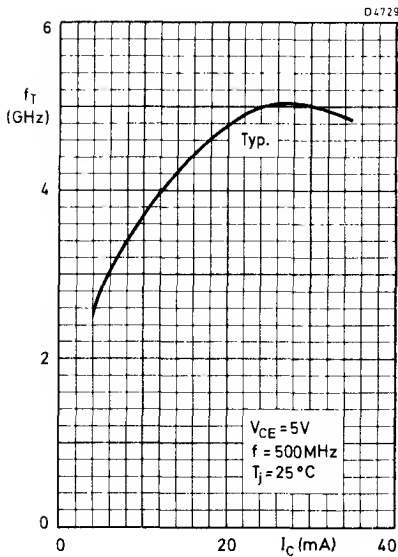
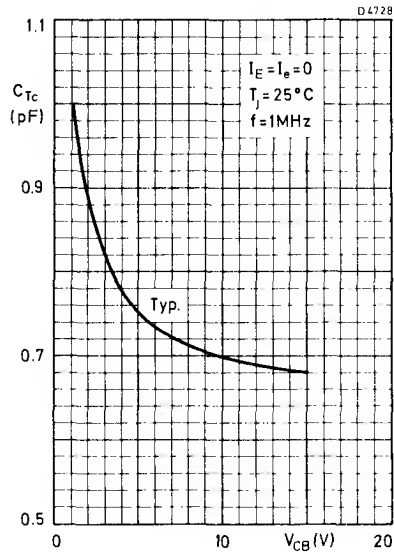
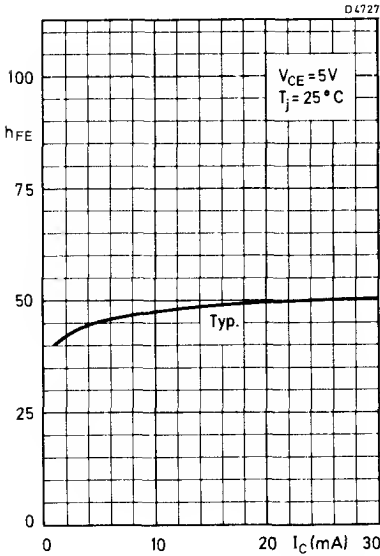


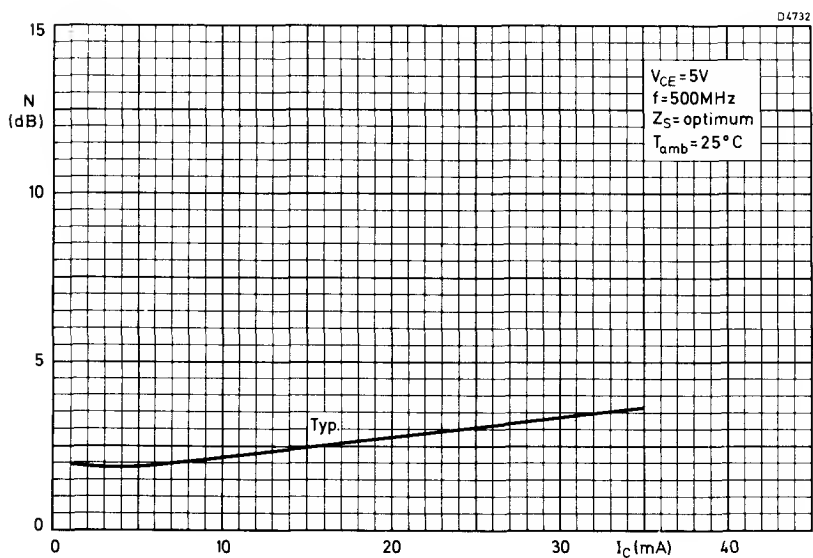
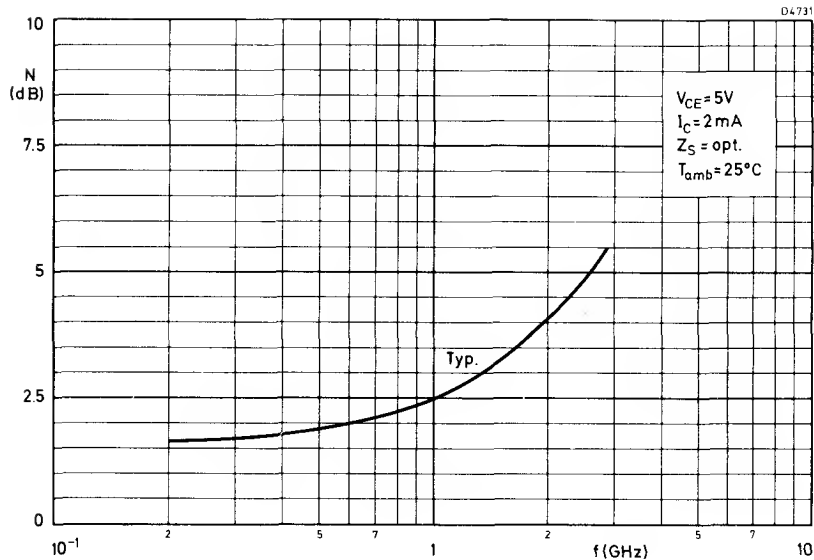
$L1 = 4$ turns of Cu. wire (0.35mm),
winding pitch 1mm, int. dia. 4mm

$L2 = L3 = 5\mu\text{H}$

†Crystal mounted in a BFR91 envelope



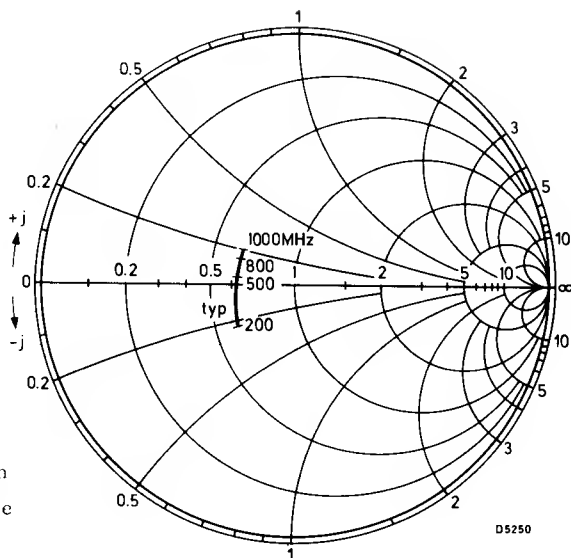




**μ min. N-P-N SILICON PLANAR
EPITAXIAL U.H.F. TRANSISTOR**

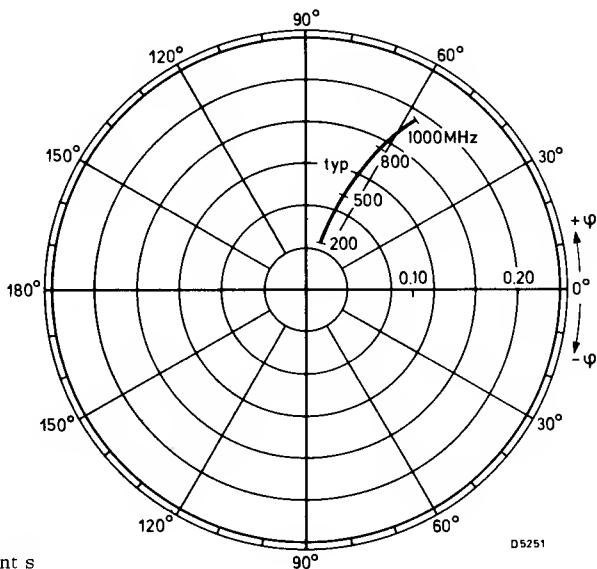
BFR93

$$\begin{aligned} V_{CE} &= 5V \\ I_C &= 30mA \\ T_{amb} &= 25^\circ C \end{aligned}$$



Input impedance derived from
input reflection coefficient s_{ic}
coordinates in ohm $\times 50$

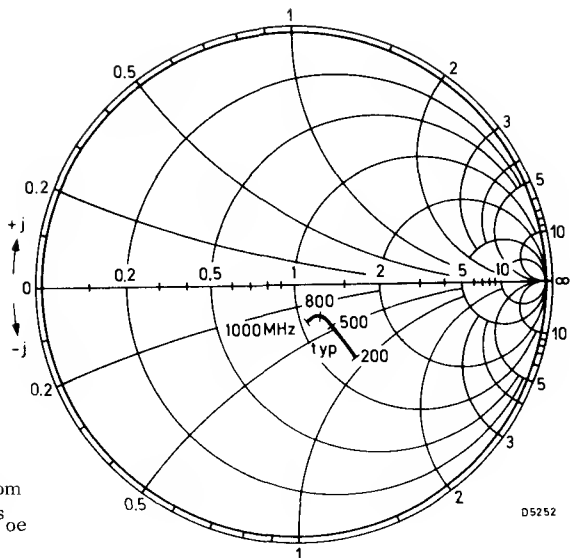
$$\begin{aligned} V_{CE} &= 5V \\ I_C &= 30mA \\ T_{amb} &= 25^\circ C \end{aligned}$$



Reverse transfer coefficient s_{re}

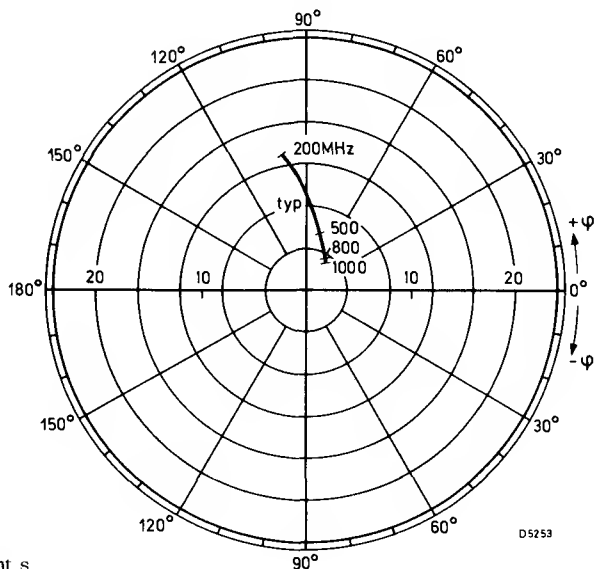
Mullard

$V_{CE} = 5V$
 $I_C = 30mA$
 $T_{amb} = 25^{\circ}C$



Output impedance derived from
output reflection coefficient s_{oe}
coordinates in ohm $\times 50$

$V_{CE} = 5V$
 $I_C = 30mA$
 $T_{amb} = 25^{\circ}C$



Forward transfer coefficient s_{fe}

BFS17R

QUICK REFERENCE DATA

V _{CBOM}	max.	25	V
V _{CEO}	max.	15	V
I _{CM}	max.	50	mA
P _{tot}	max., T _{amb} ≤ 25°C	200	mW
T _j	max.	150	°C
<hr/>			
h _{FE} at I _C = 2mA, V _{CE} = 1V		20-150	
f _T typ., I _C = 25mA, V _{CE} = 5V, f = 500MHz		1.3	GHz
<hr/>			
N typ., I _C = 2mA, V _{CE} = 5V, R _S = 50Ω, f = 500MHz		4.5	dB

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM}	max. (peak value)	25	V
V_{CEO}	max. ($I_C = 10\text{mA}$)	15	V
V_{EBO}	max.	2.5	V
I_C	max. (d. c.)	25	mA
I_{CM}	max. (peak value)	50	mA
P_{tot}	max. $T_{amb} \leq 25^{\circ}\text{C}$, mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	200	mW

Temperature

T_{stg}		-65 to +150	$^{\circ}\text{C}$
T_j	max.	150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	0.62	$^{\circ}\text{C/mW}$
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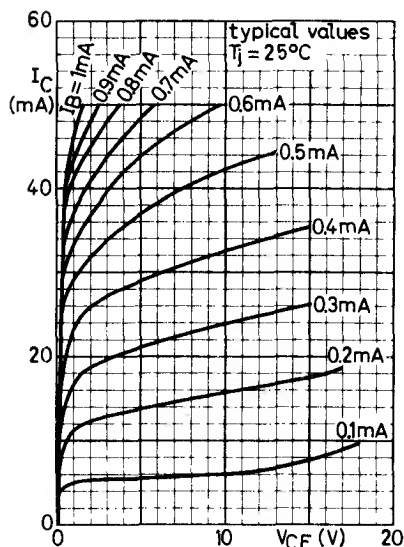
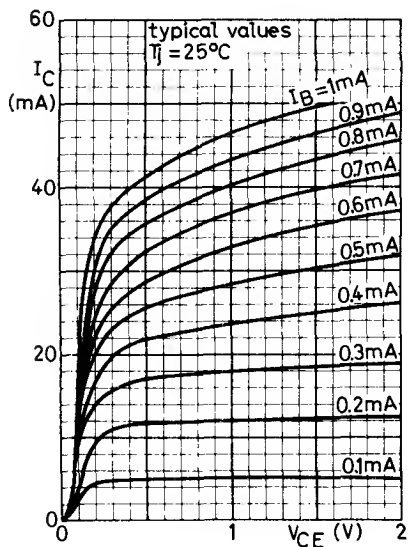
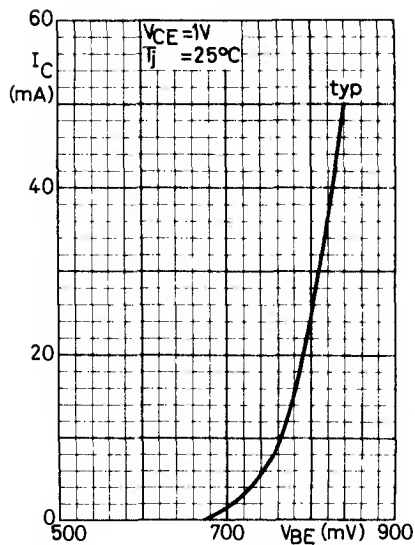
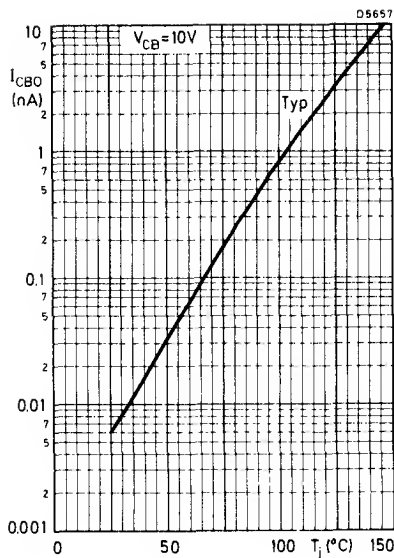
μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

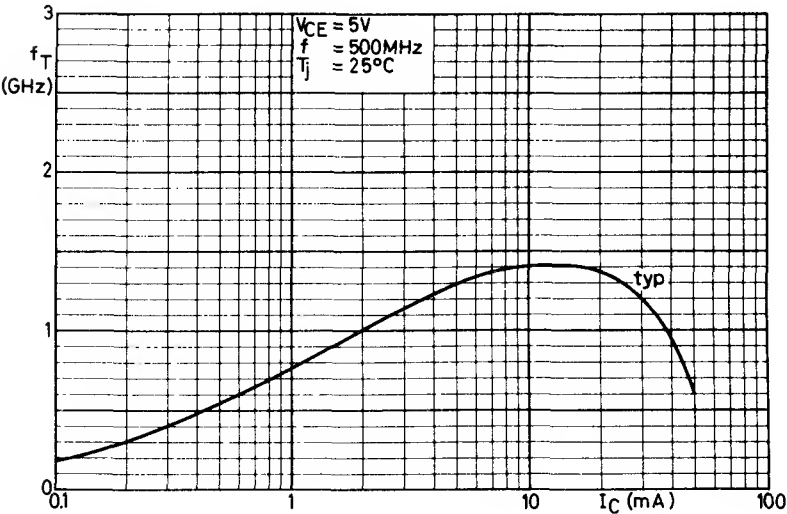
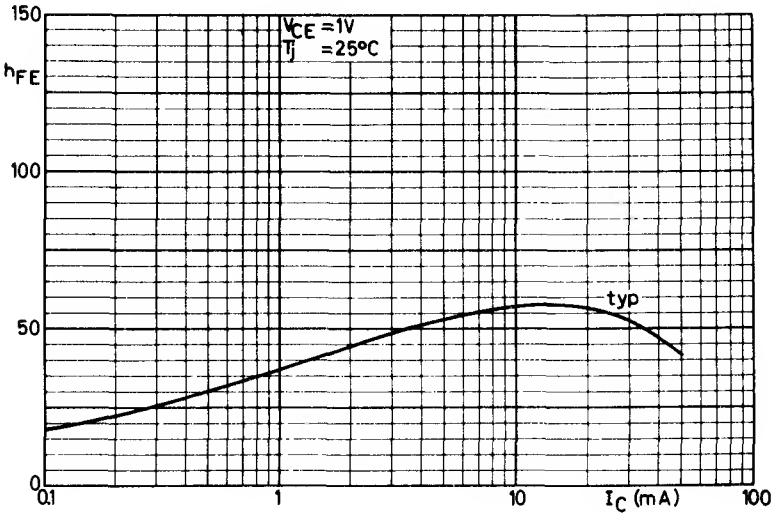
BFS17R

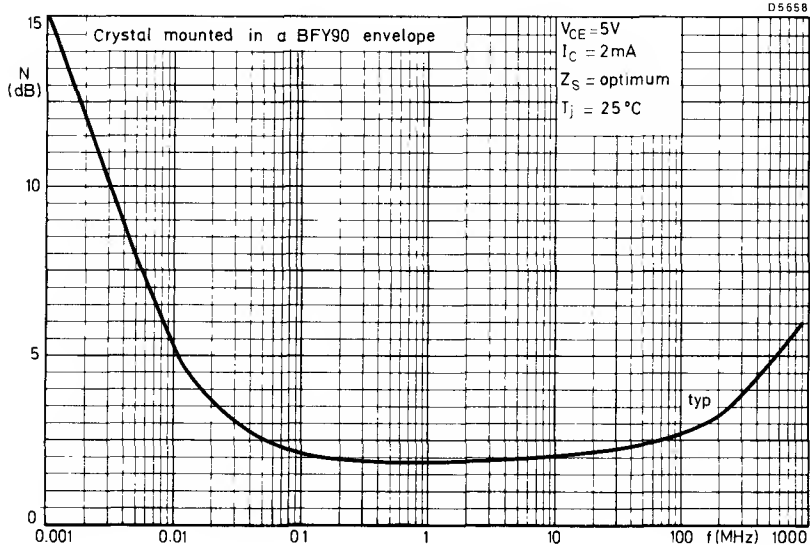
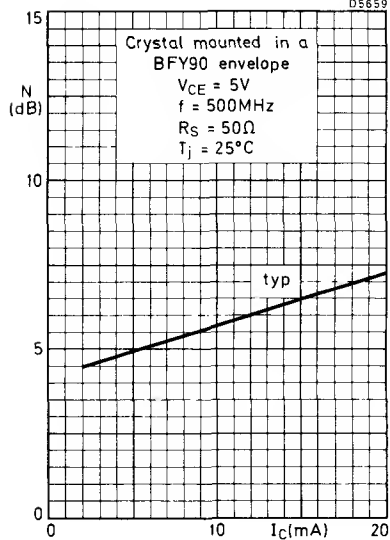
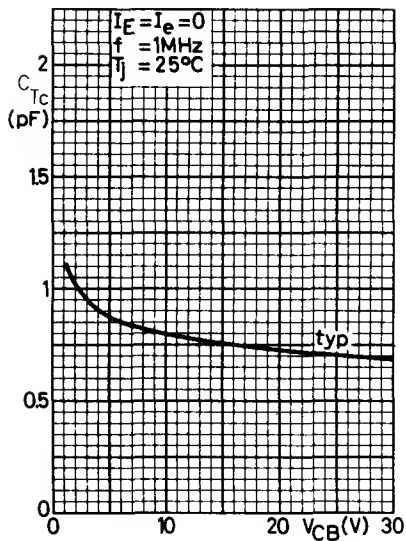
ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$I_E = 0, V_{\text{CB}} = 10\text{V}$	-	-	10	nA
h_{FE}	Static forward current transfer ratio				
	$I_E = 0, V_{\text{CB}} = 10\text{V}, T_j = 100^{\circ}\text{C}$	-	-	10	μA
h_{FE}	$I_C = 2.0\text{mA}, V_{\text{CE}} = 1.0\text{V}$	20	-	150	
	$I_C = 25\text{mA}, V_{\text{CE}} = 1.0\text{V}$	20	-	-	
f_{T}	Transition frequency				
	$I_C = 2.0\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 500\text{MHz}$	-	1.0	-	GHz
f_{T}	$I_C = 25\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 500\text{MHz}$	-	1.3	-	GHz
$-C_{\text{re}}$	Feedback capacitance				
	$I_C = 2.0\text{mA}, V_{\text{CE}} = 5.0\text{V}, f = 1.0\text{MHz}$	-	0.65	-	pF
C_{Tc}	Collector capacitance				
	$I_E = I_e = 0, V_{\text{CB}} = 10\text{V}, f = 1.0\text{MHz}$	-	-	1.5	pF
C_{Te}	Emitter capacitance				
	$I_C = I_c = 0, V_{\text{EB}} = 0.5\text{V}, f = 1.0\text{MHz}$	-	-	2.0	pF
*N	Noise figure				
	$I_C = 2.0\text{mA}, V_{\text{CE}} = 5.0\text{V},$ $R_S = 50\Omega, f = 500\text{MHz}$	-	4.5	-	dB
d_{im}	Intermodulation distortion				
	$I_C = 10\text{mA}, V_{\text{CE}} = 6.0\text{V}, R_L = 37.5\Omega,$ $T_{\text{amb}} = 25^{\circ}\text{C}$				
	$V_o = 100\text{mV}$ at $f_p = 183\text{MHz}$				
	$V_o = 100\text{mV}$ at $f_q = 200\text{MHz}$				
	measured at $f_{(2q-p)} = 217\text{MHz}$	-	-45	-	dB

*Crystal mounted in a BFY90 envelope







μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

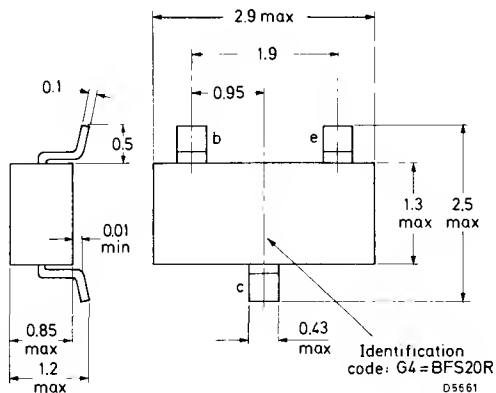
BFS20R

Silicon n-p-n planar epitaxial transistor in a microminiature plastic envelope, intended for i.f. and v.h.f. applications in thin and thick films. The device features a very low feedback capacitance.

QUICK REFERENCE DATA

V_{CBO}	max.	30	V
V_{CEO}	max.	20	V
I_C	max.	25	mA
P_{tot}	max. $T_{amb} \leq 25^\circ C$	200	mW
T_j	max.	150	$^\circ C$
h_{FE}	min., $I_C = 7mA, V_{CE} = 10V$	40	
f_T	typ., $I_C = 5mA, V_{CE} = 5V, f = 100MHz$	450	MHz
$-C_{re}$	max., $I_C = 1mA, V_{CE} = 10V, f = 1MHz$	0.4	pF

OUTLINE AND DIMENSIONS



All dimensions in millimetres

Plan view from above

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO}	max.	30	V
V_{CEO}	max. ($I_C = 2.0\text{mA}$)	20	V
V_{EBO}	max.	4.0	V
I_C	max.	25	mA
I_{CM}	max.	25	mA
P_{tot}	max. $T_{amb} \leq 25^\circ\text{C}$, mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	200	mW

Temperature

T_{stg}		-65 to +150	$^\circ\text{C}$
T_j	max.	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

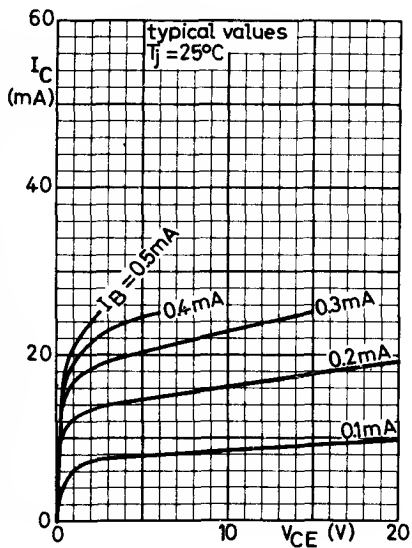
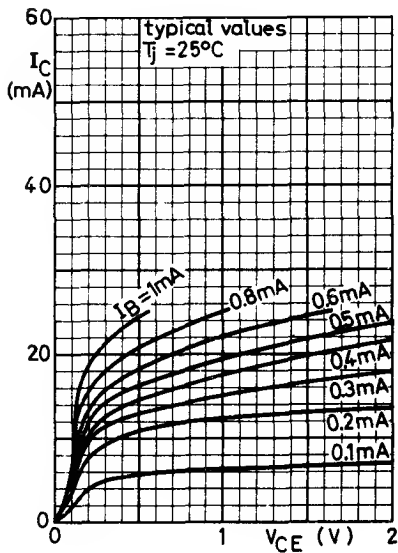
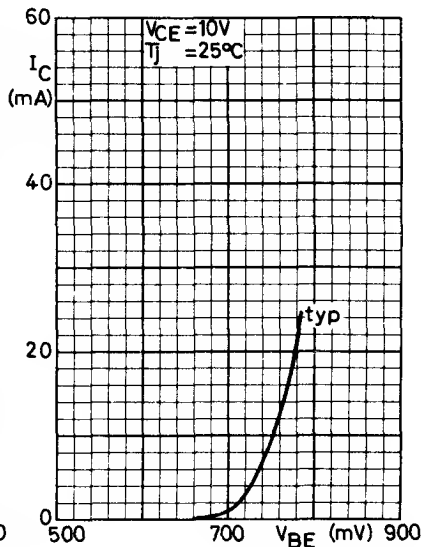
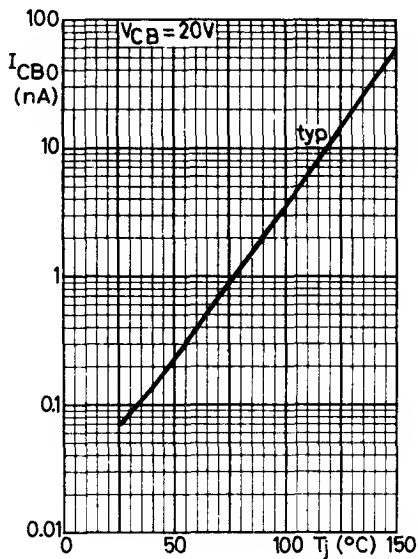
$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	0.62	$^\circ\text{C/mW}$
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

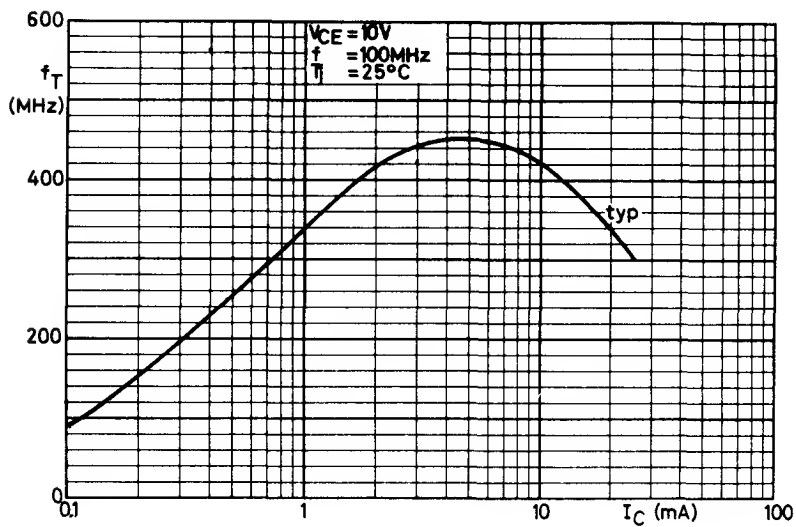
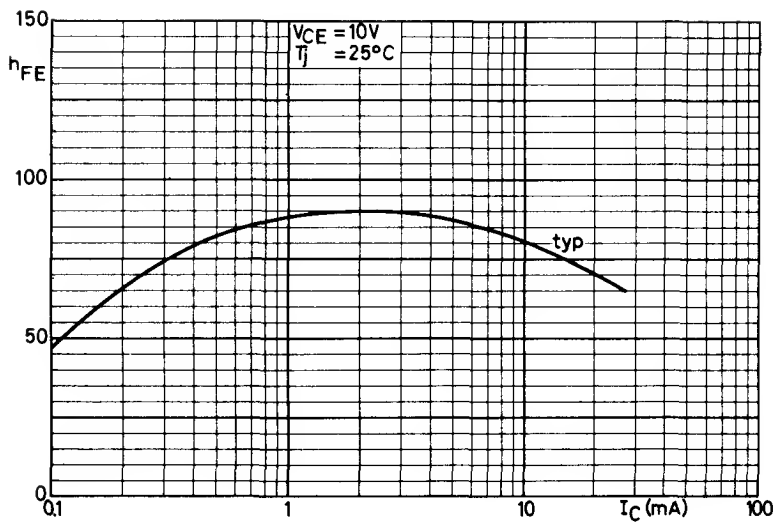
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$I_E = 0$, $V_{CB} = 20\text{V}$	-	-	100	nA
	$I_E = 0$, $V_{CB} = 20\text{V}$, $T_j = 100^\circ\text{C}$	-	-	10	μA
V_{BE}	Base-emitter voltage				
	$I_C = 7.0\text{mA}$, $V_{CE} = 10\text{V}$	-	740	900	mV
h_{FE}	Static forward current transfer ratio				
	$I_C = 7.0\text{mA}$, $V_{CE} = 10\text{V}$	40	85	-	
f_T	Transition frequency				
	$I_C = 5.0\text{mA}$, $V_{CE} = 10\text{V}$, $f = 100\text{MHz}$	275	450	-	MHz
$-C_{re}$	Feedback capacitance				
	$I_C = 1.0\text{mA}$, $V_{CE} = 10\text{V}$, $f = 1.0\text{MHz}$	-	0.35	0.40	pF
C_{Tc}	Collector capacitance				
	$I_E = I_c = 0$, $V_{CB} = 10\text{V}$, $f = 1.0\text{MHz}$	-	0.8	-	pF

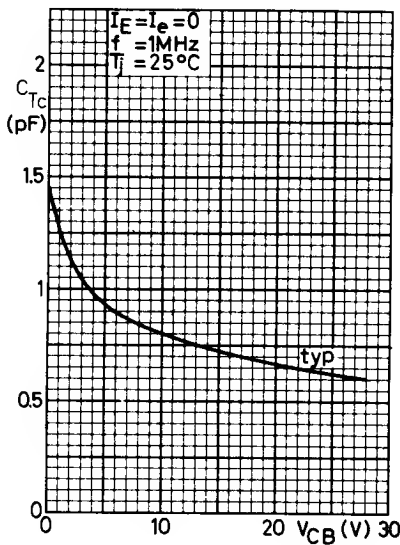
**μ min. N-P-N SILICON PLANAR
EPITAXIAL TRANSISTOR**

BFS20R



Mullard





**MATCHED N-CHANNEL
FIELD-EFFECT TRANSISTORS**

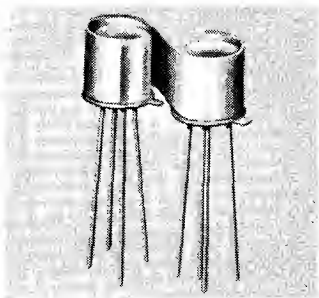
**BFS21A
BFS21**

Two matched N-channel silicon epitaxial planar junction-gate field-effect transistors in TO-72 metal envelopes, mounted together in an S-clip. This device is intended for low level differential amplifiers, sample and hold circuits, chopper circuits, etc. in instrumentation and control.

QUICK REFERENCE DATA				
		BFS21	BFS21A	
I_G	Gate cut-off leakage current $T_{amb} = 25^{\circ}C, V_{DG} = 15V, I_D = 0.5mA$	< 0.5	< 0.5	nA
$ \Delta V_{GS} $	Differential gate-source voltage $T_{amb} = 25^{\circ}C, V_{DG} = 15V, I_D = 0.5mA$	< 20	< 10	mV
$ \frac{d \Delta V_{GS}}{dT} $	Thermal drift of differential gate-source voltage $T_{amb} = 25^{\circ}C, V_{DG} = 15V, I_D = 0.5mA$	< 75	< 40	$\mu V/degC$
$ \Delta \frac{g_{os}}{g_{fs}} $	Difference of penetration factors $T_{amb} = 25^{\circ}C, V_{DG} = 15V, I_D = 0.5mA$	< 1.0	< 0.5	$\times 10^{-3}$
$ \Delta \frac{1}{g_{fs}} $	Difference of transfer impedances $T_{amb} = 25^{\circ}C, V_{DG} = 15V, I_D = 0.5mA$	< 15	< 7.5	Ω
C M R R	Common mode rejection ratio	> 60	> 66	dB

OUTLINE AND DIMENSIONS

Two devices conforming to J.E.D.E.C. TO-72 mounted in an S-clip
For details see page 5



RATINGS (of the total device)

Limiting values of operation according to the absolute maximum system

Electrical

$V_{\max.}$	Voltage between any two terminals	30	V
$I_D \max.$	Drain current	4.0	mA
$I_G \max.$	Gate current	0.5	mA
$P_{\text{tot}} \max.$	Total power dissipation ($T_{\text{clip}} < 100^\circ\text{C}$)	30	mW

Temperature

T_{amb}	Operating ambient temperature	-20 to +100	$^\circ\text{C}$
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ELECTRICAL CHARACTERISTICS (total device, $T_{\text{amb}} = 25^\circ\text{C}$ unless otherwise stated)

		BFS21	BFS21A	
$\frac{I_{\text{DSS1}}}{I_{\text{DSS2}}}$	Drain current ratio $V_D = 15\text{V}, V_{\text{GS}} = 0, T_j = 25^\circ\text{C}$	> 0.95	> 0.95	
		< 1.05	< 1.05	
$ V_{\text{GS1}} - V_{\text{GS2}} $	Differential gate-source voltage $I_D = 500\mu\text{A}, V_{\text{DG}} = 15\text{V}$ $I_D = 100\mu\text{A}, V_{\text{DG}} = 15\text{V}$	< 20 < 20	< 10 < 10	mV mV
$\frac{\Delta V_{\text{G1S1}} - V_{\text{G2S2}} }{\Delta T_{\text{amb}}}$	Thermal drift of differential gate-source voltage $I_D = 500\mu\text{A}, V_{\text{DG}} = 15\text{V}$ $I_D = 100\mu\text{A}, V_{\text{DG}} = 15\text{V}$	< 75 < 75	< 40 < 40	$\mu\text{V}/\text{degC}$ $\mu\text{V}/\text{degC}$
$\Delta V_{\text{G1S1}} - V_{\text{G2S2}} $	*Differential gate-source voltage change with ambient temperature $T_{\text{amb}} = 25 \text{ to } 100^\circ\text{C}$ $I_D = 500\mu\text{A}, V_{\text{DG}} = 15\text{V}$ $I_D = 100\mu\text{A}, V_{\text{DG}} = 15\text{V}$	< 6 < 6	< 3 < 3	mV mV
$ \Delta \frac{g_{\text{os}}}{g_{\text{fs}}} $	Difference of penetration factors (see note 1) $I_D = 500\mu\text{A}, V_{\text{DG}} = 15\text{V}$ $I_D = 100\mu\text{A}, V_{\text{DG}} = 15\text{V}$	< 1 < 1	< 0.5 < 0.5	10^{-3} 10^{-3}
$ \Delta \frac{1}{g_{\text{fs}}} $	Difference of transfer impedances (see note 2) $I_D = 500\mu\text{A}, V_{\text{DG}} = 15\text{V}$ $I_D = 100\mu\text{A}, V_{\text{DG}} = 15\text{V}$	< 15 < 75	< 7.5 < 37.5	Ω Ω
C M R R	Common mode rejection ratio (see note 3) $I_D = 500\mu\text{A}, V_{\text{DG}} = 15\text{V}$ $I_D = 100\mu\text{A}, V_{\text{DG}} = 15\text{V}$	> 60 > 60	> 66 > 66	dB dB

*Differential gate-source voltage change with ambient temperature $= |V_{\text{G1S1}} - V_{\text{G2S2}}|_{T_{\text{amb2}}} - |V_{\text{G1S1}} - V_{\text{G2S2}}|_{T_{\text{amb1}}}$

ELECTRICAL CHARACTERISTICS (contd.)

NOTES

1. The difference between the penetration factors is equal to the ratio of the change of the differential gate-source voltage (ΔV_{GS}) to the change of drain-gate voltage (V_{DG}) with the drain current (I_D) constant.

i.e.

$$\Delta \frac{g_{os}}{g_{fs}} = \frac{d \Delta V_{GS}}{d V_{DG}} \quad \text{at } I_D = \text{constant}$$

2. The difference between the transfer impedances is equal to the ratio of the change of the differential gate-source voltage (ΔV_{GS}) to the change of drain current (I_D), with the drain-gate voltage (V_{DG}) constant.

i.e.

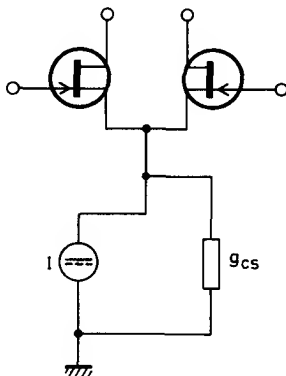
$$\Delta \frac{1}{g_{fs}} = \frac{d \Delta V_{GS}}{d I_D} \quad \text{at } V_{DG} = \text{constant}$$

3. The common mode rejection ratio

$$\frac{1}{C M R R} = \Delta \frac{g_{os}}{g_{fs}} + \frac{1}{2} g_{cs} \cdot \Delta \frac{1}{g_{fs}}$$

where g_{os} in this formula is the output conductance of the summing current source.

The guaranteed values of C M R R apply at $g_{cs} = 0.1 \mu\text{mho}$.



RATINGS (of the individual field-effect transistor)

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	30	V
V_{DGO} max.	Drain-gate voltage (open source)	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	30	V
I_D max.	Drain current	20	mA
I_G max.	Gate current	10	mA
P_{tot} max.	Power dissipation ($T_{amb} < 25^\circ\text{C}$)	300	mW

Temperature

T_{stg}	Storage temperature	-65 to +200	$^\circ\text{C}$
T_j max.	Junction temperature	+200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	for individual transistor without S-clip in free air	0.59	degC/mW
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ELECTRICAL CHARACTERISTICS (of the individual field-effect transistor)

$T_{amb} = 25^\circ\text{C}$ unless otherwise stated

I_G	Gate cut-off leakage current $I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$	< 0.5	nA
	$I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$, $T_{amb} = 100^\circ\text{C}$	< 25	nA
I_{DSS}	Drain current $V_{DG} = 15\text{V}$, $V_{GS} = 0$, $T_j = 25^\circ\text{C}$	> 1.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 0.5\text{nA}$, $V_{DG} = 15\text{V}$	< 6.0	V
g_{fs}	Transfer conductance $I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$, $f = 1\text{kHz}$	> 1.0	mmho
g_{os}	Output conductance $I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$, $f = 1\text{kHz}$	< 15	μmho
C_{is}	Input capacitance $I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$, $f = 1\text{MHz}$	< 5.0	pF
C_{rs}	Feedback capacitance $I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$, $f = 1\text{MHz}$	< 0.75	pF
$\frac{V_n}{\sqrt{B}}$	Equivalent noise voltage ($B = 5\text{Hz}$) $I_D = 500\mu\text{A}$, $V_{DG} = 15\text{V}$, $f = 10\text{Hz}$	< 200	$\text{nV}/\sqrt{\text{Hz}}$
	$V_{DG} = 15\text{V}$, $V_{GS} = 0$, $f = 10\text{Hz}$	< 75	$\text{nV}/\sqrt{\text{Hz}}$

BFS21A
BFS21

1) = shield lead (connected to case)

0.48 max diameter of leads controlled from bottom to 12.7 mm.

D1222

1. Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for a time of up to 10 seconds at least 1.5mm from the seal. At an iron temperature of 245°C to 400°C the maximum soldering time is 5 seconds at least 5mm from the seal.
2. These devices may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a device mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

SILICON N-CHANNEL DUAL-INSULATED-GATE FIELD-EFFECT TRANSISTOR

BFS28

The BFS28 is a silicon n-channel, depletion-type dual-insulated-gate M.O.S. field effect transistor. It is intended for a wide range of applications in communications, instrumentation and control.

QUICK REFERENCE DATA

V_{DS} max.	Drain-source voltage	20	V
$\pm V_{G1S}$ max.	Gate 1-source voltage	8.0	V
$\pm V_{G2S}$ max.	Gate 2-source voltage	8.0	V
I_D max.	Drain current	20	mA
P_{tot} max.	Total device power dissipation ($T_{amb} \leq 25^\circ C$)	200	mW
T_j max.	Maximum junction temperature	135	$^\circ C$

Characteristics

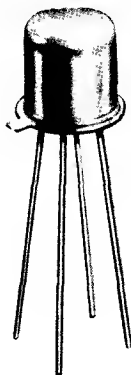
$I_D = 10\text{mA}$, $V_{DS} = 13\text{V}$, $V_{G2S} = +4.0\text{V}$

$ y_{fs} $ typ.	Small signal forward transfer admittance in common source ($f = 1\text{kHz}$)	13	mmho
G_a typ.	Power gain ($f = 200\text{MHz}$)	18	dB
$-C_{rs}$ typ.	Feedback capacitance ($f = 10\text{MHz}$)	25	fF
N typ.	Noise figure at optimum source admittance ($f = 200\text{MHz}$)	3	dB

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72
B.S. 3934 SO-12A/SB4-3

For details see page 4



Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DS} max.	Drain-source voltage	20	V
$\pm V_{G1S}$ max.	Gate 1-source voltage	8.0	V
$\pm V_{G2S}$ max.	Gate 2-source voltage	8.0	V
$\pm V_{G1SM}$ max.	Non-repetitive peak gate 1-source voltage ($t \leq 10\text{ms}$)	50	V
$\pm V_{G2SM}$ max.	Non-repetitive peak gate 2-source voltage ($t \leq 10\text{ms}$)	50	V
I_D max.	Drain current	20	mA
P_{tot} max.	Total device power dissipation ($T_{amb} \leq 25^\circ\text{C}$)	200	mW

Temperature

T_{stg} min.	-65	$^\circ\text{C}$
T_{stg} max.	+135	$^\circ\text{C}$
T_j max.	+135	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$$R_{th(j-amb)} = 0.55 \text{ degC/mW}$$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$-V_{G1S}$	Gate 1-source cut-off voltage $V_{DS} = 20\text{V}$, $I_D = 100\mu\text{A}$, $V_{G2S} = +4\text{V}$	-	-	5.0	V
$-V_{G2S}$	Gate 2-source cut-off voltage $V_{DS} = 20\text{V}$, $I_D = 50\mu\text{A}$, $V_{G1S} = 0$	-	-	4.0	V
$-V_{G1S}$	Gate 1-source voltage $I_D = 10\text{mA}$, $V_{DS} = 13\text{V}$, $V_{G2S} = +4\text{V}$	0.6	-	2.8	V
	$I_D = 4\text{mA}$, $V_{DS} = 10\text{V}$, $V_{G2S} = +4\text{V}$	1.0	-	3.2	V
$\pm I_{G1SS}$	Gate 1 leakage current $\pm V_{G1} = 8\text{V}$, $V_{G2S} = 0$, $V_{DS} = 0$, $T_j = 135^\circ\text{C}$	-	-	1.0	nA
$\pm I_{G2SS}$	Gate 2 leakage current $\pm V_{G2} = 8\text{V}$, $V_{G1S} = 0$, $V_{DS} = 0$, $T_j = 135^\circ\text{C}$	-	-	1.0	nA

SILICON N-CHANNEL DUAL-INSULATED-GATE FIELD-EFFECT TRANSISTOR

BFS28

ELECTRICAL CHARACTERISTICS (cont'd)

Small signal y-parameters (see also graphs on pages 6 and 7)

$I_D = 10\text{mA}$, $V_{DS} = 13\text{V}$, $V_{G2S} = +4\text{V}$, $T_{\text{amb}} = 25^\circ\text{C}$

		Min.	Typ.	Max.
$ y_{fs} $	Forward transfer admittance			
	$f = 1\text{kHz}$	8	13	- mmho
	$f = 200\text{MHz}$	-	12	- mmho
	$f = 500\text{MHz}$	-	11.3	- mmho
$-C_{rs}$	Feedback capacitance			
	$f = 10\text{MHz}$	-	25	- fF
G_a	Power gain			
	$I_D = 10\text{mA}$, $V_{DS} = 13\text{V}$, $V_{G2S} = +4\text{V}$, $f = 200\text{MHz}$, $G_S = 1.3\text{mmho}$, $G_L = 1\text{mmho}$, B_S and B_L tuned for maximum gain	-	18	- dB
G_{UM}	Max. unilateralised power gain (see note 1) $I_D = 10\text{mA}$, $V_{DS} = 13\text{V}$, $V_{G2S} = +4\text{V}$, $f = 200\text{MHz}$	-	20.5	- dB
	$f = 500\text{MHz}$	-	7.9	- dB
N	Noise figure at optimum source admittance			
	$I_D = 10\text{mA}$, $V_{DS} = 13\text{V}$, $V_{G2S} = +4\text{V}$, $f = 200\text{MHz}$, $G_{S(\text{opt})}$ typ. = 1.4mmho , $B_{S(\text{opt})}$ typ. = 5.5mmho	-	3.0	4.0 dB

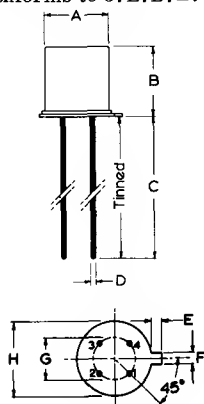
NOTE

$$1. \quad G_{UM} \approx 10 \log \frac{y_{fs}^2}{4 g_{is} \times g_{os}}$$

Mullard

OUTLINE AND DIMENSIONS

Conforms to J. E. D. E. C. TO-72



Millimetres

	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections

1. Drain
2. Gate 2
3. Gate 1
4. Source and substrate connected to case.

SOLDERING AND WIRING RECOMMENDATIONS

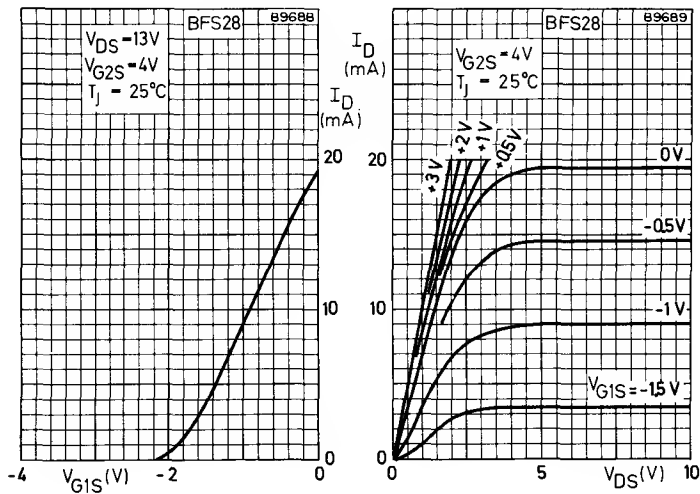
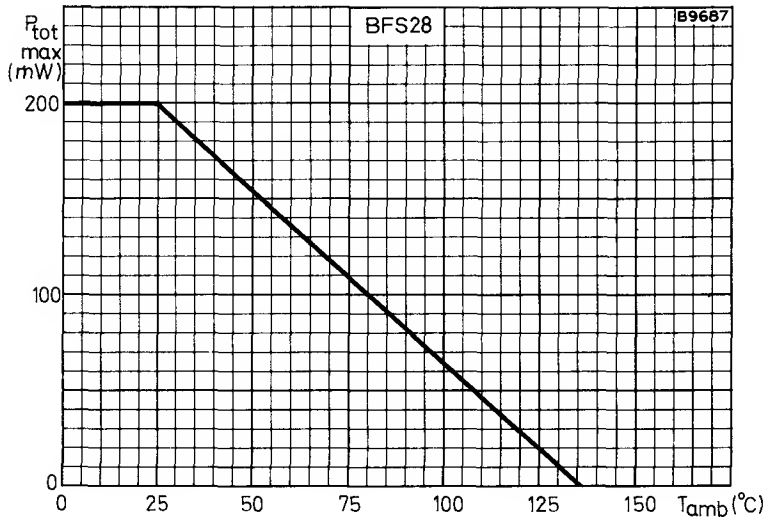
1. Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for a time of up to 10 seconds at least 1.5mm from the seal. At an iron temperature of 245°C to 400°C the maximum soldering time is 5 seconds at least 5mm from the seal.
2. These devices may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a device mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

HANDLING NOTE

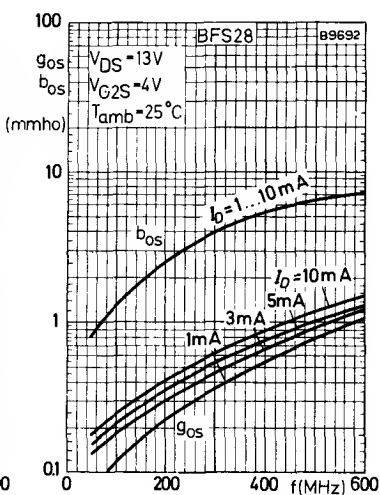
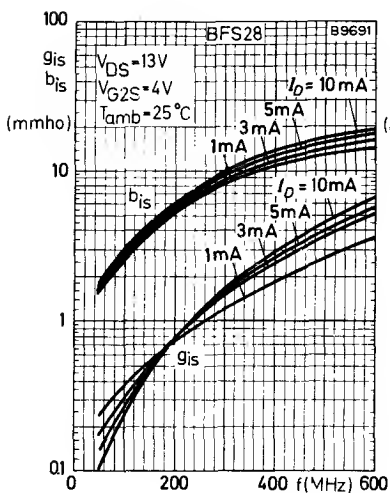
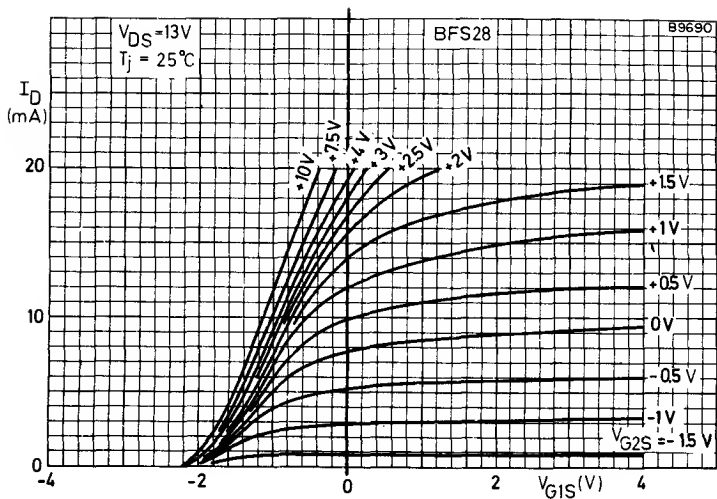
To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conducting rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.

SILICON N-CHANNEL
DUAL-INSULATED-GATE
FIELD-EFFECT TRANSISTOR

BFS28

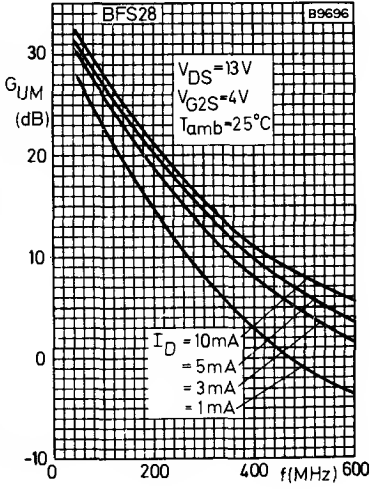
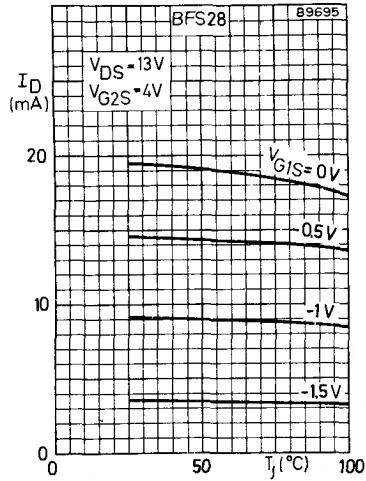
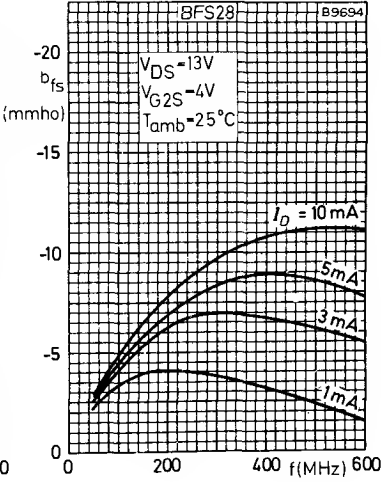
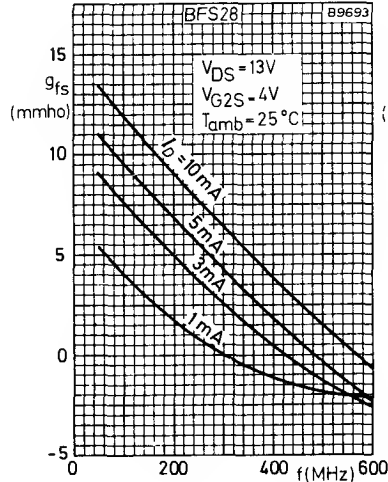


Mullard

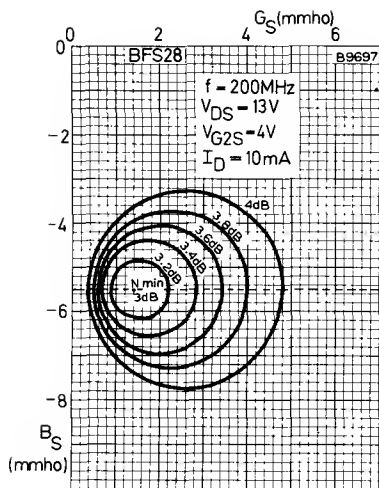


SILICON N-CHANNEL
DUAL-INSULATED-GATE
FIELD-EFFECT TRANSISTOR

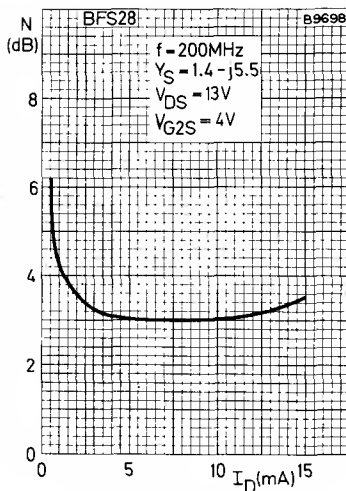
BFS28



Mullard



Circles of constant typical noise figure



Typical noise figure versus drain current

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT 24

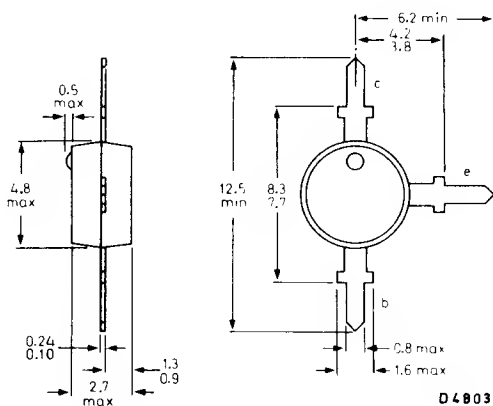
Silicon planar epitaxial n-p-n transistor in a subminiature plastic T-package, primarily intended for use in u.h.f. low power amplifiers such as in pocket phones, paging systems, etc.

The transistor features low current consumption (100 μ A -1mA), excellent wideband properties and low noise up to high frequencies.

QUICK REFERENCE DATA

V_{CBO}	max.	8.0	V
V_{CEO}	max.	5.0	V
I_C	max.	2.5	mA
P_{tot}	max. ($T_{amb} \leq 135^{\circ}C$)	30	mW
T_j	max.	150	$^{\circ}C$
f_T	typ. ($I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$)	2.3	GHz
C_{re}	max. ($I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 1.0MHz$)	0.4	pF
N	typ. ($I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$, at optimum source impedance)	3.8	dB
G_{UM}	typ. ($I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$)	17	dB

OUTLINE AND DIMENSIONS



All dimensions in millimetres

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

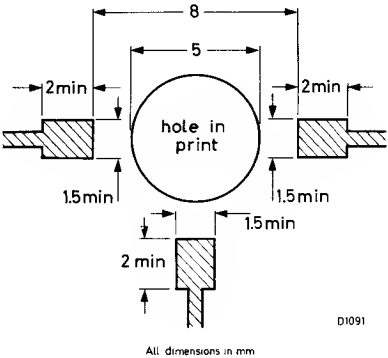
V_{CBO}	max.	8.0	V
V_{CEO}	max.	5.0	V
V_{EBO}	max.	2.0	V
I_C	max.	2.5	mA
I_{CM}	max. (peak value, $f > 1.0\text{MHz}$)	5.0	mA
P_{tot}	max. ($T_{amb} \leq 135^{\circ}\text{C}$)	30	mW

Temperature

T_{stg}		-65 to +150	$^{\circ}\text{C}$
T_j	max.	150	$^{\circ}\text{C}$

THERMAL CHARACTERISTIC

R_{th} (j-amb)	Thermal resistance from junction to ambient in free air, mounted on a glass-fibre print of $40 \times 25 \times 1\text{mm}$	0.5	$^{\circ}\text{C}/\text{mW}$
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All dimensions in mm

Requirements for a glass-fibre print

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT 24

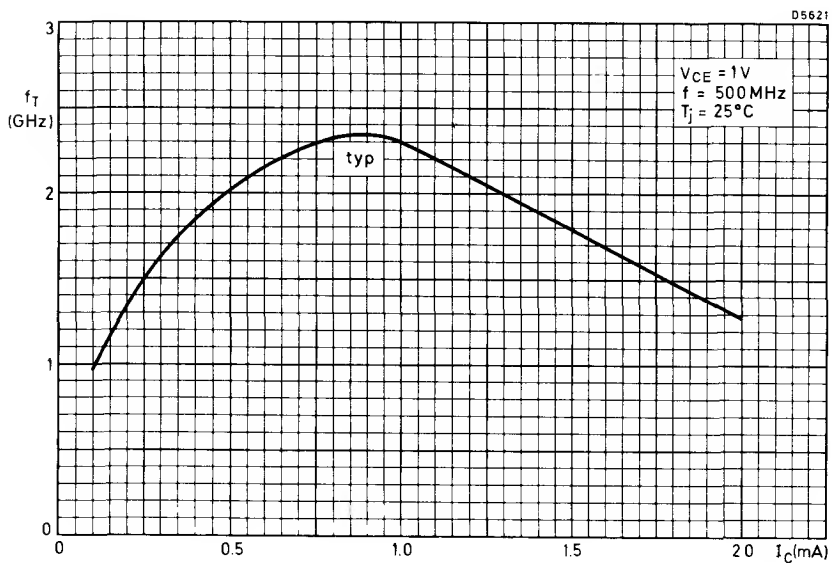
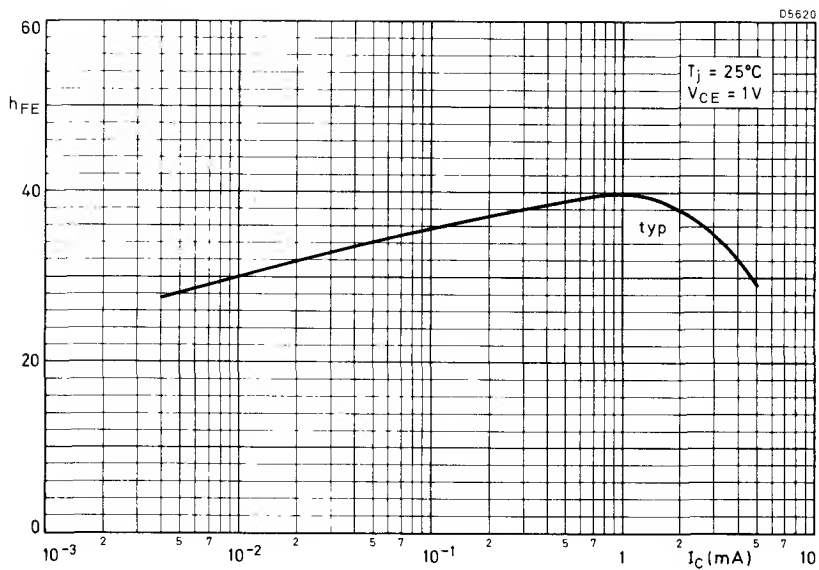
ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

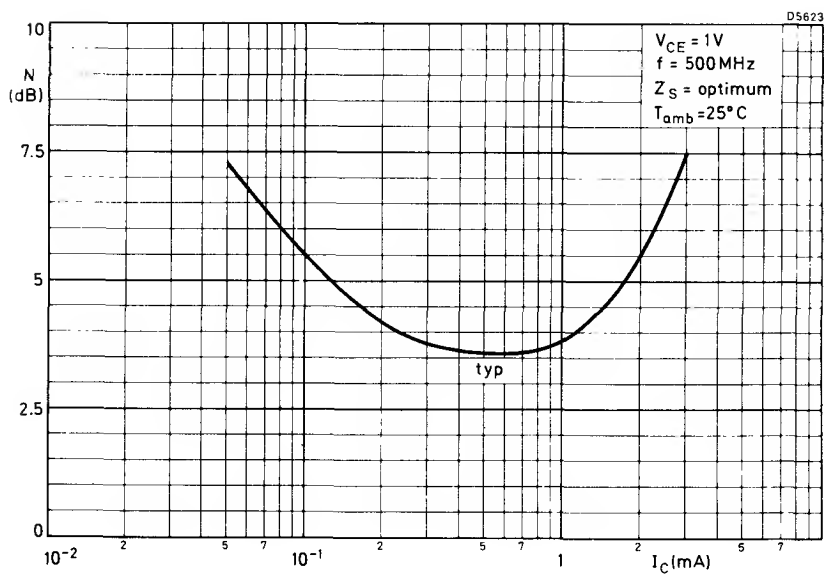
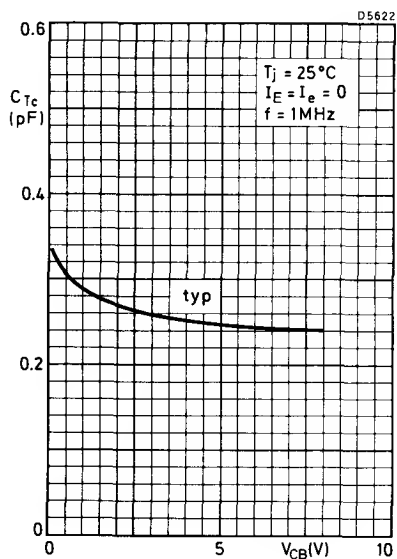
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0, V_{\text{CB}} = 5.0\text{V}$	-	-	50	nA
h_{FE}	Static forward current transfer ratio $I_C = 10\mu\text{A}, V_{\text{CE}} = 1.0\text{V}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}$	20 20	30 40	-	
$V_{\text{CE(sat)}}$	Collector-emitter saturation voltage $I_C = 10\mu\text{A}, I_B = 1.0\mu\text{A}$ $I_C = 1.0\text{mA}, I_B = 0.1\text{mA}$	- -	- -	100 125	mV
$V_{\text{BE(sat)}}$	Base-emitter saturation voltage $I_C = 10\mu\text{A}, I_B = 1.0\mu\text{A}$ $I_C = 1.0\text{mA}, I_B = 0.1\text{mA}$	- -	- -	700 850	mV
f_T	Transition frequency $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 500\text{MHz}$	1.2	2.3	-	GHz
C_{Tc}	Collector capacitance at $f = 1.0\text{MHz}$ $I_E = I_c = 0, V_{\text{CB}} = 0.5\text{V}$	-	-	0.55	pF
C_{Te}	Emitter capacitance at $f = 1.0\text{MHz}$ $I_C = I_c = 0, V_{\text{EB}} = 0$	-	-	0.45	pF
C_{re}	Feedback capacitance at $f = 1.0\text{MHz}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, T_{\text{amb}} = 25^{\circ}\text{C}$	-	-	0.4	pF
N	Noise figure at optimum source impedance, $f = 500\text{MHz}, T_{\text{amb}} = 25^{\circ}\text{C}$ $I_C = 0.1\text{mA}, V_{\text{CE}} = 1.0\text{V}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}$	- -	5.5 3.8	-	dB
G_{UM}	Max. unilateral power gain (s_{re} assumed to be zero), $T_{\text{amb}} = 25^{\circ}\text{C}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 200\text{MHz}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 500\text{MHz}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 800\text{MHz}$	- - -	24 17 11	-	dB

$$G_{\text{UM}} (\text{in dB}) = 10 \log \frac{|s_{\text{fe}}|^2}{(1 - |s_{\text{ie}}|^2)(1 - |s_{\text{oe}}|^2)}$$

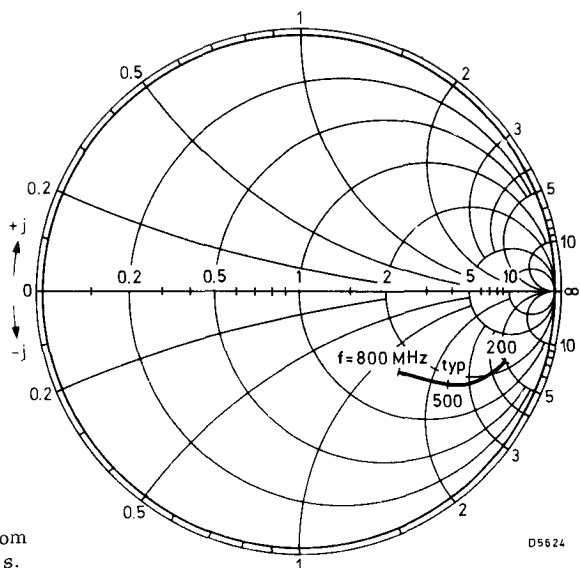
*Measured under pulse conditions.

Mullard



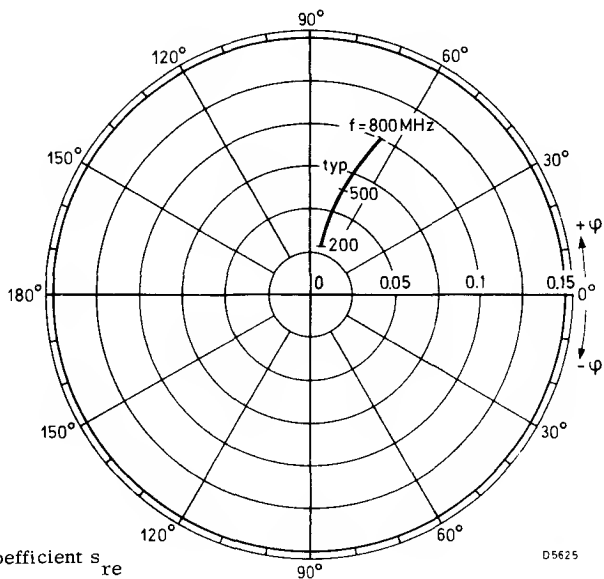


$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^{\circ}C$



Input impedance derived from
 input reflection coefficient s_{ie}
 coordinates in $\text{ohm} \times 50$

$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^{\circ}C$

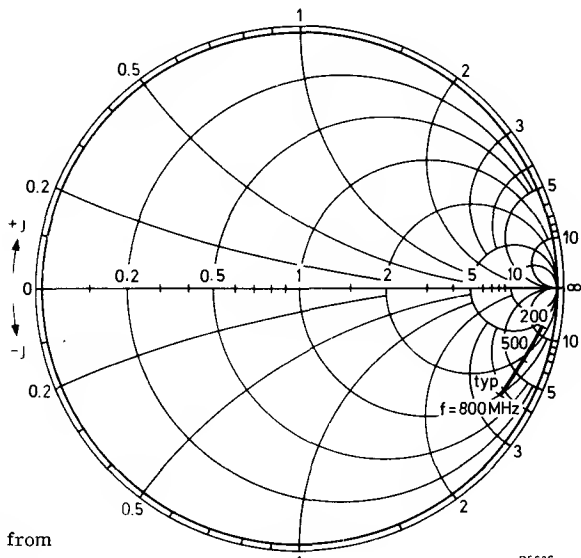


Reverse transmission coefficient s_{re}

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT 24

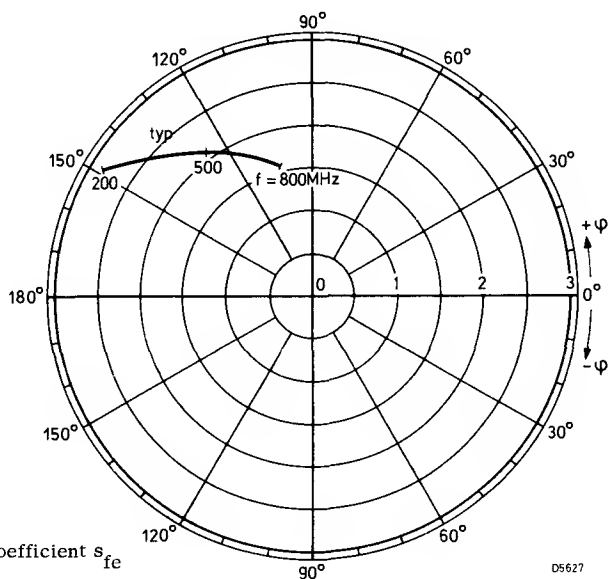
$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^{\circ}C$



D5626

Output impedance derived from
output reflection coefficient s_{oe}
coordinates in ohm $\times 50$

$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^{\circ}C$



D5627

Forward transmission coefficient s_{fe}

Mullard

μ min. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT25

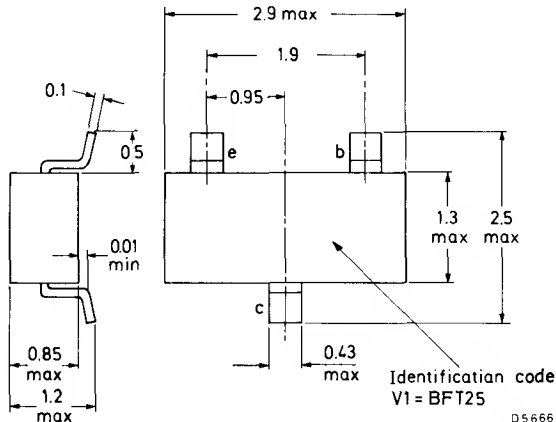
Silicon planar epitaxial n-p-n transistor in a microminiature plastic envelope, primarily intended for use in u.h.f. low power amplifiers, in thick and thin film circuits such as in pocket phones, paging systems, etc.

The transistor features low current consumption (100 μ A -1mA), excellent wideband properties and low noise up to high frequencies.

QUICK REFERENCE DATA

V_{CBO}	max.	8.0	V
V_{CEO}	max.	5.0	V
I_C	max.	2.5	mA
P_{tot}	max. ($T_{amb} \leq 135^{\circ}C$)	30	mW
T_j	max.	150	$^{\circ}C$
f_T	typ. ($I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz$)	2.3	GHz
C_{re}	max. ($I_C = 1.0mA, V_{CE} = 1.0V, f = 1.0MHz$)	0.45	pF
N	typ. ($I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz$, at optimum source impedance)	3.8	dB
G_{UM}	typ. ($I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz$)	18	dB

OUTLINE AND DIMENSIONS



All dimensions in millimetres

Plan view from above

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO}	max.	8.0	V
V_{CEO}	max.	5.0	V
V_{EBO}	max.	2.0	V
I_C	max.	2.5	mA
I_{CM}	max. (peak value, $f > 1.0\text{MHz}$)	5.0	mA
P_{tot}	max. ($T_{amb} \leq 135^{\circ}\text{C}$, mounted on a ceramic substrate of $15 \times 10 \times 0.5\text{mm}$)	30	mW

Temperature

T_{stg}		-65 to +150	$^{\circ}\text{C}$
T_j	max.	150	$^{\circ}\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance from junction to ambient in free air, mounted on a ceramic substrate of $15 \times 10 \times 0.5\text{mm}$	0.5	$^{\circ}\text{C/mW}$
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μ min. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT25

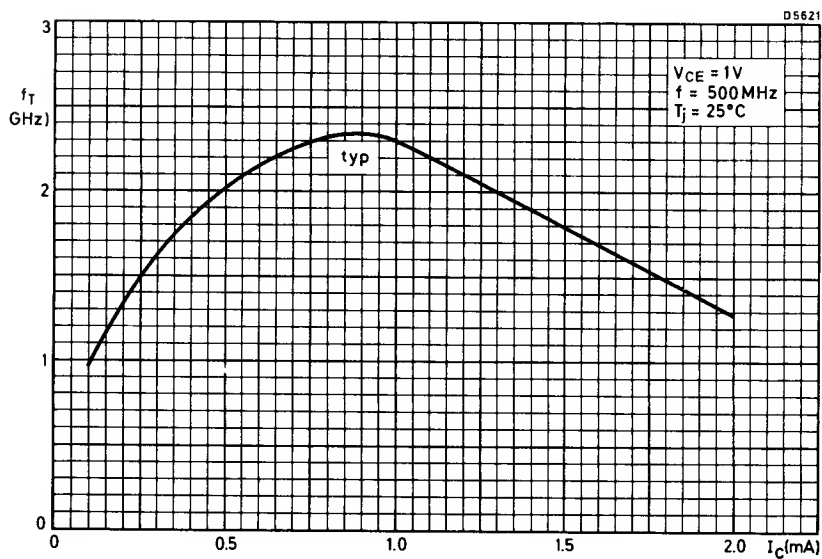
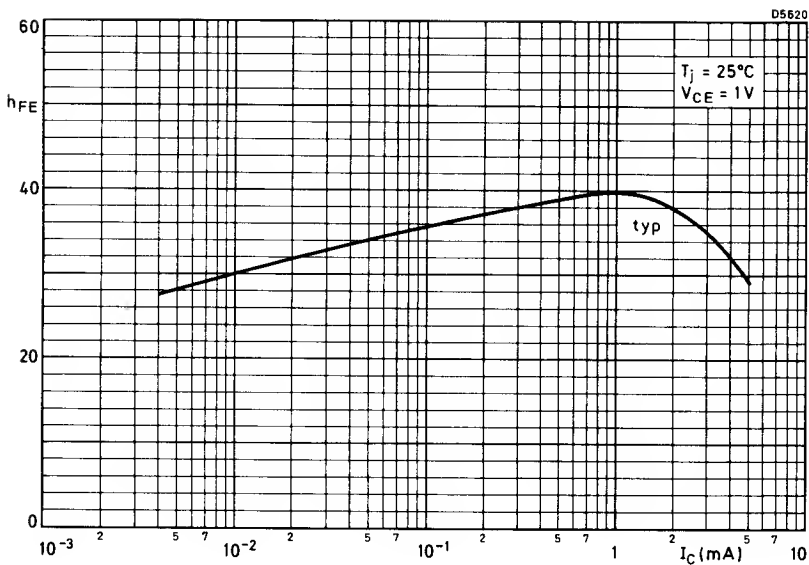
ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0, V_{\text{CB}} = 5.0\text{V}$	-	-	50	nA
h_{FE}	Static forward current transfer ratio $I_C = 10\mu\text{A}, V_{\text{CE}} = 1.0\text{V}$	20	30	-	
	$I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}$	20	40	-	
$V_{\text{CE(sat)}}$	Collector-emitter saturation voltage $I_C = 10\mu\text{A}, I_B = 1.0\mu\text{A}$	-	-	200	mV
	$I_C = 1.0\text{mA}, I_B = 0.1\text{mA}$	-	-	175	mV
$V_{\text{BE(sat)}}$	Base-emitter saturation voltage $I_C = 10\mu\text{A}, I_B = 1.0\mu\text{A}$	-	-	750	mV
	$I_C = 1.0\text{mA}, I_B = 0.1\text{mA}$	-	-	900	mV
f_{T}	Transition frequency $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 500\text{MHz}$	1.2	2.3	-	GHz
C_{Tc}	Collector capacitance at $f = 1.0\text{MHz}$ $I_E = I_e = 0, V_{\text{CB}} = 0.5\text{V}$	-	-	0.6	pF
C_{Te}	Emitter capacitance at $f = 1.0\text{MHz}$ $I_C = I_c = 0, V_{\text{EB}} = 0$	-	-	0.5	pF
C_{re}	Feedback capacitance at $f = 1.0\text{MHz}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, T_{\text{amb}} = 25^\circ\text{C}$	-	-	0.45	pF
N	Noise figure at optimum source impedance, $f = 500\text{MHz}, T_{\text{amb}} = 25^\circ\text{C}$ $I_C = 0.1\text{mA}, V_{\text{CE}} = 1.0\text{V}$	-	5.5	-	dB
	$I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}$	-	3.8	-	dB
G_{UM}	Max. unilateral power gain (s_{re} assumed to be zero), $T_{\text{amb}} = 25^\circ\text{C}$ $I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 200\text{MHz}$	-	25	-	dB
	$I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 500\text{MHz}$	-	18	-	dB
	$I_C = 1.0\text{mA}, V_{\text{CE}} = 1.0\text{V}, f = 800\text{MHz}$	-	12	-	dB

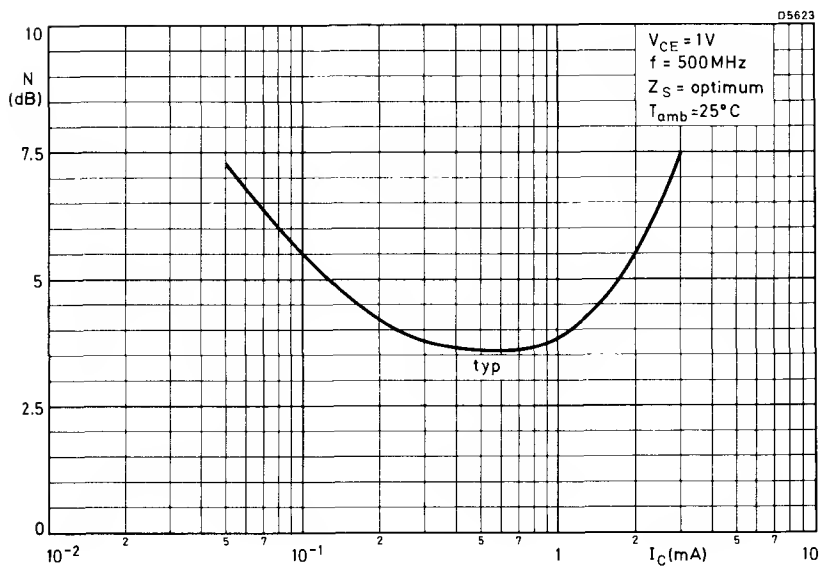
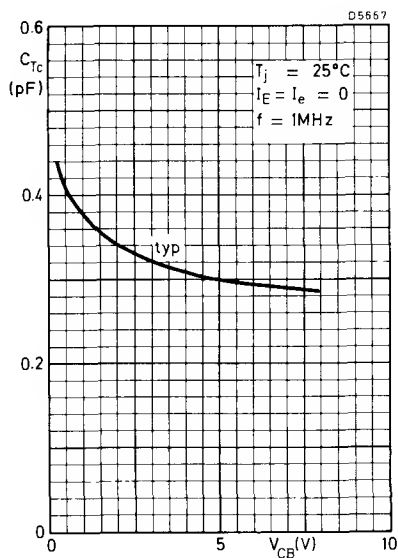
$$G_{\text{UM}} \text{ (in dB)} = 10 \log \frac{|s_{\text{fe}}|^2}{(1 - |s_{\text{ie}}|^2)(1 - |s_{\text{oe}}|^2)}$$

*Measured under pulse conditions.

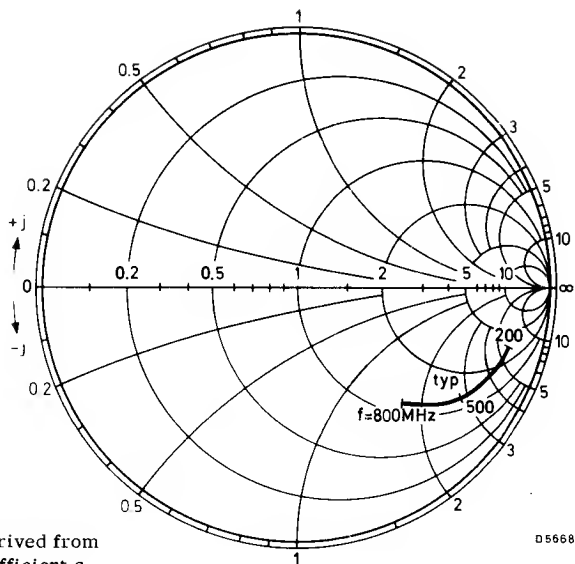
Mullard



Mullard

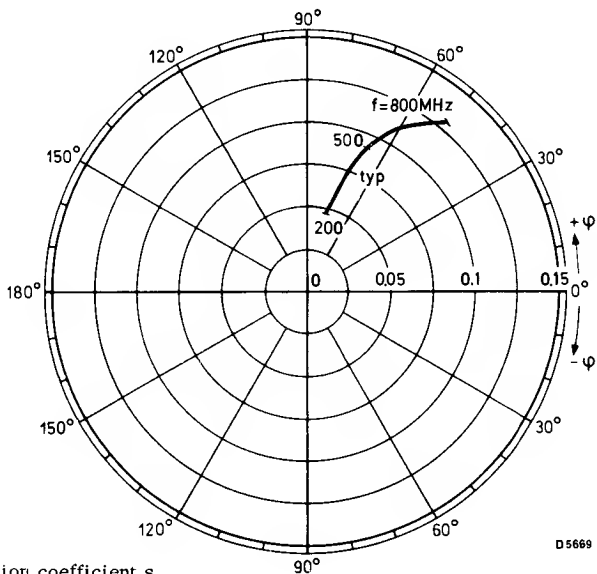


$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^{\circ}C$



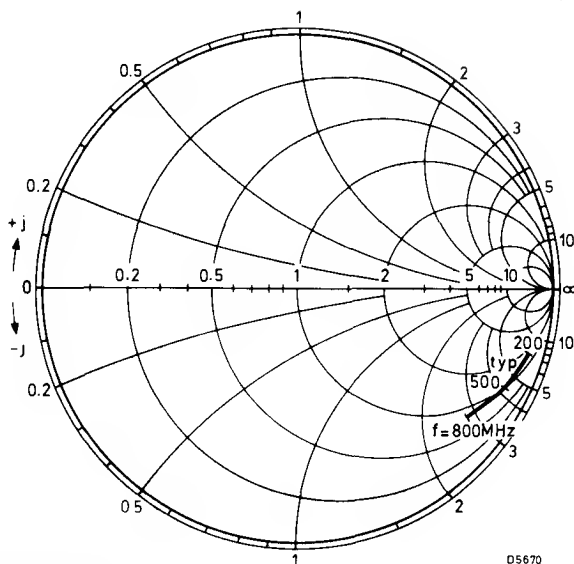
Input impedance derived from
 input reflection coefficient s_{ie}
 coordinates in $\text{ohm} \times 50$

$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^{\circ}C$



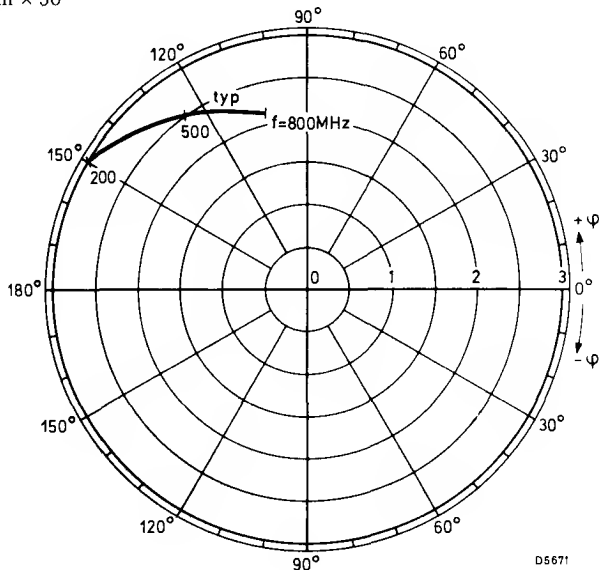
Reverse transmission coefficient s_{re}

$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^\circ C$



Output impedance derived from
output reflection coefficient s_{oe}
coordinates in ohm $\times 50$

$V_{CE} = 1.0V$
 $I_C = 1.0mA$
 $T_{amb} = 25^\circ C$



Forward transmission coefficient s_{fe}

N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

BFW10 BFW11

N-Channel depletion mode silicon epitaxial planar junction field effect transistors designed for use in wide-band amplifiers (0 to 300MHz). Their very low noise figure at low frequencies makes them suitable for differential amplifiers, electromedical and nuclear detector pre-amplifiers. They are in TO-72 encapsulation with a shield lead connected to case.

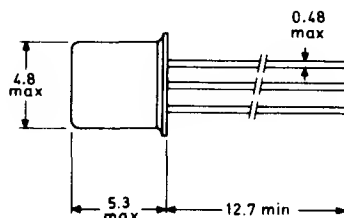
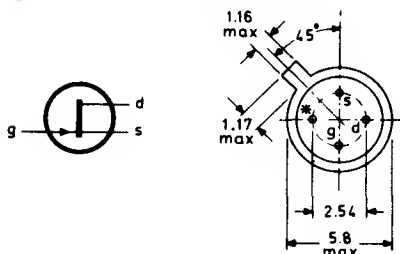
QUICK REFERENCE DATA

$\pm V_{DS}$ max.	30	V	
$-V_{GSO}$ max. (open drain)	30	V	
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	300	mW	
	BFW10	BFW11	
I_{DSS} ($V_{DS} = 15V$, $V_{GS} = 0$) min.	8.0	4.0	mA
	20	10	mA
$-V_{(P)GS}$ max. ($I_D = 0.5nA$, $V_{DS} = 15V$)	8.0	6.0	V
$-C_{rs}$ max. ($f = 1.0MHz$, $V_{DS} = 15V$, $V_{GS} = 0$)	0.80	0.80	pF
$ y_{fs} $ min. ($f = 200MHz$, $V_{DS} = 15V$, $V_{GS} = 0$)	3.2	3.2	mA/V
N max. ($f = 100MHz$, $V_{DS} = 15V$, $V_{GS} = 0$, $R_G = 1k\Omega$)	2.5	2.5	dB
V_n/\sqrt{B} max. ($f = 10Hz$, $B = 5.0Hz$)	75	75	nV/ \sqrt{Hz}

Unless otherwise stated, data are applicable to both types

OUTLINE AND DIMENSIONS

Conforms to J. E. D. E. C. TO-72
B.S. 3934 SO-12A/SB4-3



All dimensions in mm

Insulated electrodes

*Shield lead (connected to case)

Accessories available: 56246, 56263

02967

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DGO} max.	Drain-gate voltage (open source)	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	30	V
I_D max.	Drain current	20	mA
I_G max.	Gate current	10	mA
P_{tot} max.	Power dissipation ($T_{amb} \leq 25^\circ\text{C}$)	300	mW

Temperature

T_{stg} min.	-65	$^\circ\text{C}$
T_{stg} max.	200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.59	$^\circ\text{C}/\text{mW}$
-----------------	------	----------------------------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		BFW10	BFW11	
$-I_{GSS}$	Gate cut-off current			
	$-V_{GS} = 20\text{V}, V_{DS} = 0$	max. 0.1	0.1	nA
	$-V_{GS} = 20\text{V}, V_{DS} = 0,$ $T_j = 150^\circ\text{C}$	max. 0.5	0.5	μA
I_{DSS}	*Drain current			
	$V_{DS} = 15\text{V}, V_{GS} = 0$	min. 8.0 max. 20	4.0 10	mA mA
$-V_{GS}$	Gate-source voltage			
	$I_D = 400\mu\text{A}, V_{DS} = 15\text{V}$	min 2.0 max. 7.5	- -	V V
	$I_D = 50\mu\text{A}, V_{DS} = 15\text{V}$	min. - max. -	1.25 4.0	V V

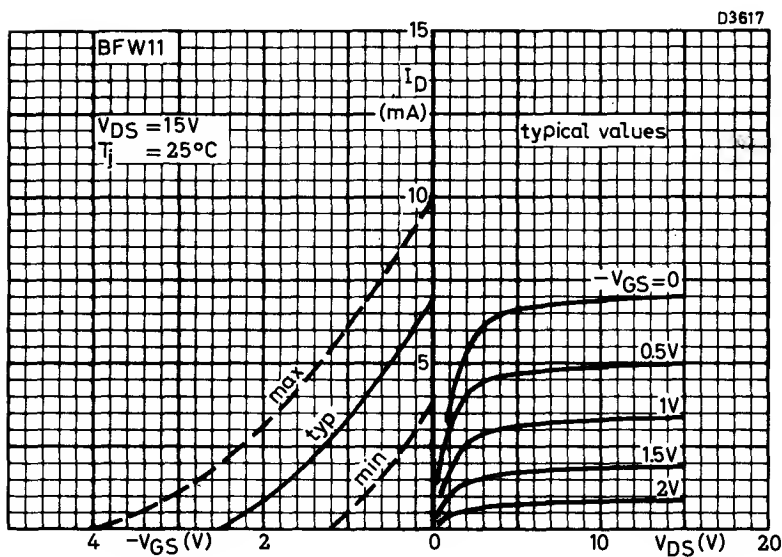
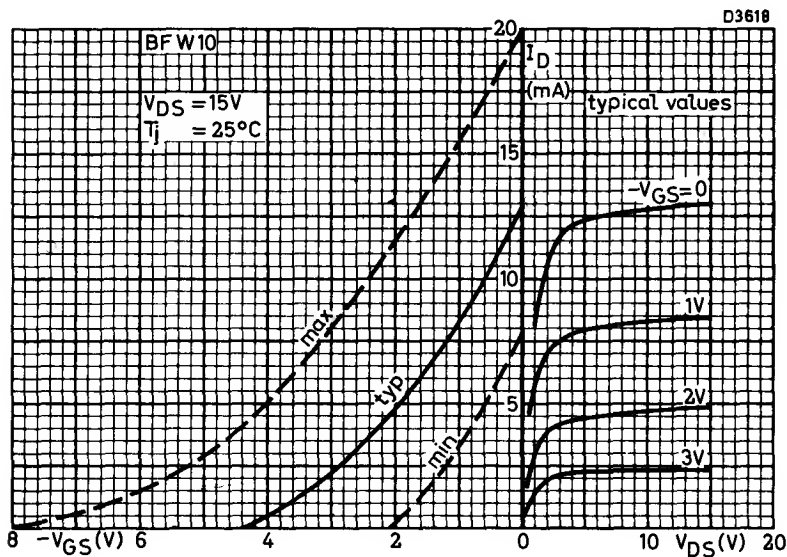
*Measured under pulsed conditions.

N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

BFW10
BFW11

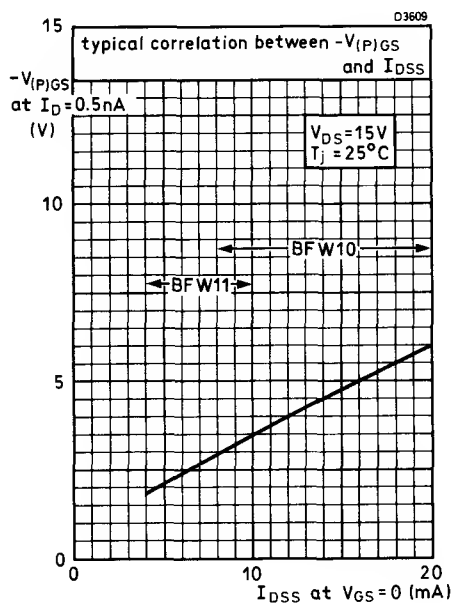
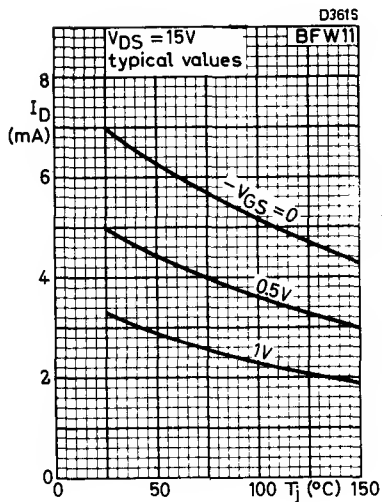
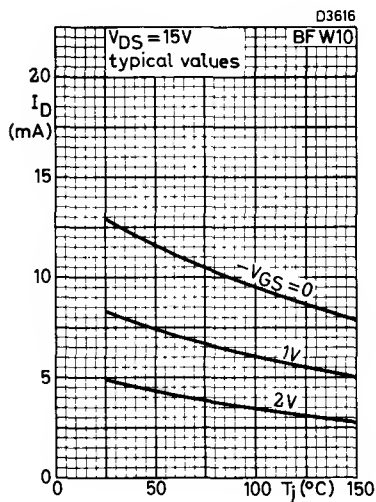
ELECTRICAL CHARACTERISTICS (contd.)

			BFW10	BFW11	
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 0.5nA, V_{DS} = 15V$	max.	8.0	6.0	V
y-parameters $V_{DS} = 15V, V_{GS} = 0, T_{amb} = 25^{\circ}C$					
$f = 1.0kHz$					
$ y_{fs} $	Transfer admittance	min.	3.5	3.0	mA/V
		max.	6.5	6.5	mA/V
$ y_{os} $	Output admittance	max.	85	50	$\mu A/V$
$f = 1.0MHz$					
C_{is}	Input capacitance	typ.	4.0	4.0	pF
		max.	5.0	5.0	pF
$-C_{rs}$	Feedback capacitance	typ.	0.6	0.6	pF
		max.	0.80	0.80	pF
$f = 200MHz$					
$ y_{fs} $	Transfer admittance	min.	3.2	3.2	mA/V
g_{is}	Input conductance	max.	800	800	$\mu A/V$
g_{os}	Output conductance	max.	200	100	$\mu A/V$
N	Noise figure, $T_{amb} = 25^{\circ}C$ $f = 100MHz, R_G = 1k\Omega$ $V_{DS} = 15V, V_{GS} = 0$, (input tuned to minimum noise)	max.	2.5	2.5	dB
V_n/\sqrt{B}	Equivalent noise voltage $V_{DS} = 15V, V_{GS} = 0, f = 10Hz$, $T_{amb} = 25^{\circ}C$	max.	75	75	nV/ \sqrt{Hz}

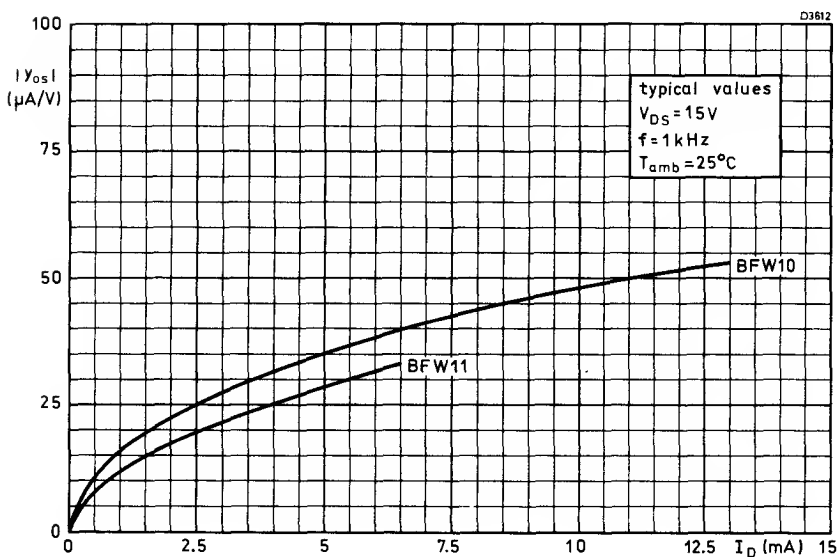
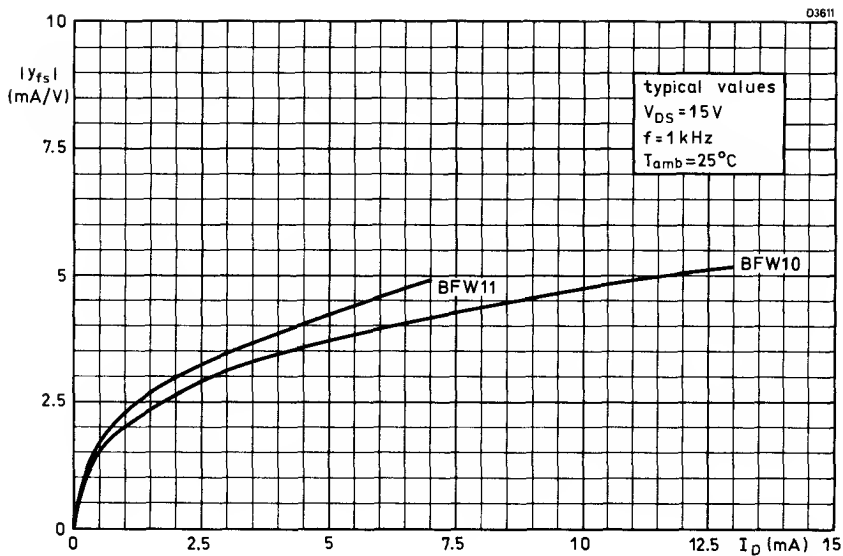


N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

BFW10
BFW11

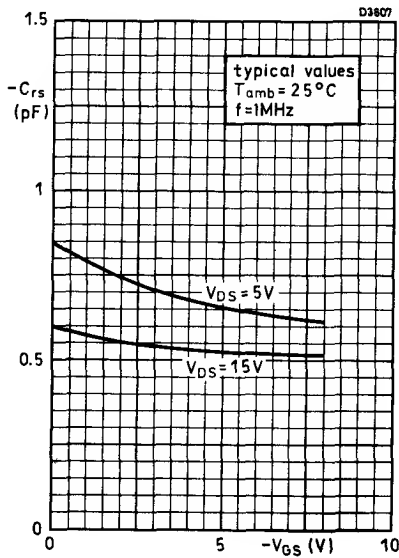
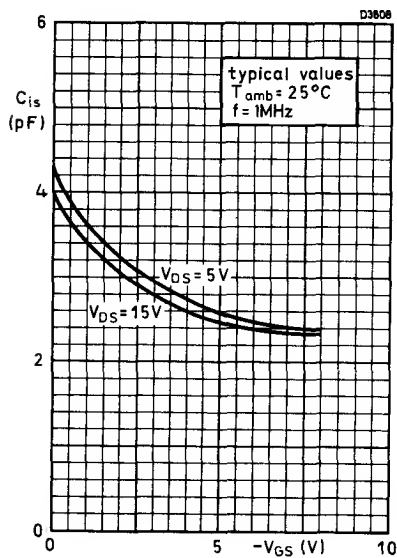


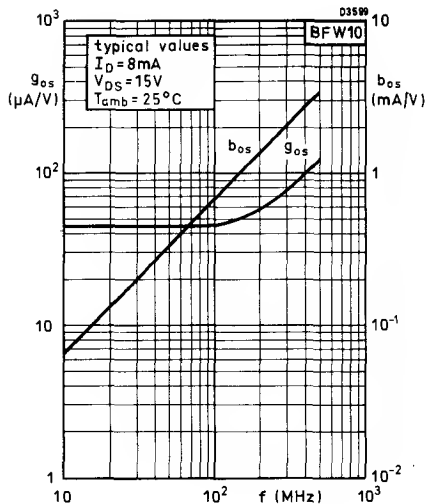
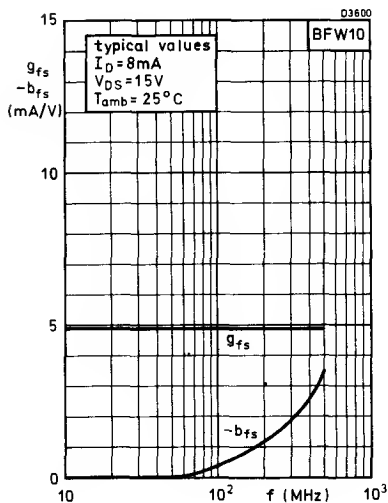
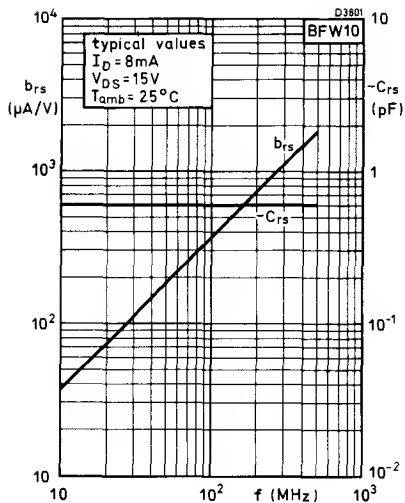
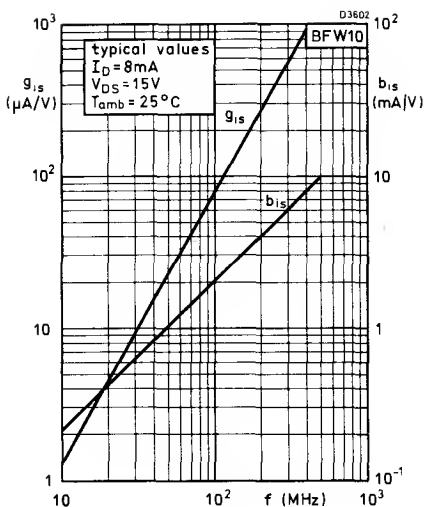
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N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

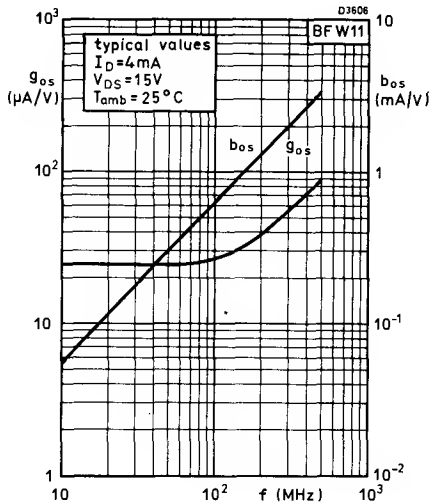
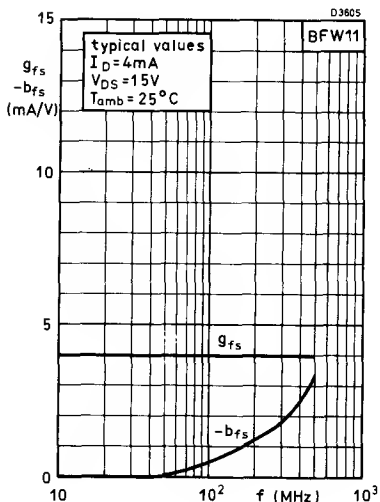
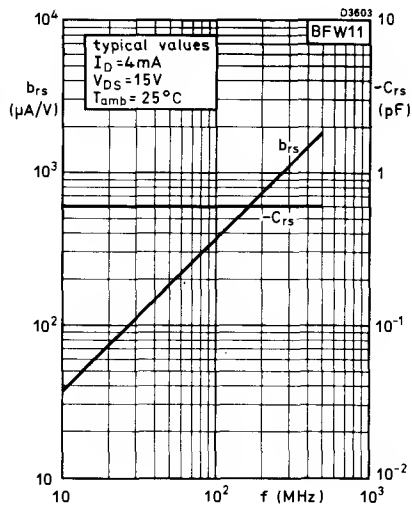
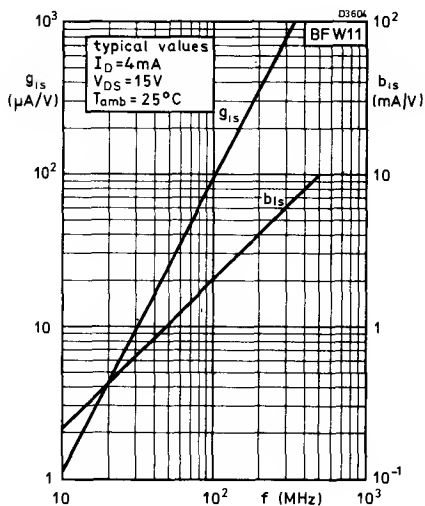
BFW10
BFW11



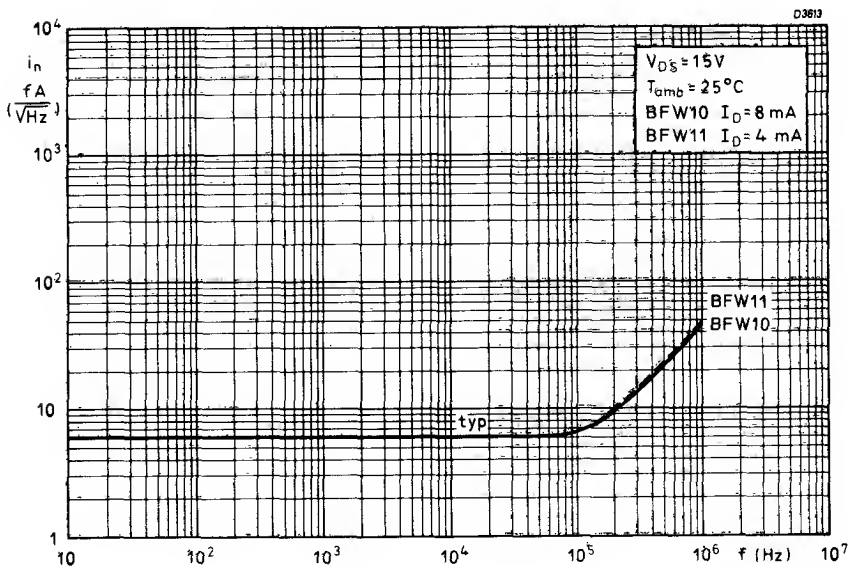
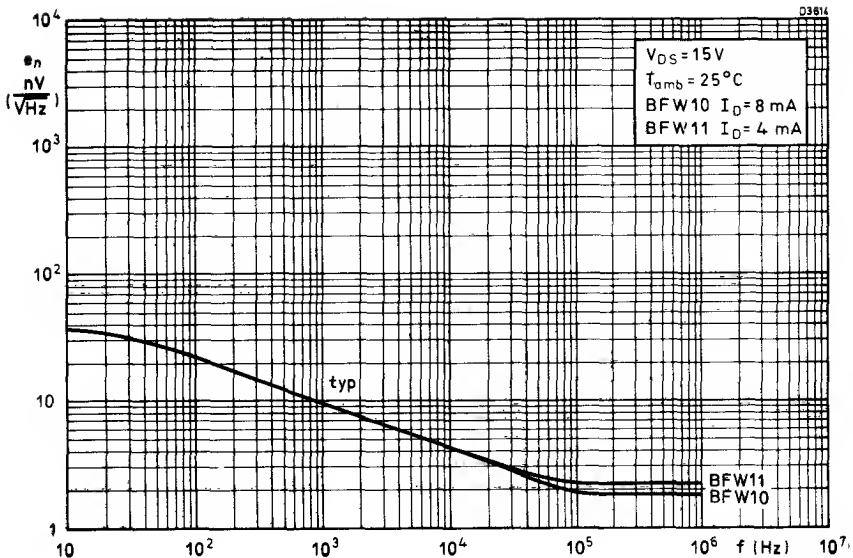


N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

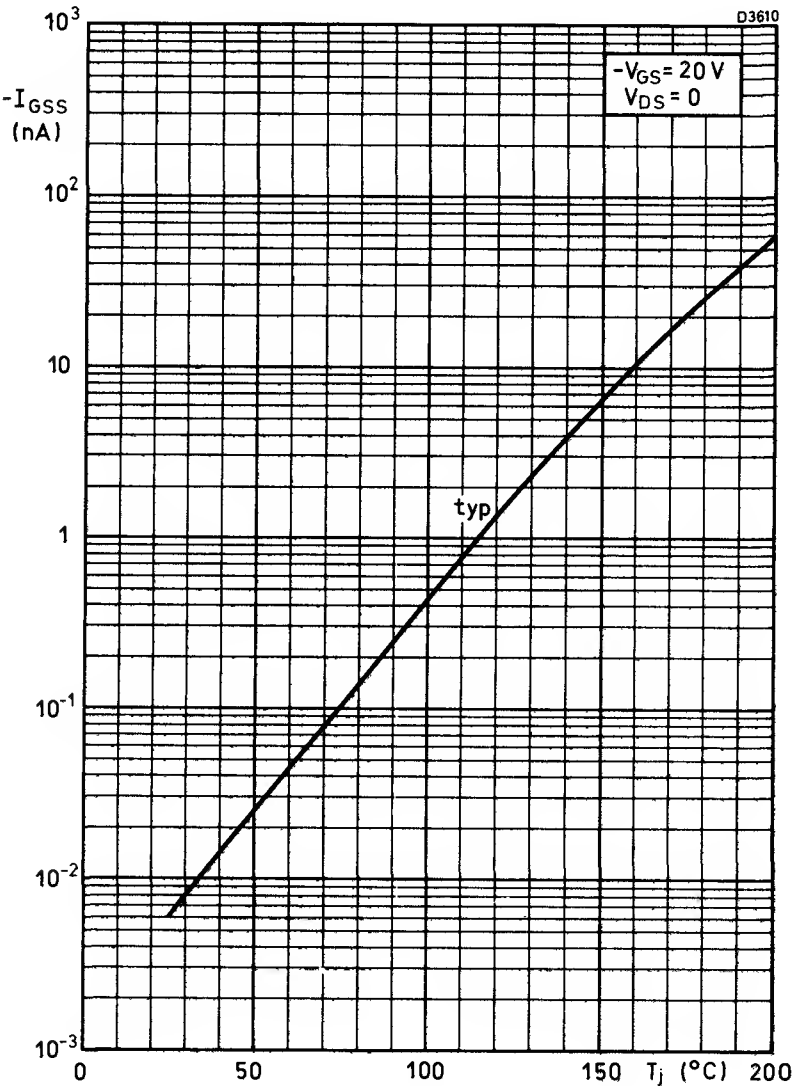
BFW10
BFW11



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N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFW16A

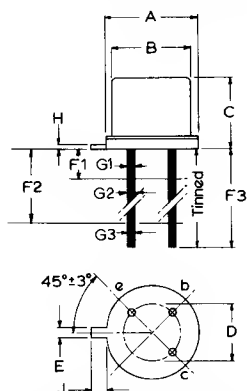
N-P-N silicon planar epitaxial, multi-emitter transistor with extremely good inter-modulation properties and a high power gain. The BFW16A is primarily intended for the final and driver stages of channel and band aerial amplifiers with high output power in bands I to V (40-860MHz), and for the final stage of wideband vertical deflection amplifiers in high speed oscilloscopes. Encapsulated in a metal TO-39 envelope with the collector connected to case. The BFW16A is a ruggedized version of BFW16, which it succeeds.

QUICK REFERENCE DATA

V_{CBOM} max.	40	V
V_{CEO} max.	25	V
I_{CM} max. ($f > 1.0\text{MHz}$)	300	mA
P_{tot} max. ($T_{case} \leq 125^\circ\text{C}$)	1.5	W
T_j max.	200	$^\circ\text{C}$
f_T typ. ($I_C = 150\text{mA}$, $V_{CE} = 15\text{V}$, $f = 500\text{MHz}$)	1.2	GHz
$-C_{re}$ typ. ($I_C = 10\text{mA}$, $V_{CE} = 15\text{V}$, $f = 1.0\text{MHz}$)	1.7	pF
G_p typ. ($I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$) $f = 200\text{MHz}$	16	dB
$f = 800\text{MHz}$	6.5	dB
P_o typ. ($I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$) $f = 200\text{MHz}$	150	mW
$f = 800\text{MHz}$	90	mW

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



Millimetres

	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

Accessories available:- 56218, 56245, 56265

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	40	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	40	V
V_{CEO} max. ($I_C = 10mA$)	25	V
V_{EBO} max.	2.0	V
I_C max.	150	mA
I_{CM} max. ($f > 1.0MHz$)	300	mA
P_{tot} max. ($T_{case} \leq 125^\circ C$)	1.5	W

Temperature

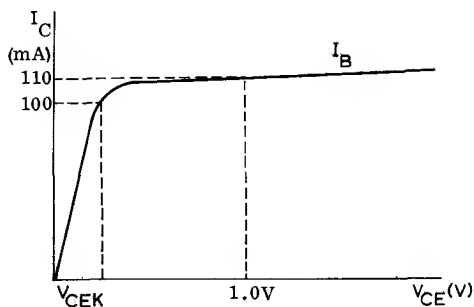
T_{stg} min.	-65	$^\circ C$
T_{stg} max.	200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	250	degC/W
$R_{th(j-case)}$	50	degC/W
$R_{th(case-h)}$ when mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 20V$, $I_E = 0$, $T_j = 150^\circ C$	-	-	20	μA
V_{CEK}	Collector-emitter knee voltage $I_C = 100mA$, $I_B =$ the value for which $I_C = 110mA$, at $V_{CE} = 1.0V$	-	-	0.75	V



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N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFW16A

ELECTRICAL CHARACTERISTICS (contd.)

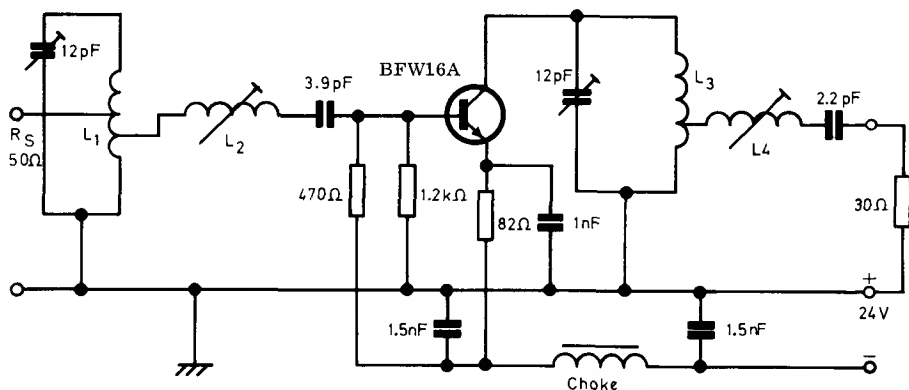
		Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio				
	$I_C = 50\text{mA}$, $V_{CE} = 5.0\text{V}$	25	-	-	
	$I_C = 150\text{mA}$, $V_{CE} = 5.0\text{V}$	25	-	-	
f_T	Transition frequency				
	$I_C = 150\text{mA}$, $V_{CE} = 15\text{V}$, $f = 500\text{MHz}$	-	1.2	-	GHz
C_{Tc}	Collector capacitance $V_{CB} = 15\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	-	4.0	pF
$-C_{re}$	Feedback capacitance $I_C = 10\text{mA}$, $V_{CE} = 15\text{V}$, $f = 1.0\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	-	1.7	-	pF
N	Noise figure				
	$I_C = 30\text{mA}$, $V_{CE} = 15\text{V}$, $f = 200\text{MHz}$, $R_s = 75\Omega$, $T_{amb} = 25^\circ\text{C}$	-	-	6.0	dB
G_P	Power gain (not neutralised)				
	$I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$, $T_{amb} = 25^\circ\text{C}$				
	$f = 200\text{MHz}$	-	16	-	dB
	$f = 800\text{MHz}$	-	6.5	-	dB

Intermodulation characteristics

P_o	Output power (see test circuits)				
	$I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$, v.s.w.r. at output < 2, intermodulation factor = -30dB, $T_{amb} = 25^\circ\text{C}$				
	$f = 200\text{MHz}$, $f_p = 202\text{MHz}$,				
	$f_q = 205\text{MHz}$,				
	$f_{(2q-p)} = 208\text{MHz}$ (channel 9)	130	150	-	mW
	$f = 800\text{MHz}$, $f_p = 798\text{MHz}$,				
	$f_q = 802\text{MHz}$,				
	$f_{(2q-p)} = 806\text{MHz}$ (channel 62)	70	90	-	mW

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POWER OUTPUT TEST CIRCUIT (f=200MHz)



D1180

L_1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.

L_2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.

L_3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.

L_4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

ADJUSTMENT OF TEST CIRCUIT

Basis of adjustment

Intermodulation distortion at $d_{im} = -30\text{dB}$ is caused by clipping in h.f. output current and voltage.

The maximum undistorted output power is attained when

- a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek})/I_C$$

Where V_{cek} is the high frequency knee voltage

- b) The h.f. collector current is as low as possible; this occurs if

$$-C_{load} = +C_{oe}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input.

Experimentally obtained values of R_{load} and C_{load} , for maximum output power at an intermodulation factor of -30dB, are:

$$R_{load} = 220\Omega, C_{load} = -5.6\text{pF}$$

In this case 4pF are provided by C_{oe} of the transistor itself and 1.6pF by the mounting system, with the boron nitride washer between the transistor and the chassis.

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

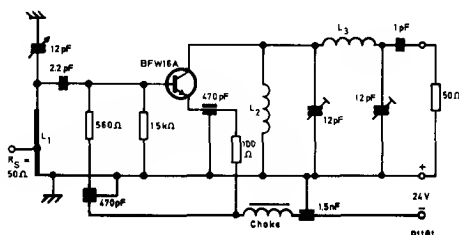
BFW16A

ADJUSTMENT OF TEST CIRCUIT (contd.)

Procedure

1. Remove the transistor and connect a dummy, consisting of a 220Ω resistor in parallel with a 5.6pF capacitor, between the collector and the emitter connections of the output circuit.
2. Tune and match the output circuit for zero reflection at 205MHz (i.e., v.s.w.r. = 1).
3. Replace the dummy by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L_2 .

POWER OUTPUT TEST CIRCUIT ($f = 800\text{MHz}$)



$L_1 = 25 \times 7 \times 0.85\text{mm}$ silver plated copper strip, input tap at 5mm from earth.

$L_2 = 13$ turns of 0.6mm enamelled copper wire, int. dia. 8mm .

$L_3 = 1.5$ turns of 1.3mm copper wire, int. dia. 8mm .

ADJUSTMENT OF TEST CIRCUIT

At 800MHz a dummy cannot be used to adjust for optimum collector load, because at these frequencies the impedance transformations of the dummy are too high.

A small signal with a frequency of the midchannel 802MHz is fed to the input. The signal is increased until clipping occurs, that is until the output power no longer increases linearly with increasing input signal. Care should be taken not to allow the voltage swing to exceed the V_{CER} value as this may result in the destruction of the transistor by second breakdown.

The output circuit is then tuned to eliminate clipping.

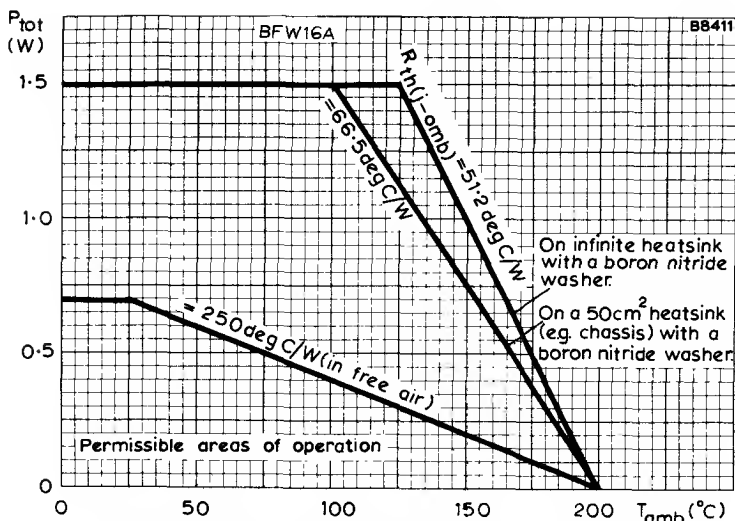
The output P_o is given by

$$P_o = I_C(V_{\text{CE}} - V_{\text{cek}})/2 = 480\text{mW}$$

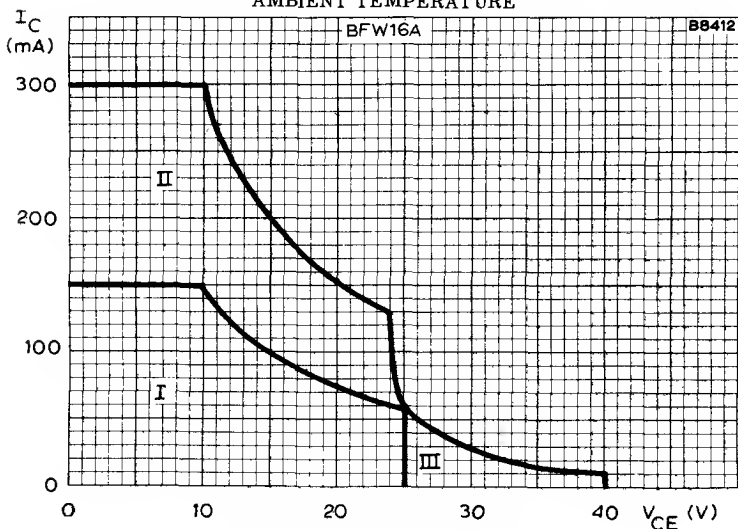
where V_{cek} is the high frequency knee voltage

Keeping the input signal as small as possible at $P_o = 480\text{mW}$, the output circuit is adjusted for minimum intermodulation. The input circuit is then adjusted for maximum gain and good bandpass curve. The v.s.w.r. is found to be ≤ 2 over the whole channel.

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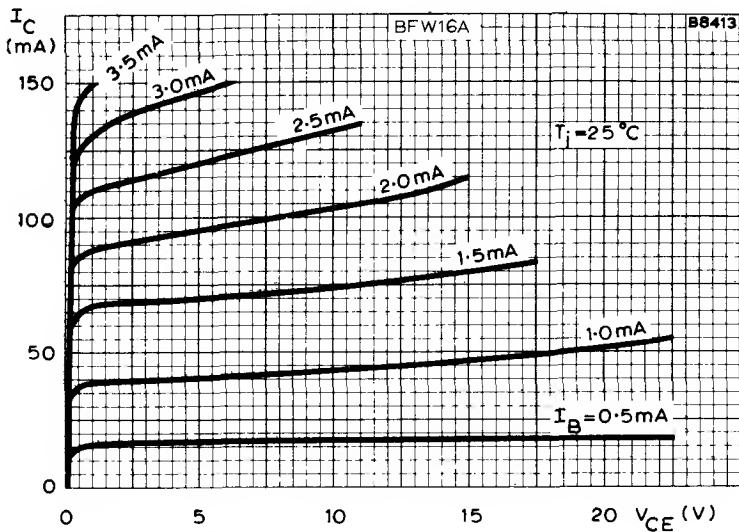


MAXIMUM PERMISSIBLE TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

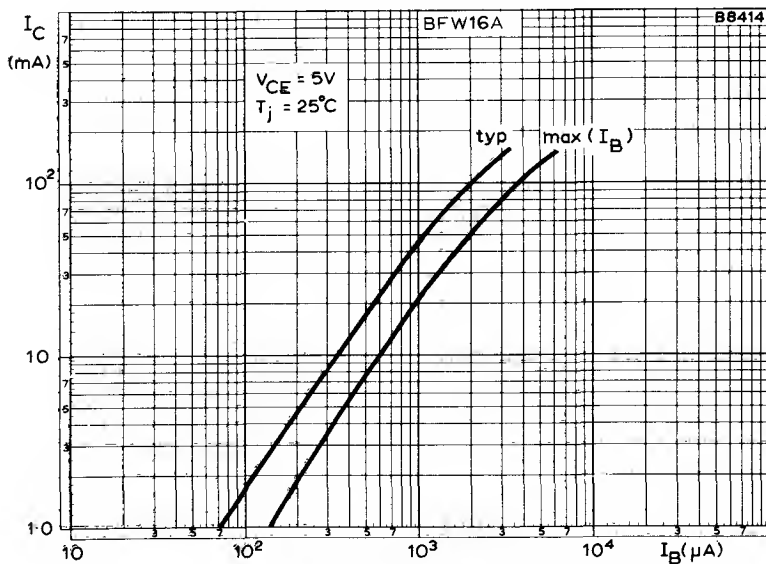


AREAS OF SAFE OPERATION

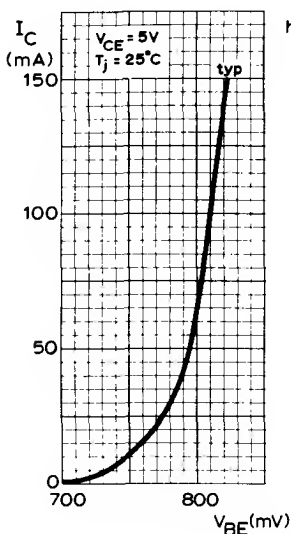
- I. D.C. and A.C. operation is allowed under all base-emitter conditions, provided no limiting values are exceeded.
- II. Operation is allowed under all base-emitter conditions at $f \geq 1\text{MHz}$, provided no limiting values are exceeded.
- III. Operation is allowed under pulse conditions, provided the transistor is cut-off, $R_{BE} \leq 50\Omega$, and $f \geq 1\text{MHz}$.



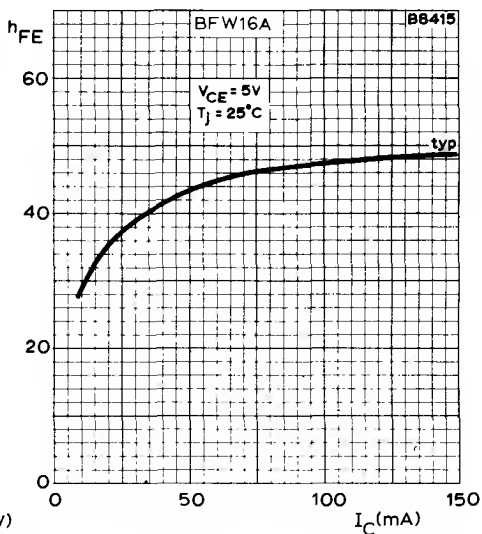
TYPICAL OUTPUT CHARACTERISTICS



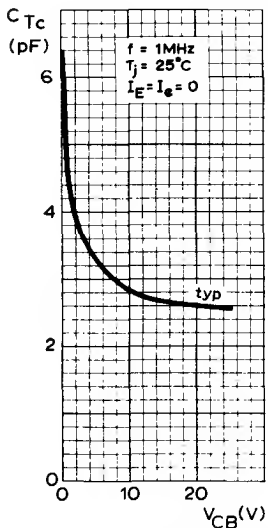
TRANSFER CHARACTERISTICS



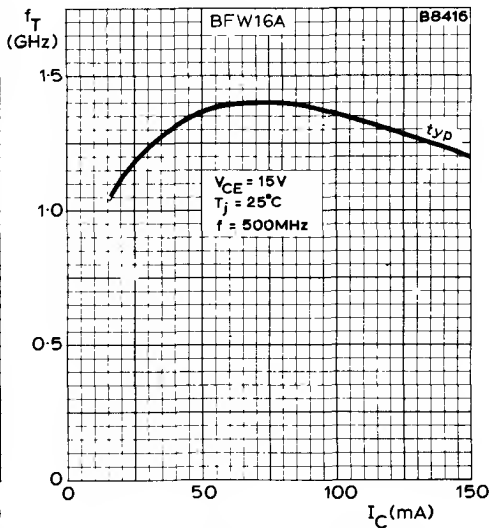
Typical mutual characteristics



Typical static forward current transfer ratio versus collector current



Typical collector capacitance versus collector-base voltage



Typical transition frequency versus collector current

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFW16A

APPLICATION INFORMATION

Performance of channel and band amplifiers

Frequency range	channel 4 61-68	channel 9 202-209	channel 55 742-750	band I 47-68	band II 87.5-108	band III 174-230	MHz
Transistor used in:							
final stage	BFW16A	BFW16A	BFW16A	BFW16A	BFW16A	BFW16A	
driver stage		BFW16A	BFW16A			BFW16A	
second stage			BFY90				
first stage	BFY90	BFY90	BFY90	BFY90	BFY90	BFY90	
Output power at:							
$d_{im} = -30\text{dB}$	150*	150*	100				mW
$d_{im} = -50\text{dB}$					30		mW
$d_{im} = -60\text{dB}$				10		10	mW
Power gain	50	44	26.5	51	43	39	dB
Noise figure	7	6	8	6.0-6.5	6.5	6.5	dB
V.S.W.R. over the whole channel or band							
for the input	<2	<2	<2	<2	<2	<2	
for the output	<2	<2	<2	<2	<2	<2	
Load impedance	30	30	50	30	30	30	Ω
Source impedance	60	60	50	60	60	60	Ω

* $V_o = 2.2\text{V}$ over $R_L = 30\Omega$ or

$V_o = 3\text{V}$ over $R_L = 60\Omega$

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BFW17A

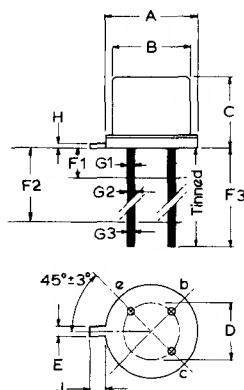
N-P-N silicon planar epitaxial, multi-emitter transistor with extremely good inter-modulation properties and a high powergain. The BFW17A is primarily intended for the final and driver stages of channel and band aerial amplifiers with high output in bands I, II and III (40-230MHz). Encapsulated in a metal TO-39 envelope with the collector connected to the case. The BFW17A is a ruggedized version of the BFW17, which it succeeds.

QUICK REFERENCE DATA

V_{CBOM} max.	40	V
V_{CEO} max.	25	V
I_{CM} max. ($f > 1.0\text{MHz}$)	300	mA
P_{tot} max. ($T_{case} \leq 125^{\circ}\text{C}$)	1.5	W
T_j max.	200	$^{\circ}\text{C}$
f_T typ. ($I_C = 150\text{mA}$, $V_{CE} = 15\text{V}$, $f = 500\text{MHz}$)	1.1	GHz
$-C_{re}$ typ. ($I_C = 10\text{mA}$, $V_{CE} = 15\text{V}$, $f = 1.0\text{MHz}$)	1.7	pF
G_p typ. ($I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$, $f = 200\text{MHz}$)	16	dB
P_o typ. ($I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$, $f = 200\text{MHz}$)	150	mW

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



Collector connected to case

Accessories available:
56218, 56245, 56265

Millimetres

	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	40	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	40	V
V_{CEO} max. ($I_C = 10mA$)	25	V
V_{EBO} max.	2.0	V
I_C max.	150	mA
I_{CM} max. ($f > 1.0MHz$)	300	mA
P_{tot} max. ($T_{case} \leq 125^\circ C$)	1.5	W

Temperature

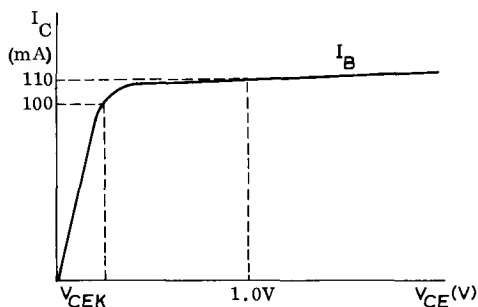
T_{stg} min.	-65	$^\circ C$
T_{stg} max.	200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	in free air	250	degC/W
$R_{th(j-case)}$		50	degC/W
$R_{th(case-h)}$	when mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 20V$, $I_E = 0$, $T_j = 150^\circ C$	-	-	20	μA
V_{CEK}	Collector-emitter knee voltage $I_C = 100mA$, $I_B =$ the value for which $I_C = 110mA$, at $V_{CE} = 1.0V$	-	-	0.75	V



Mullard

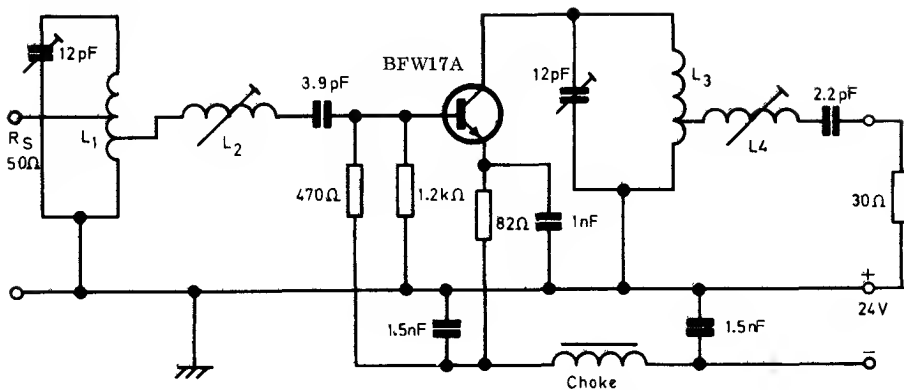
N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BFW17A

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio				
	$I_C = 50\text{mA}$, $V_{CE} = 5.0\text{V}$	25	-	-	
	$I_C = 150\text{mA}$, $V_{CE} = 5.0\text{V}$	25	-	-	
f_T	Transition frequency				
	$I_C = 150\text{mA}$, $V_{CE} = 15\text{V}$, $f = 500\text{MHz}$	-	1.1	-	GHz
C_{Tc}	Collector capacitance				
	$V_{CB} = 15\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	-	4.0	pF
$-C_{re}$	Feedback capacitance				
	$I_C = 10\text{mA}$, $V_{CE} = 15\text{V}$, $f = 1.0\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	-	1.7	-	pF
G_p	Power gain (not neutralised)				
	$I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$, $f = 200\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	-	16	-	dB
Intermodulation characteristics					
P_o	Output power (see test circuit)	-	150	-	mW
	$I_C = 70\text{mA}$, $V_{CE} = 18\text{V}$, $f = 200\text{MHz}$, intermodulation factor = -30dB, v.s.w.r. at output < 2.0, $T_{amb} = 25^\circ\text{C}$				
	$f_p = 202\text{MHz}$, $f_q = 205\text{MHz}$, $f_{(2q-p)} = 208\text{MHz}$ (channel 9)				

POWER OUTPUT TEST CIRCUIT (f = 200MHz)



D1180

L_1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.

L_2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.

L_3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.

L_4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

ADJUSTMENT OF TEST CIRCUIT

Basis of adjustment

Intermodulation distortion at $d_{im} = -30dB$ is caused by clipping in h.f. output current and voltage.

The maximum undistorted output power is attained when

a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek}) / I_C$$

Where V_{cek} is the high frequency knee voltage

b) The h.f. collector current is as low as possible; this occurs if

$$-C_{load} = +C_{oe}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input.

Experimentally obtained values of R_{load} and C_{load} , for maximum output power at an intermodulation factor of -30dB, are:

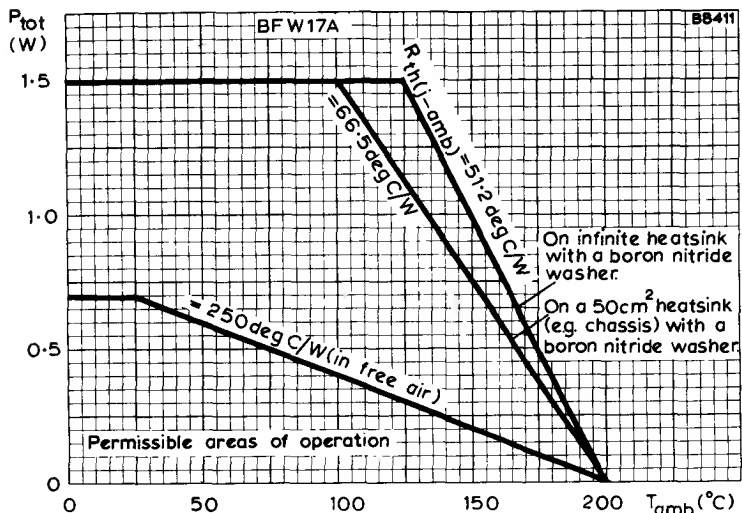
$$R_{load} = 220\Omega, C_{load} = -5.6pF$$

In this case 4pF are provided by C_{oe} of the transistor itself and 1.6pF by the mounting system, with the boron nitride washer between the transistor and the chassis.

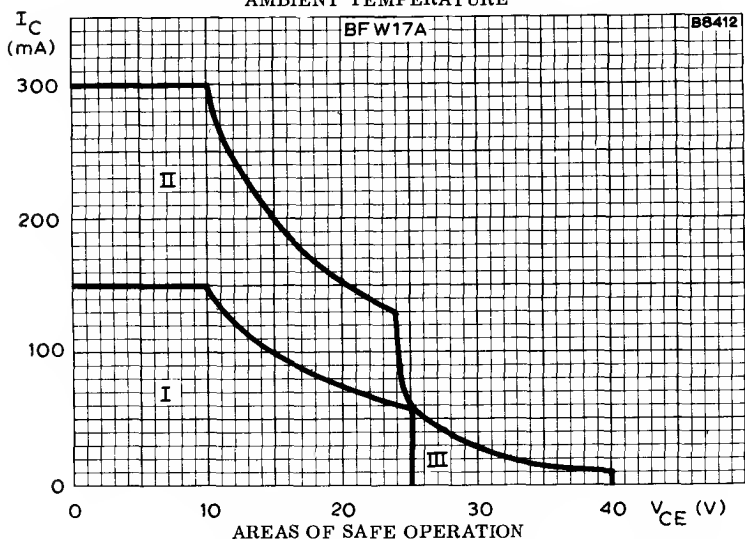
ADJUSTMENT OF TEST CIRCUIT (contd.)

Procedure

1. Remove the transistor and connect a dummy, consisting of a 220Ω resistor in parallel with a 5.6pF capacitor, between the collector and the emitter connections of the output circuit.
2. Tune and match the output circuit for zero reflection at 205MHz (i.e., v.s.w.r. = 1).
3. Replace the dummy by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L_2 .

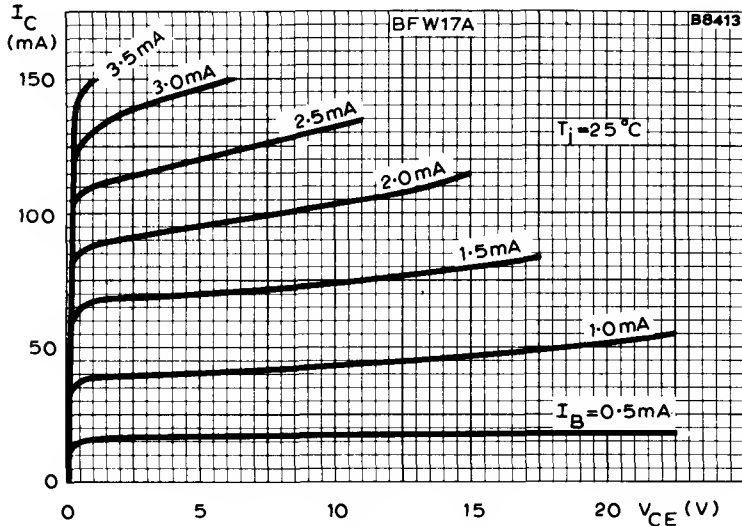


MAXIMUM PERMISSIBLE TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

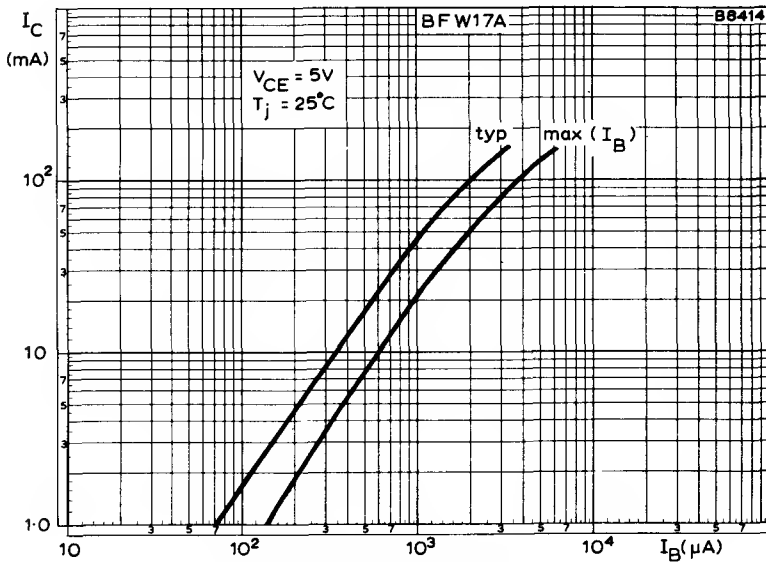


AREAS OF SAFE OPERATION

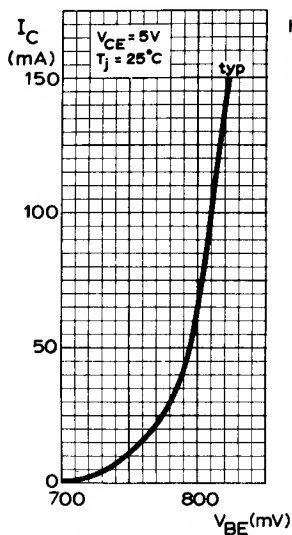
- I. D.C. and A.C. operation is allowed under all base-emitter conditions, provided no limiting values are exceeded.
- II. Operation is allowed under all base-emitter conditions at $f \geq 1\text{MHz}$, provided no limiting values are exceeded.
- III. Operation is allowed under pulse conditions, provided the transistor is cut-off, $R_{BE} \leq 50\Omega$ and $f \geq 1\text{MHz}$.



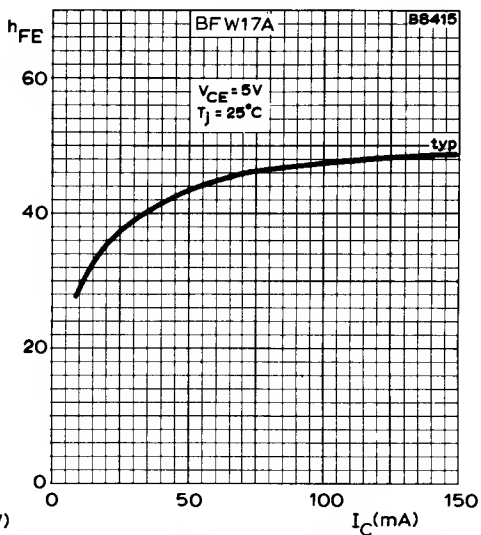
TYPICAL OUTPUT CHARACTERISTICS



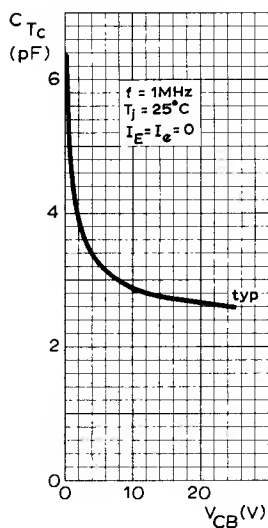
TRANSFER CHARACTERISTICS



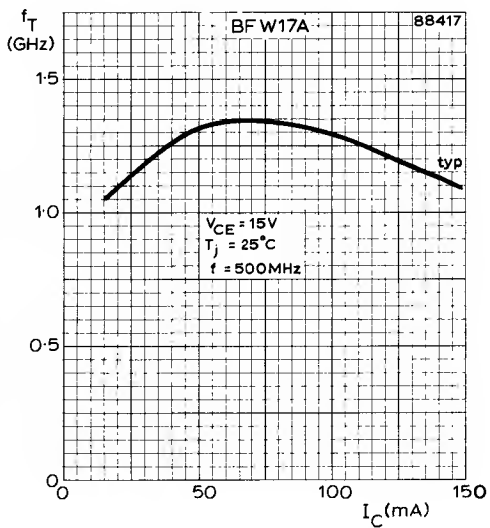
Typical mutual characteristics



Typical static forward current transfer ratio versus collector current



Typical collector capacitance versus collector-base voltage



Typical transition frequency versus collector current

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFW30

N-P-N silicon planar epitaxial, multi-emitter transistor with extremely good intermodulation properties and a high power gain. The BFW30 is primarily intended for wideband vertical amplifiers in high speed oscilloscopes, wideband aerial amplifiers (40-860MHz) and television distribution amplifiers. Encapsulated in a metal TO-72 envelope with all electrodes insulated from the case. Shield lead connected to case.

QUICK REFERENCE DATA

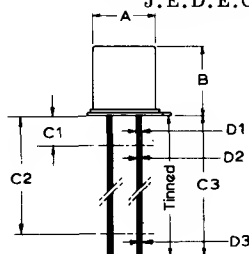
V _{CBOM} max.	20	V	
V _{CEO} max.	10	V	
I _{CM} max. (f>1.0MHz)	100	mA	
P _{tot} max. (T _{amb} ≤25 ^o C)	250	mW	
T _j max.	200	°C	
f _T typ. (I _C =50mA, V _{CE} =5.0V, f=500MHz)	1.6	GHz	
-C _{re} typ. (I _C =2.0mA, V _{CE} =5.0V, f=1.0MHz)	0.8	pF	
G _p typ. (I _C =30mA, V _{CE} =5.0V) f=200MHz	21	dB	
	f=800MHz	7.5	dB
d _{im} typ. (I _C =30mA, V _{CE} =6.0V, R _L =37.5Ω, f _p =183MHz, V _o =100mV f _q =200MHz, V _o =100mV f _(2q-p) =217MHz)	-60	dB	

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB4-3

J.E.D.E.C. TO-72

Millimetres



Viewed from underside

	Min.	Nom.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections

1. Emitter
3. Collector

2. Base
4. Shield
(connected to case)

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	20	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	20	V
V_{CEO} max. ($I_C = 10mA$)	10	V
V_{EBO} max.	2.5	V
I_C max.	50	mA
I_{CM} max. ($f > 1.0MHz$)	100	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	250	mW

Temperature

T_{stg} min.	-65	$^\circ C$
T_{stg} max.	200	$^\circ C$
T_j max. operating	200	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	0.7	degC/mW
$R_{th(j-case)}$	0.5	degC/mW

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 10V$, $I_E = 0$	-	-	50	nA
h_{FE}	Static forward current transfer ratio $I_C = 25mA$, $V_{CE} = 5.0V$	25	-	-	
	$I_C = 50mA$, $V_{CE} = 5.0V$	25	-	-	
f_T	*Transition frequency $I_C = 50mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	1.6	-	GHz
C_{tc}	**Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	-	1.5	pF
$-C_{re}$	*Feedback capacitance $V_{CE} = 5.0V$, $I_C = 2.0mA$, $f = 1.0MHz$	-	0.8	-	pF

*Fourth lead (case) grounded

**Fourth lead (case) not connected

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFW30

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
G_p	*Power gain (not neutralised)				
	$I_C = 30\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 200\text{MHz}$	19	21	-	dB
	$f = 800\text{MHz}$	-	7.5	-	dB
N	*Noise figure				
	$V_{CE} = 5.0\text{V}$, $I_C = 2.0\text{mA}$, $f = 500\text{MHz}$, $R_S = 50\Omega$	-	-	5.0	dB
d_{im}	*Intermodulation distortion (see fig. 1)				
	$I_C = 30\text{mA}$, $V_{CE} = 6.0\text{V}$, $R_L = 37.5\Omega$,				
	$f_p = 183\text{MHz}$, $V_o = 100\text{mV}$				
	$f_q = 200\text{MHz}$, $V_o = 100\text{mV}$				
	$f_{(2q-p)} = 217\text{MHz}$	-	-60	-	dB

*Fourth lead (case) grounded

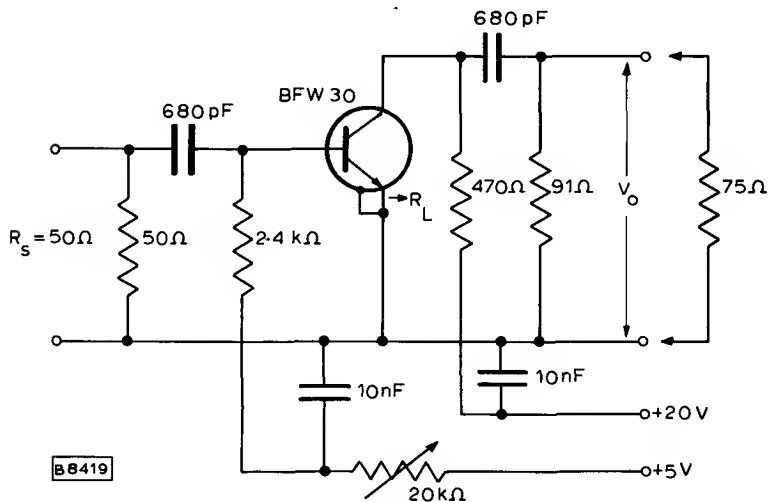
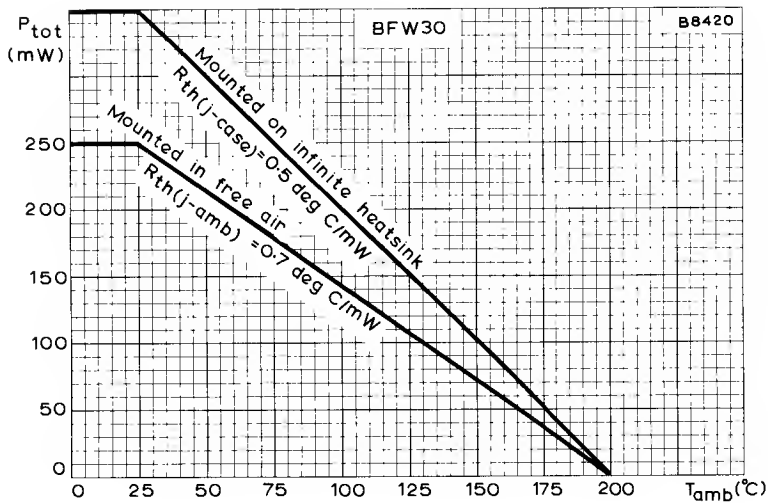
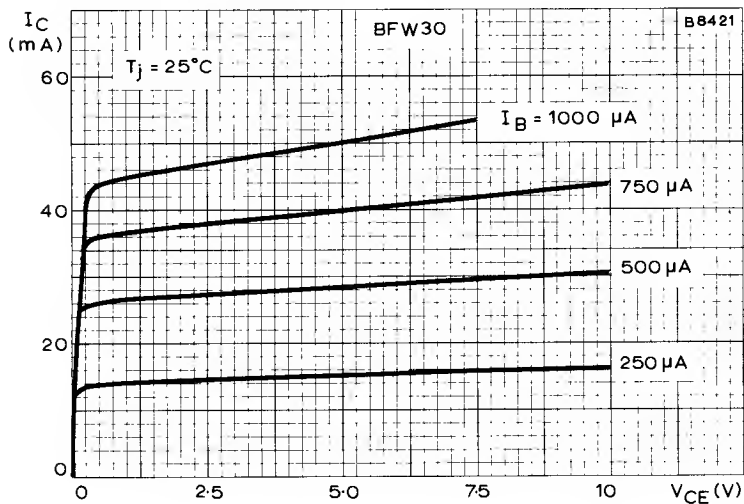


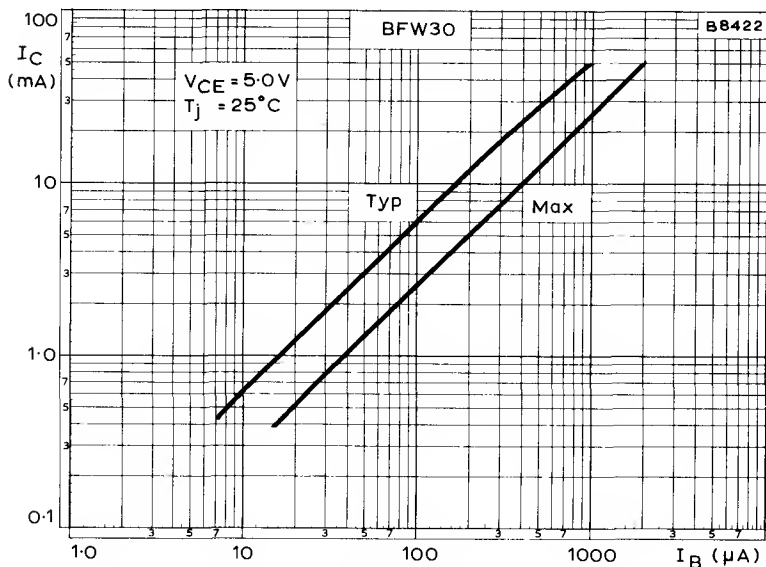
Fig. 1



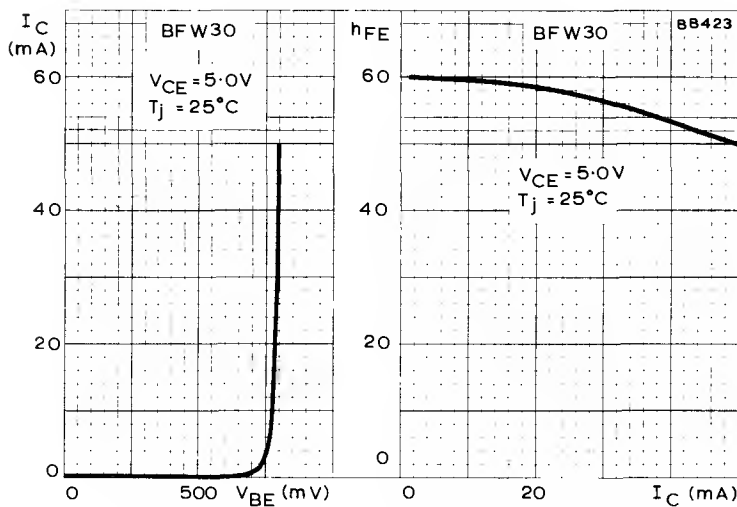
MAXIMUM PERMISSIBLE TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



TYPICAL OUTPUT CHARACTERISTICS

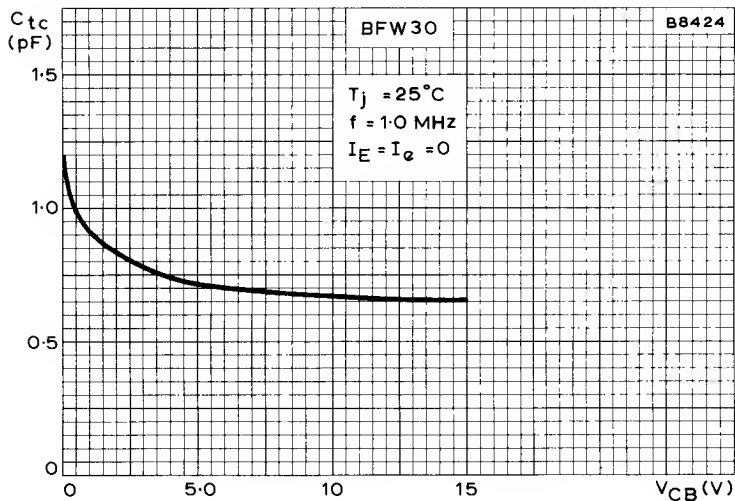


TRANSFER CHARACTERISTICS

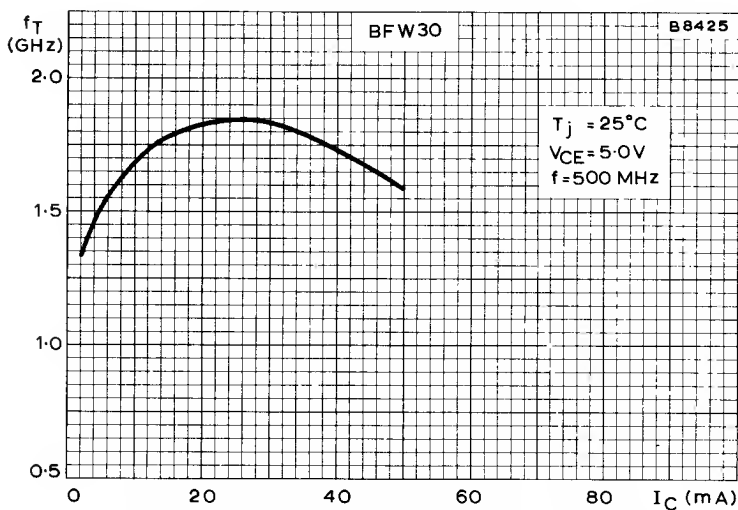


Typical mutual characteristic

Typical static forward current transfer ratio versus collector current



TYPICAL COLLECTOR CAPACITANCE PLOTTED AGAINST
COLLECTOR-BASE VOLTAGE



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST
COLLECTOR CURRENT

N-CHANNEL SILICON FIELD EFFECT TRANSISTOR

BFW61

The BFW61 is an n-channel silicon epitaxial planar junction field effect transistor for general purpose industrial applications.

QUICK REFERENCE DATA

V_{DSS} max.		±25	V
V_{GSO} max.		-25	V
$V_{(P)GS}$ max.		8.0	V
I_{DSS} ($V_{DS}=15V$, $V_{GS}=0$)	min.	2.0	mA
	max.	20	mA
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)		300	mW
y_{fs} min.		1.6	mmho
$-C_{rs}$ max.		2.0	pF

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72

B.S. 3934 SO-12A/SB4-3

For details see page 4.



Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DSS} max.	Drain-source voltage	± 25	V
V_{DGO} max.	Drain-gate voltage	25	V
V_{GSO} max.	Gate-source voltage	-25	V
I_D max.	Drain current	20	mA
I_G max.	Gate current	10	mA
P_{tot} max.	Total device dissipation ($T_{amb} \leq 25^\circ\text{C}$)	300	mW

Temperature

T_{stg}	Storage temperature range	-65 to +200	$^\circ\text{C}$
T_j max.	Max. junction temperature	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.59	degC/mW
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Max.	
$-I_{GSS}$	Gate cut-off current			
	$-V_{GS} = 20\text{V}, V_{DS} = 0$	-	1.0	nA
	$-V_{GS} = 20\text{V}, V_{DS} = 0, T_j = 150^\circ\text{C}$	-	1.0	μA
I_{DSS}	*Drain current			
	$V_{DS} = 15\text{V}, V_{GS} = 0$	2.0	20	mA
$-V_{GS}$	Gate-source voltage			
	$I_D = 200\mu\text{A}, V_{DS} = 15\text{V}$	0.5	7.5	V
$-V_{(P)GS}$	Gate-source cut-off voltage			
	$I_D = 1.0\text{nA}, V_{DS} = 15\text{V}$	-	8.0	V

* Measured under pulse conditions.

N-CHANNEL SILICON FIELD EFFECT TRANSISTOR

BFW61

ELECTRICAL CHARACTERISTICS (cont'd)

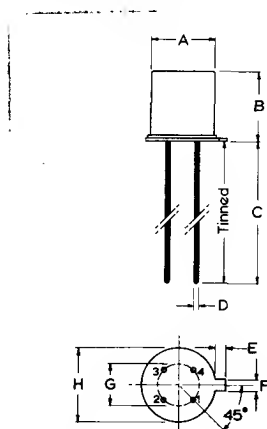
Small signal y-parameters		Min.	Max.
Common source, $V_{DS} = 15V$, $V_{GS} = 0$			
y_{fs}	Forward transfer admittance $f = 1.0kHz$	2.0	6.5 mmho
y_{os}	Output admittance $f = 1.0kHz$	-	85 μ mho
C_{is}	Input capacitance $f = 1.0MHz$	-	6.0 pF
$-C_{rs}$	Reverse transfer capacitance $f = 1.0MHz$	-	2.0 pF
y_{fs}	Forward transfer admittance $f = 10MHz$	1.6	- mmho

SOLDERING AND WIRING RECOMMENDATIONS

1. Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for a time of up to 10 seconds at least 1.5mm from the seal. At an iron temperature of 245°C to 400°C the maximum soldering time is 5 seconds at least 5mm from the seal.
2. These devices may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a device mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

OUTLINE, DIMENSIONS AND CONNECTIONS

Conforms to J.E.D.E.C. TO-72



Millimetres

	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Pinning

1. Source
2. Drain
3. Gate
4. Shield lead connected to case

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

BFX29
BFX87
BFX88

BFX29 is also available to BS9365—F010

P-N-P silicon planar epitaxial transistors for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

QUICK REFERENCE DATA

	BFX29	BFX87	BFX88	
$-V_{CBO}$ max.	60	50	40	V
$-V_{CEO}$ max.	60	50	40	V
$-I_{CM}$ max.				600 mA
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)				600 mW
h_{FE} ($-I_C = 10mA, -V_{CE} = 10V$)				
min.	50	40	40	
typ.	125	125	125	
f_T min. ($-I_C = 50mA, -V_{CE} = 10V$, $f = 100MHz$)				100 MHz

Unless otherwise stated, data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

The collector is electrically connected to the envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BFX29	BFX87	BFX88	
$-V_{CBO}$ max.	60	50	40	V
$-V_{CEO}$ max.	60	50	40	V
$-V_{EBO}$ max.	5.0	4.0	4.0	V
$-I_C$ max.			600	mA
$-I_{CM}$ max.			600	mA
I_{EM} max.			600	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)			600	mW

Temperature

T_{stg} range	-65 to +200	$^\circ C$
T_j max.	+200	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	292	degC/W
-----------------	-----	--------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 60V, I_E = 0$	BFX29	-	1.0	500 nA
	$-V_{CB} = 50V, I_E = 0$	BFX87	-	1.0	500 nA
	$-V_{CB} = 40V, I_E = 0$	BFX88	-	1.0	500 nA
	$-V_{CB} = 50V, I_E = 0$	BFX29	-	0.5	50 nA
	$-V_{CB} = 40V, I_E = 0$	BFX87	-	0.5	50 nA
	$-V_{CB} = 30V, I_E = 0$	BFX88	-	0.5	50 nA
	$-V_{CB} = 50V, I_E = 0,$ $T_j = 100^\circ C$	BFX29	-	0.03	2.0 μA
	$-V_{CB} = 40V, I_E = 0,$ $T_j = 100^\circ C$	BFX87	-	0.03	2.0 μA
	$-V_{CB} = 30V, I_E = 0,$ $T_j = 100^\circ C$	BFX88	-	0.03	2.0 μA
$-I_{EBO}$	Emitter cut-off current				
	$-V_{EB} = 5.0V, I_C = 0$	BFX29	-	30	500 nA
	$-V_{EB} = 4.0V, I_C = 0$	BFX87, 88	-	2.0	500 nA
	$-V_{EB} = 3.0V, I_C = 0$	BFX29, 87, BFX88	-	1.0	100 nA

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

BFX29
BFX87
BFX88

ELECTRICAL CHARACTERISTICS (cont'd)

			Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio					
	$-I_C = 0.1\text{mA}$, $-V_{CE} = 10\text{V}$	BFX29	20	90	-	
	$-I_C = 1.0\text{mA}$, $-V_{CE} = 10\text{V}$	BFX29, 87, BFX88	40	105	-	
	$-I_C = 10\text{mA}$, $-V_{CE} = 10\text{V}$	BFX29	50	125	-	
		BFX87, 88	40	125	-	
	$-I_C = 50\text{mA}$, $-V_{CE} = 10\text{V}$	BFX29	50	125	-	
	$-I_C = 150\text{mA}$, $-V_{CE} = 10\text{V}$	BFX29, 87, BFX88	40	90	-	
	$-I_C = 500\text{mA}$, $-V_{CE} = 10\text{V}$	BFX87, 88	25	40	-	
$-V_{CE(sat)}$	Collector-emitter saturation voltage					
	$-I_C = 150\text{mA}$, $-I_B = 15\text{mA}$		-	0.15	0.40	V
$-V_{BE(sat)}$	Base-emitter saturation voltage					
	$-I_C = 30\text{mA}$, $-I_B = 1.0\text{mA}$		-	0.77	0.90	V
	$-I_C = 150\text{mA}$, $-I_B = 15\text{mA}$		-	1.05	1.30	V
C_{tc}	Collector capacitance					
	$-V_{CB} = 10\text{V}$, $I_E = I_C = 0$, $f = 1.0\text{MHz}$		-	6.0	12	pF
C_{te}	Emitter capacitance					
	$-V_{EB} = 2.0\text{V}$, $I_C = I_E = 0$, $f = 1.0\text{MHz}$		-	18	30	pF
f_T	Transition frequency					
	$-I_C = 50\text{mA}$, $-V_{CE} = 10\text{V}$, $f = 100\text{MHz}$, $T_{amb} = 25^\circ\text{C}$		100	360	-	MHz

ELECTRICAL CHARACTERISTICS (cont'd)

Saturated switching times (see test circuits)

		Min.	Typ.	Max.	
t_{on}	Turn-on time	-	25	60	ns
t_{off}	Turn-off time	-	55	150	ns

h-parameters

Measured at $-I_C = 10\text{mA}$, $-V_{CE} = 10\text{V}$, $f = 1.0\text{kHz}$, $T_{amb} = 25^\circ\text{C}$

		Min.	Typ.	Max.	
h_{ie}	Input impedance	-	600	-	Ω
h_{re}	Voltage feedback ratio	-	1.50	-	$\times 10^{-4}$
h_{fe}	Forward current transfer ratio	-	155	-	
h_{oe}	Output admittance	-	104	-	μmho

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

TEST CIRCUITS

Saturated turn-on switching time

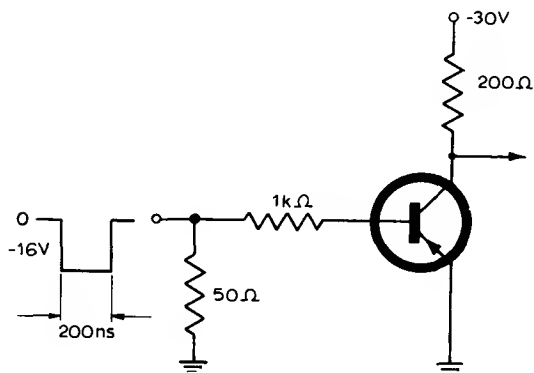


Fig. 1

Saturated turn-off switching time

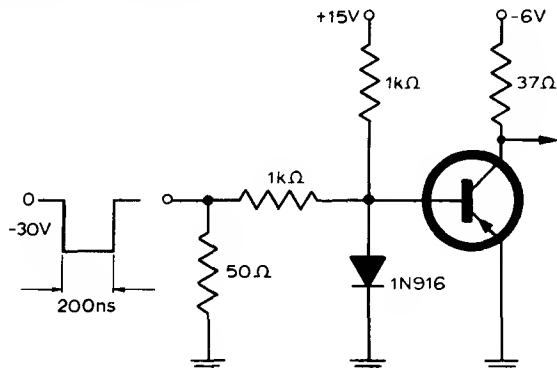
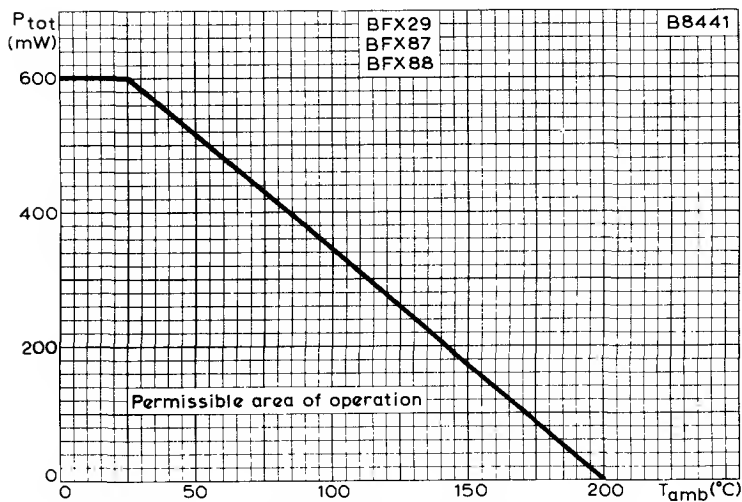
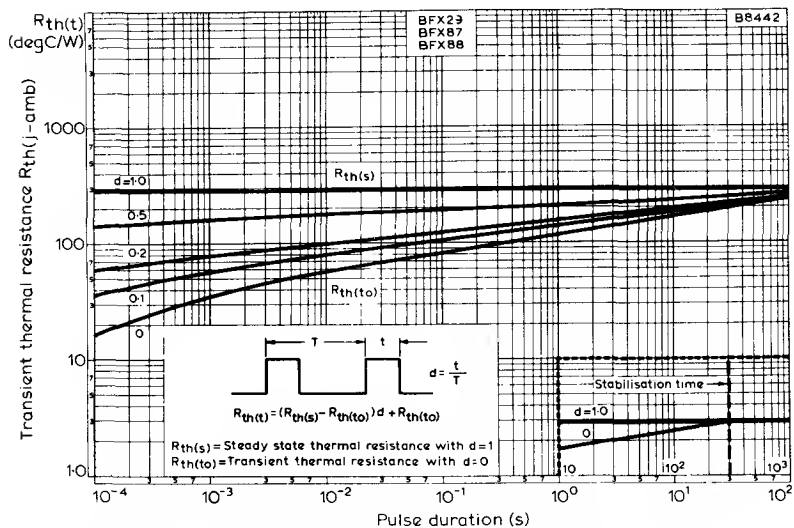


Fig. 2



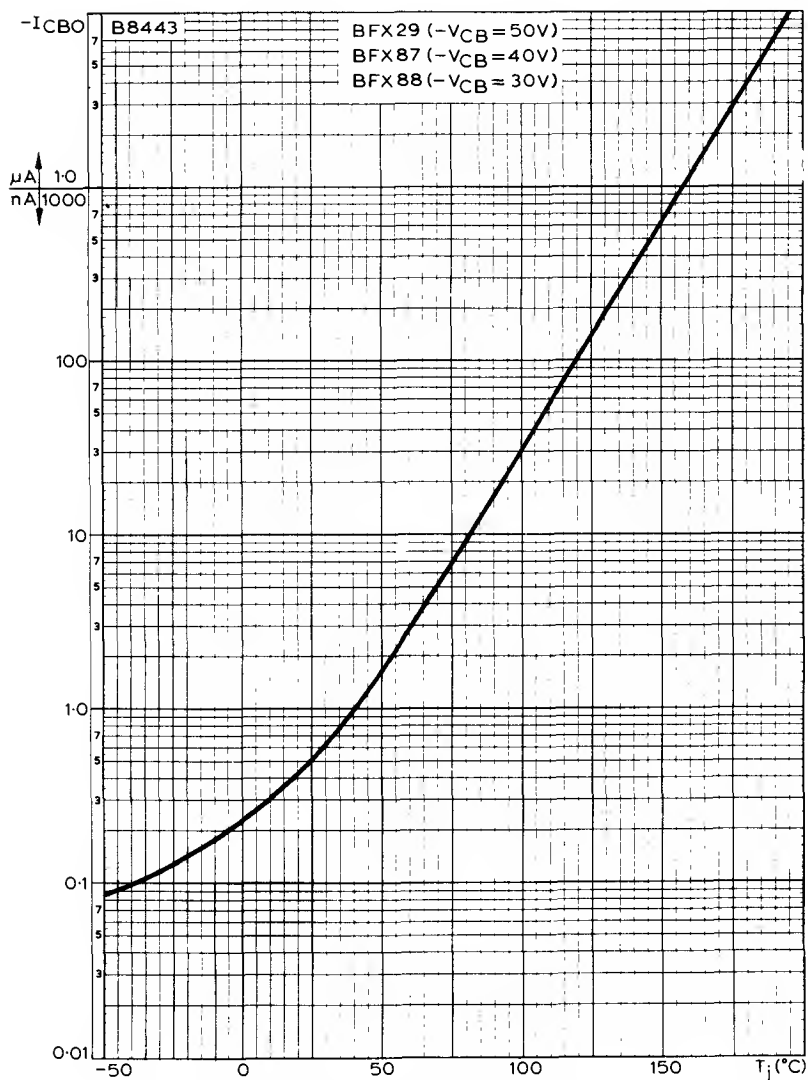
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS PLOTTED AGAINST PULSE DURATION

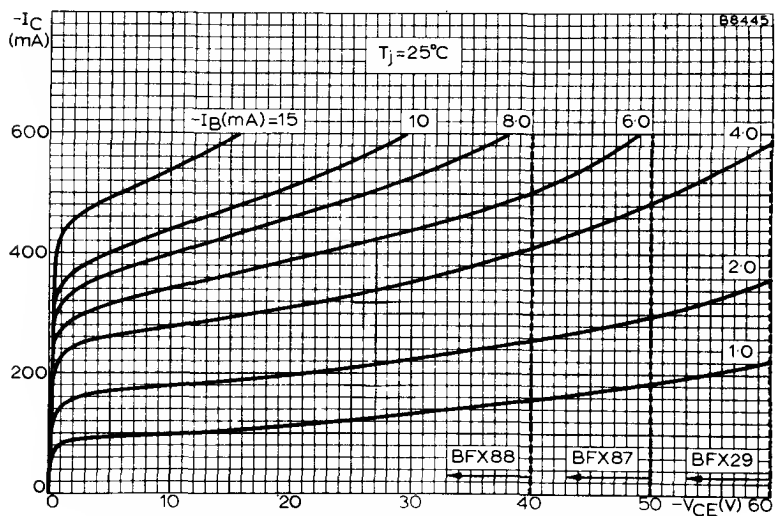
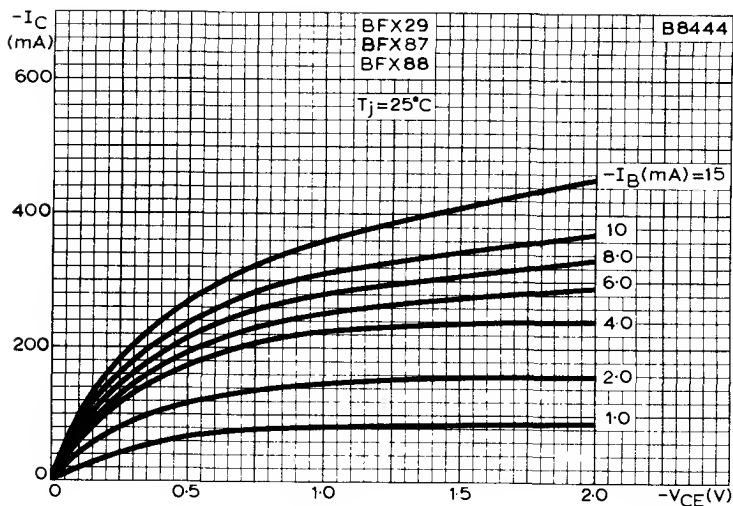
P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

BFX29
BFX87
BFX88



TYPICAL VARIATION OF COLLECTOR CUT-OFF CURRENT
WITH JUNCTION TEMPERATURE

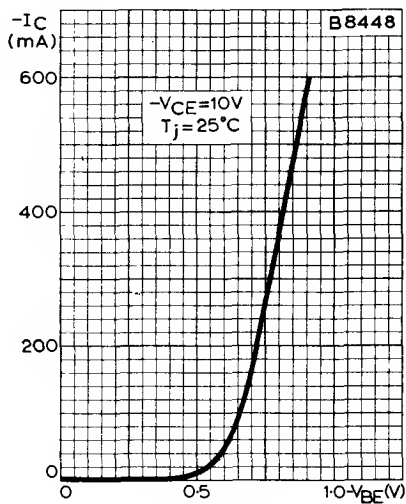
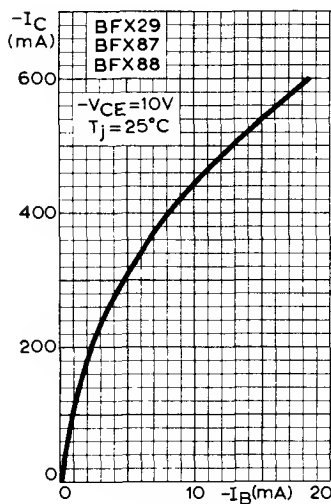
Mullard



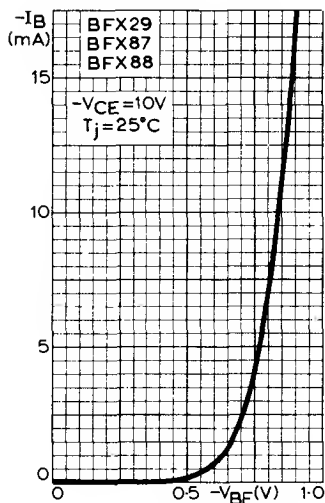
TYPICAL OUTPUT CHARACTERISTICS AT LOW AND HIGH
 COLLECTOR-EMITTER VOLTAGES

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

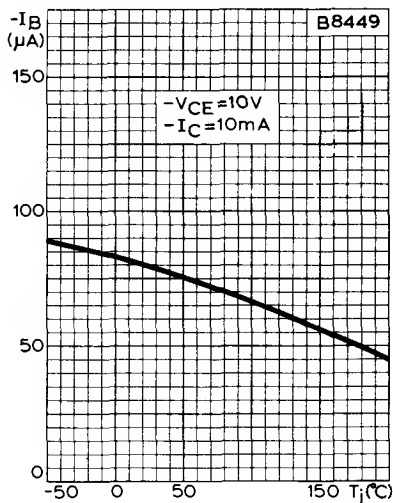
BFX29
BFX87
BFX88



TYPICAL TRANSFER AND MUTUAL CHARACTERISTICS

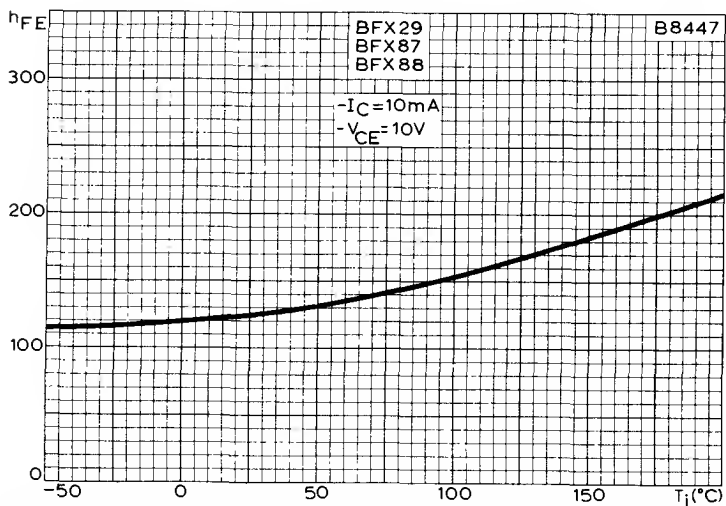
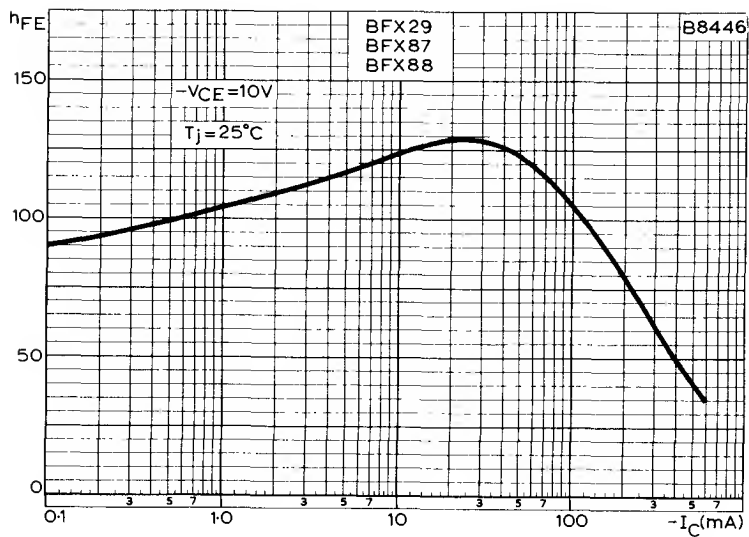


Typical input characteristic



Typical base current versus
junction temperature

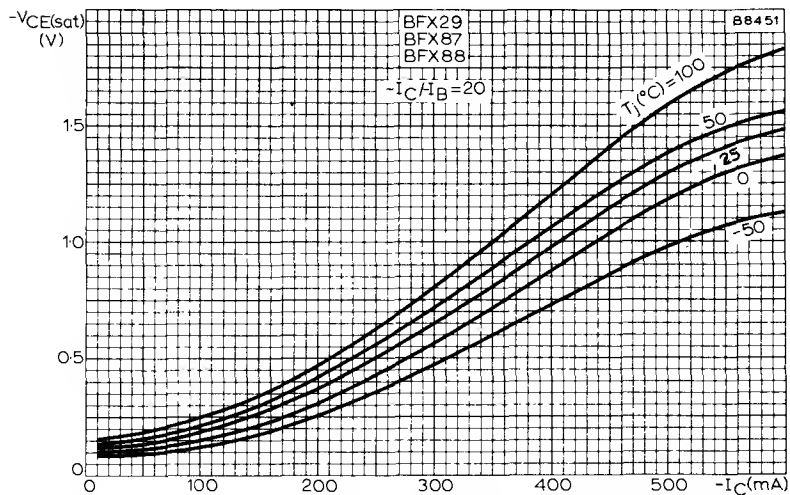
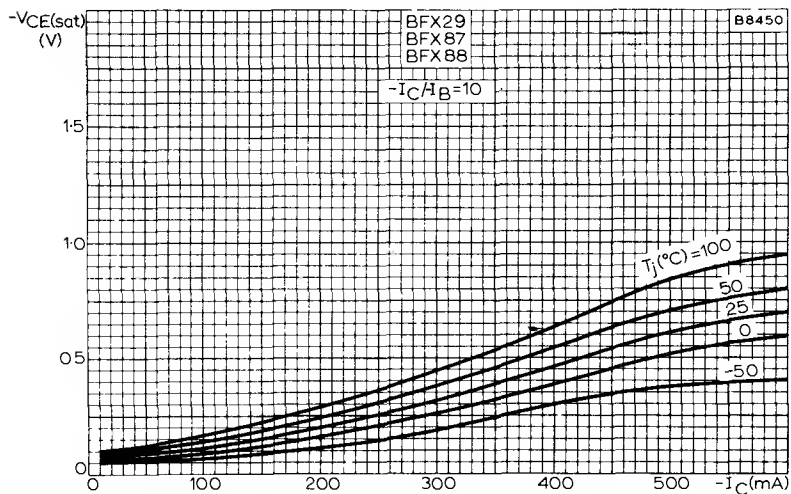
Mullard



TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH COLLECTOR CURRENT AND JUNCTION TEMPERATURE

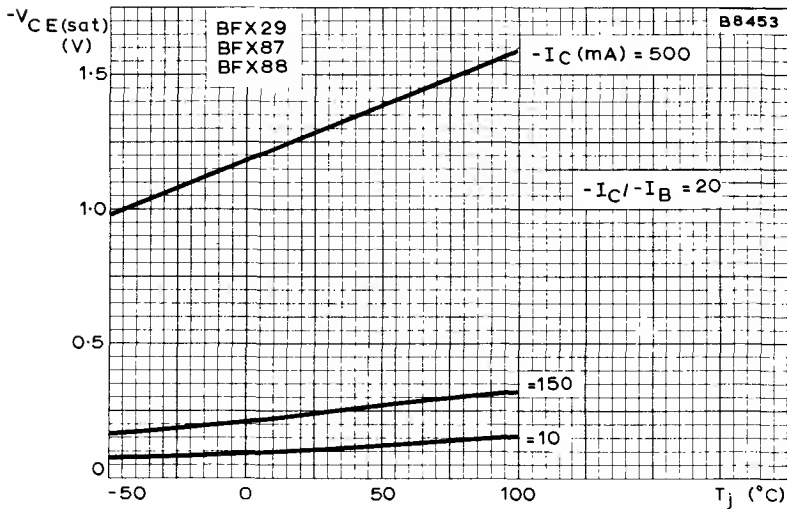
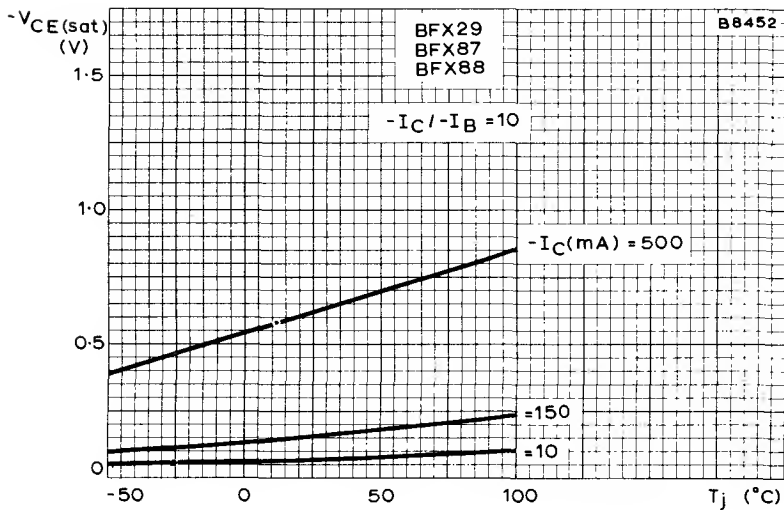
P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

BFX29
BFX87
BFX88

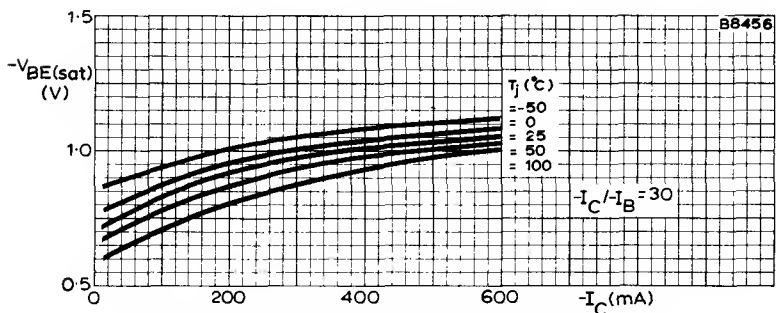
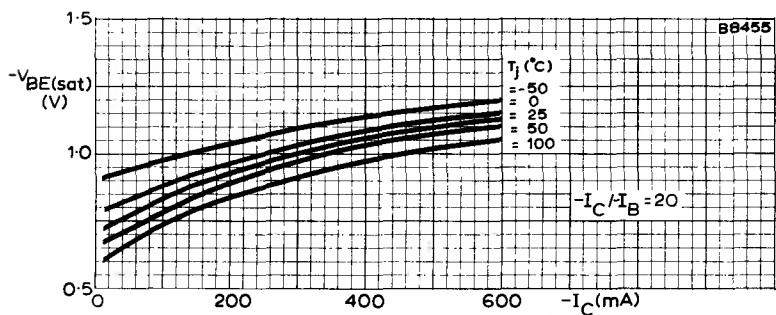
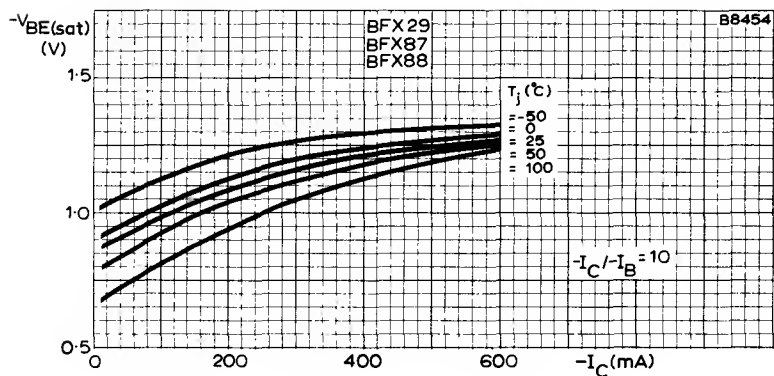


TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION
VOLTAGE WITH COLLECTOR CURRENT

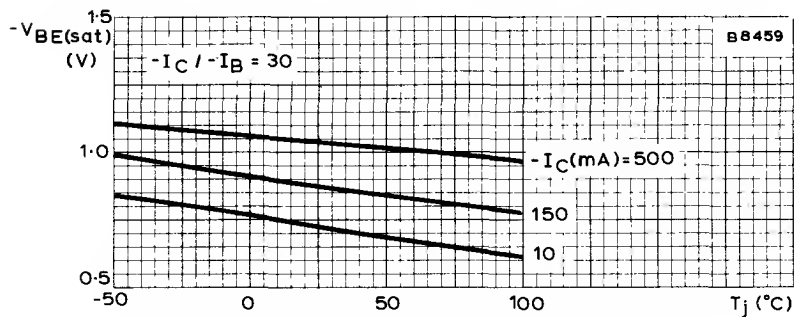
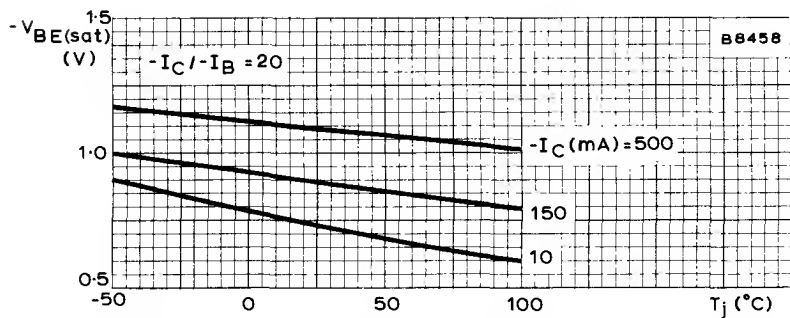
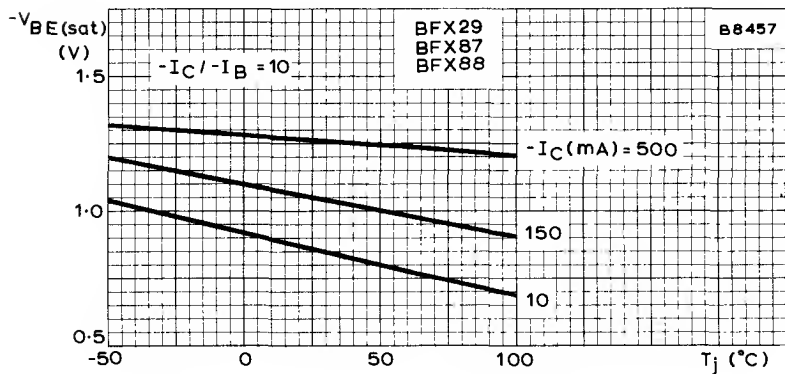
Mullard



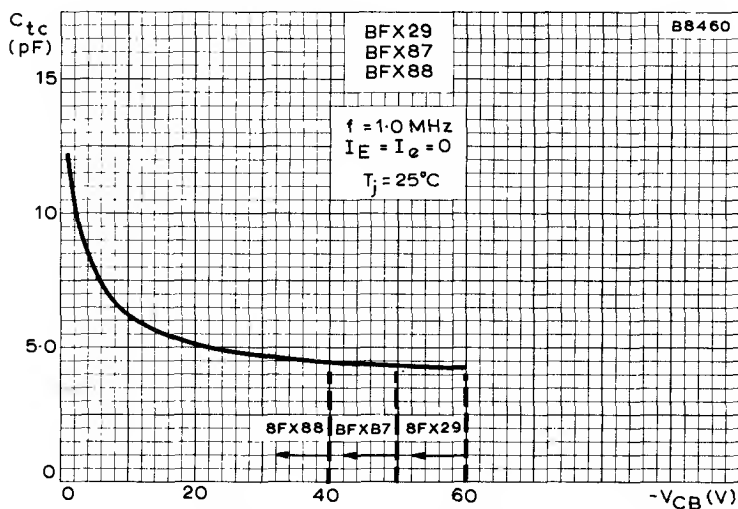
TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION
 VOLTAGE WITH JUNCTION TEMPERATURE



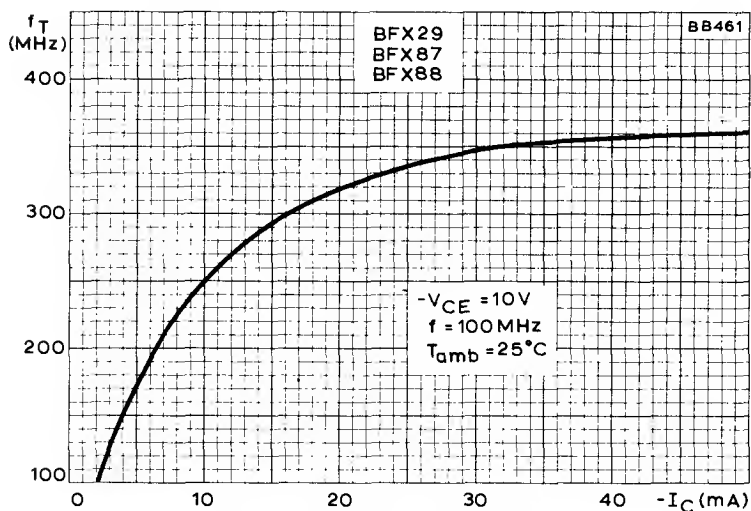
TYPICAL VARIATION OF BASE-EMITTER SATURATION
VOLTAGE WITH COLLECTOR CURRENT



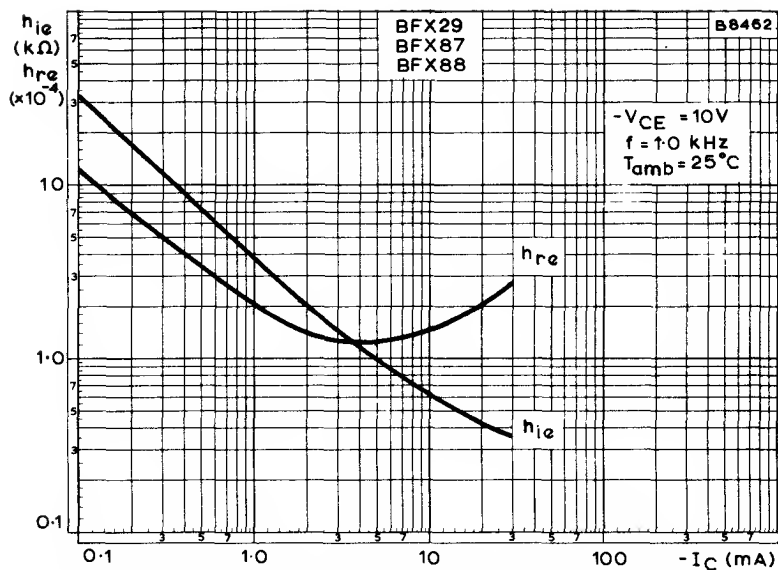
TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE WITH JUNCTION TEMPERATURE



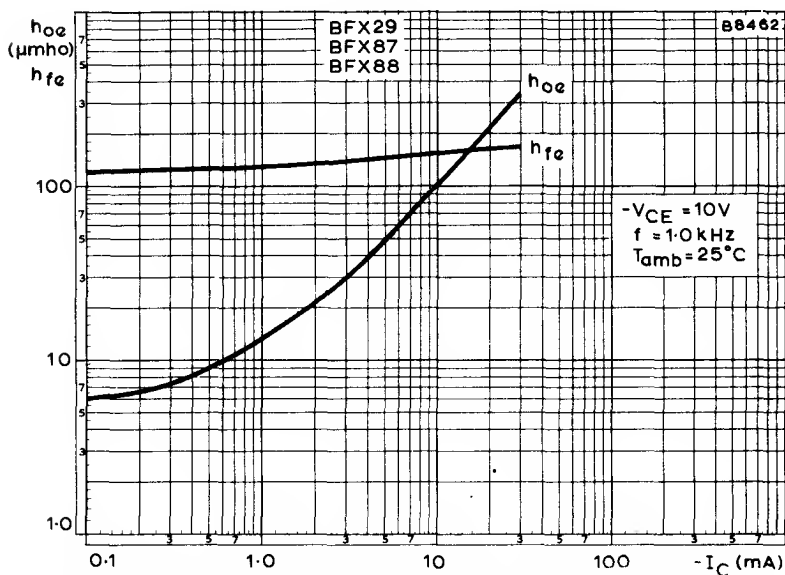
TYPICAL VARIATION OF COLLECTOR CAPACITANCE WITH
COLLECTOR-BASE VOLTAGE



TYPICAL VARIATION OF TRANSITION FREQUENCY
WITH COLLECTOR CURRENT



TYPICAL INPUT IMPEDANCE AND TYPICAL VOLTAGE FEEDBACK
 RATIO PLOTTED AGAINST COLLECTOR CURRENT



TYPICAL FORWARD CURRENT TRANSFER RATIO AND TYPICAL OUTPUT
 ADMITTANCE PLOTTED AGAINST COLLECTOR CURRENT

P-N-P SILICON PLANAR EPITAXIAL TRANSISTOR

BFX30

Also available to BS9365—F011

Silicon p-n-p planar epitaxial transistor intended for switching applications.
Encapsulated in TO-5 envelope with the collector connected to can.

QUICK REFERENCE DATA

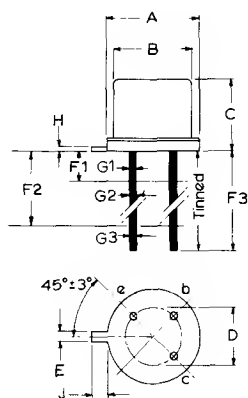
$-V_{CBO}$ max.	65	V
$-V_{CEO}$ max.	65	V
$-I_{CM}$ max.	600	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	600	mW
h_{FE} ($-I_C = 10mA$, $-V_{CE} = 0.4V$) min.	50	
	typ.	90
	max.	200
t_s max. ($-I_C = 100mA$, $-I_{Bon} = I_{Boff} = 10mA$)	250	ns

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A

J.E.D.E.C. TO-5

Millimetres



	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

Collector connected to can

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.	65	V
$-V_{CEO}$ max.	65	V
$-V_{EBO}$ max.	5.0	V
$-I_C$ max.	600	mA
$-I_{CM}$ max.	600	mA
$-I_{EM}$ max.	600	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	600	mW

Temperature

T_{stg} min.	-65	$^\circ C$
T_{stg} max.	200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	292	degC/W
-----------------	-----	--------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 65V, I_E = 0$	-	1.0	500	nA
	$-V_{CB} = 50V, I_E = 0$	-	0.5	50	nA
	$-V_{CB} = 50V, I_E = 0, T_j = 100^\circ C$	-	0.03	2.0	μA
$-I_{EBO}$	Emitter cut-off current				
	$-V_{EB} = 5.0V, I_C = 0$	-	30	500	nA
	$-V_{EB} = 3.0V, I_C = 0$	-	1.0	100	nA
$-V_{BE(sat)}$	Base-emitter saturation voltage				
	$-I_C = 30mA, -I_B = 1.0mA$	-	0.77	0.90	V
	$-I_C = 150mA, -I_B = 15mA$	-	1.05	1.30	V
h_{FE}	Static forward current transfer ratio				
	$-I_C = 1.0mA, -V_{CE} = 0.4V$	40	80	-	
	$-I_C = 10mA, -V_{CE} = 0.4V$	50	90	200	
	$-I_C = 50mA, -V_{CE} = 0.4V$	20	92	-	
	$-I_C = 150mA, -V_{CE} = 0.4V$	10	50	-	

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ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
C_{tc}	Collector capacitance $-V_{CB} = 10V, I_E = I_c = 0,$ $f = 1.0MHz$	-	6.0	12	pF
C_{te}	Emitter capacitance $-V_{EB} = 2.0V, I_C = I_c = 0,$ $f = 1.0MHz$	-	18	30	pF

Saturated switching times (see page 4)

$-I_C = 100mA, -I_{Bon} = I_{Boff} = 10mA, V_{EE} = 10V, V_{BEoff} = 2.0V$

t_d	Delay time	-	9	15	ns
t_r	Rise time	-	18	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	-	27	50	ns
t_s	Storage time	-	95	250	ns
t_f	Fall time	-	30	50	ns
t_{off}	Turn-off time ($t_s + t_f$)	-	125	290	ns

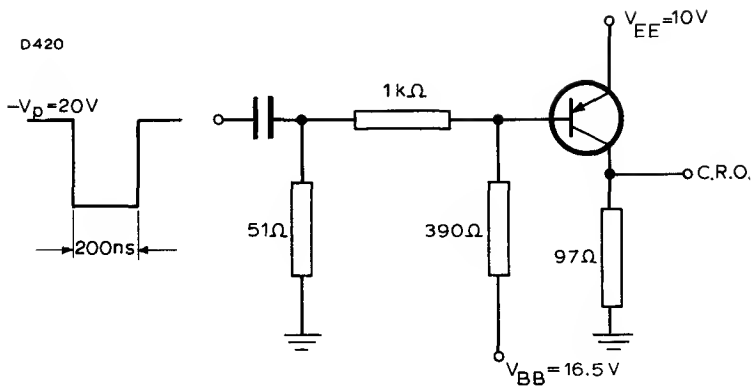
SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of $245^{\circ}C$ for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above $100^{\circ}C$ before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

ELECTRICAL CHARACTERISTICS (cont'd)

Saturated switching times

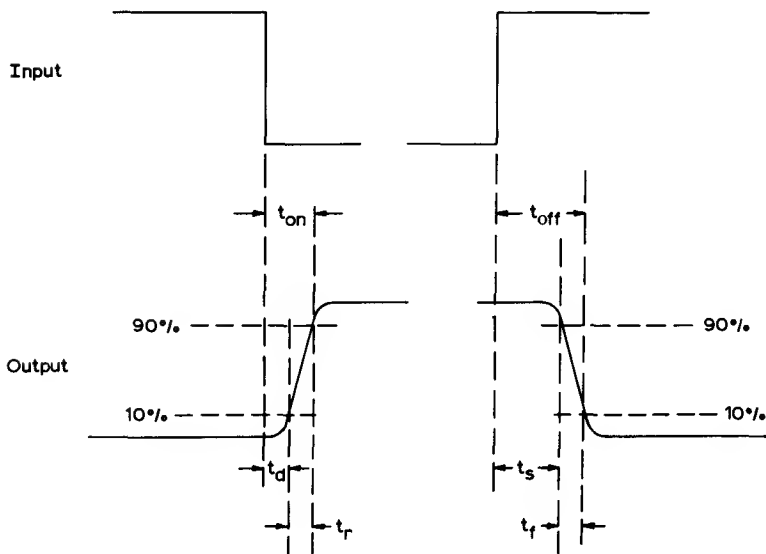
Test circuit

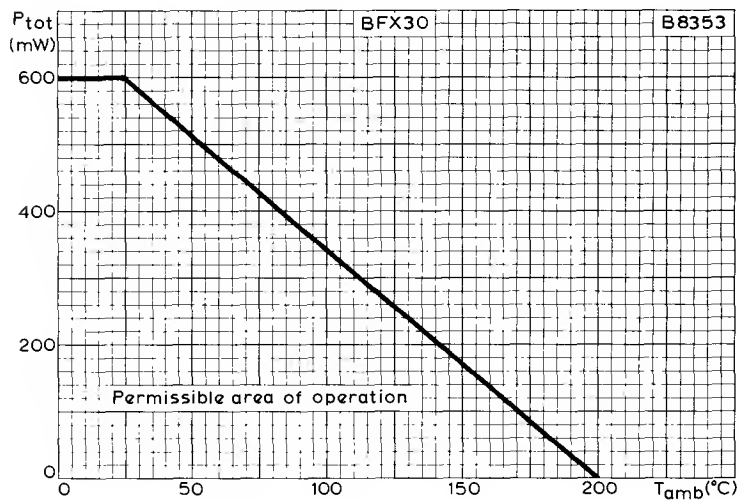


$$-I_C = 100\text{mA}, -I_{B(\text{on})} = I_{B(\text{off})} = 10\text{mA}$$

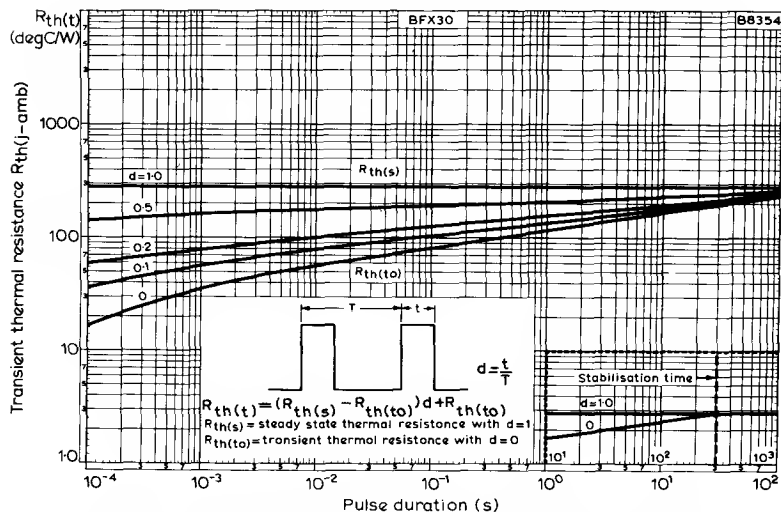
$$V_{BE(\text{off})} = 2.0\text{V}$$

Waveforms

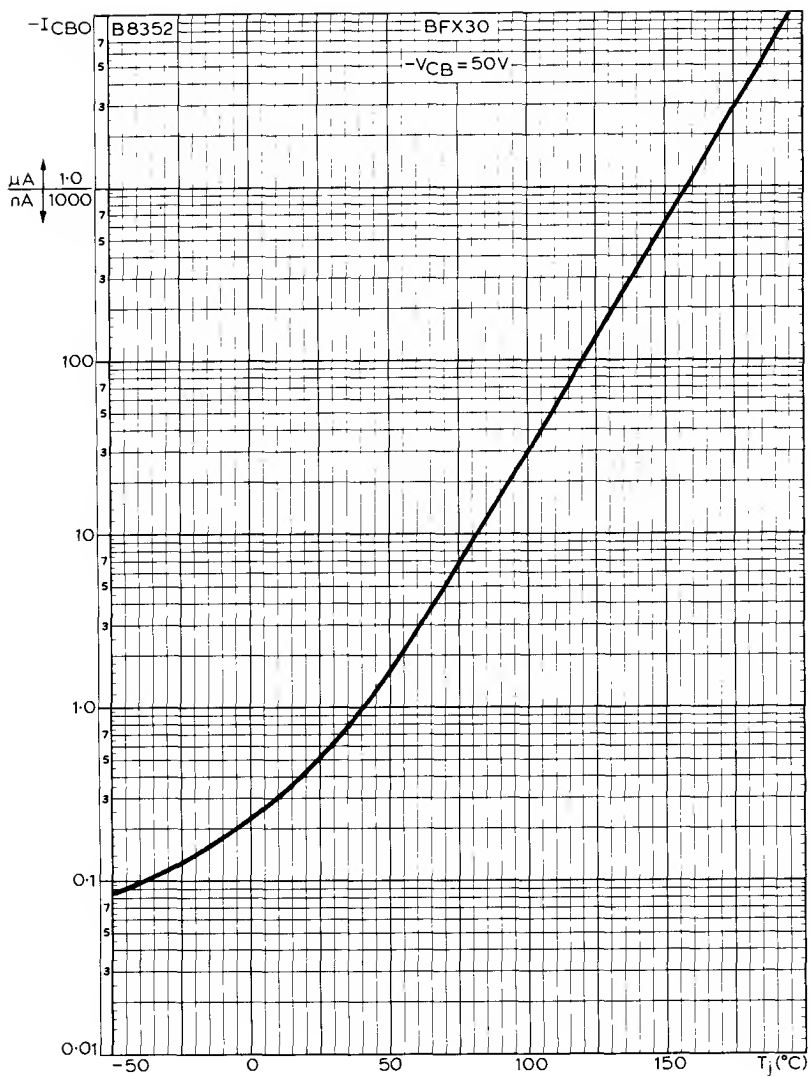




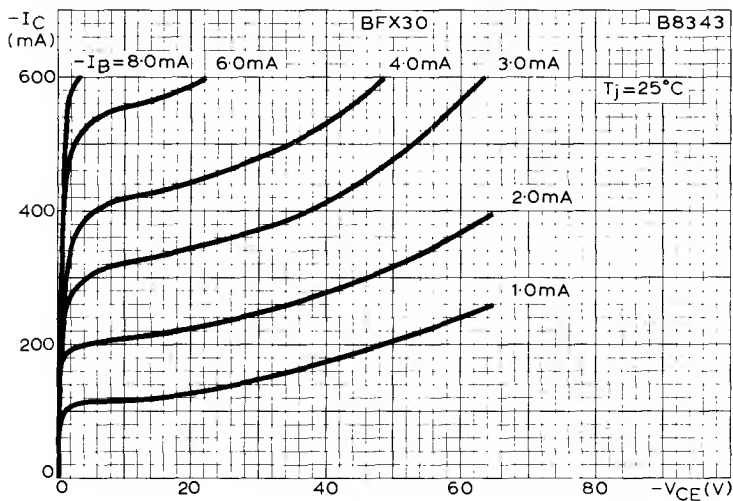
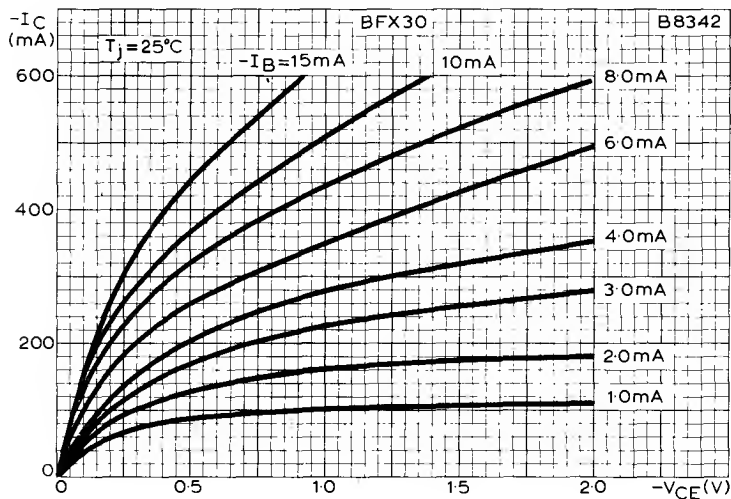
TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



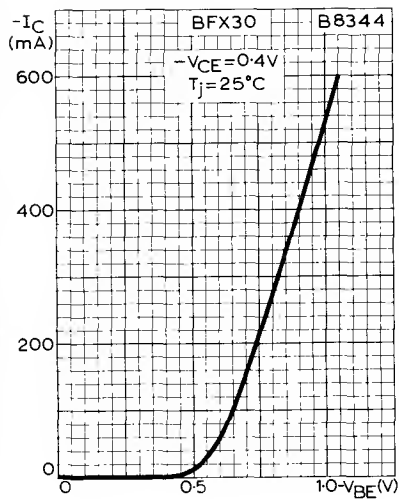
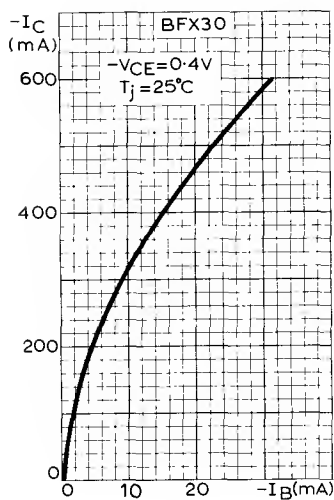
TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS
PLOTTED AGAINST PULSE DURATION



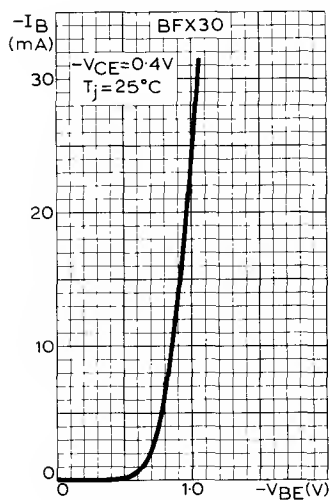
TYPICAL VARIATION OF COLLECTOR CUT-OFF CURRENT
WITH JUNCTION TEMPERATURE



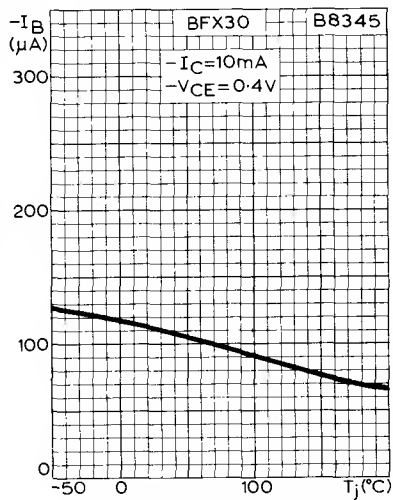
TYPICAL OUTPUT CHARACTERISTICS AT LOW AND HIGH
COLLECTOR-EMITTER VOLTAGES



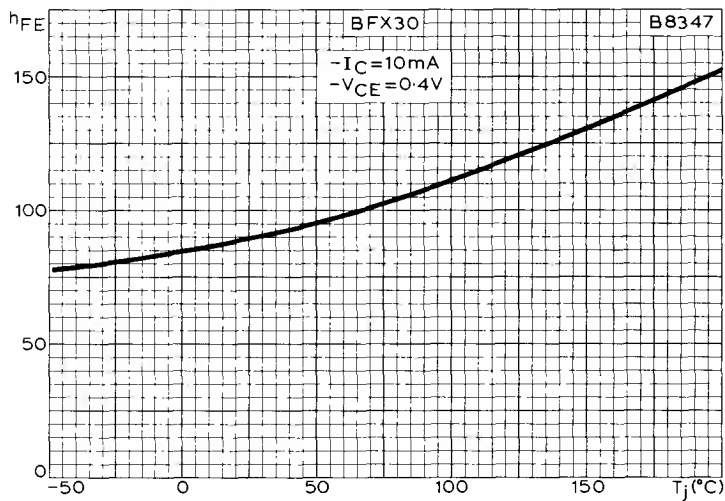
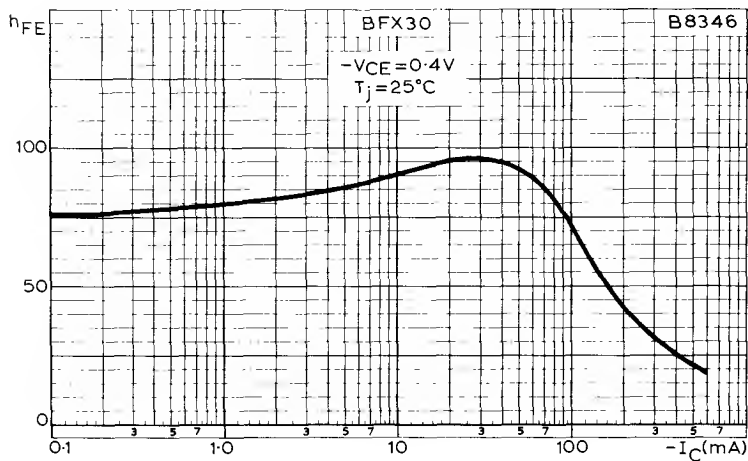
TYPICAL TRANSFER AND MUTUAL CHARACTERISTICS



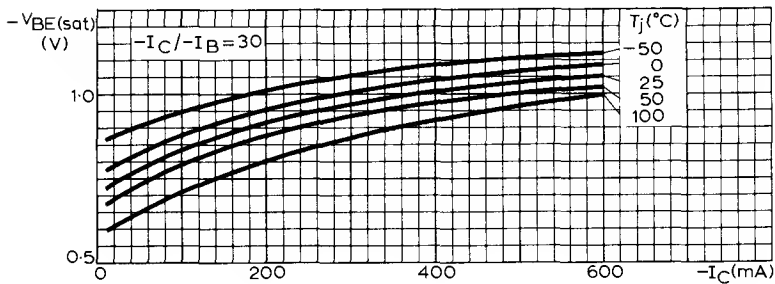
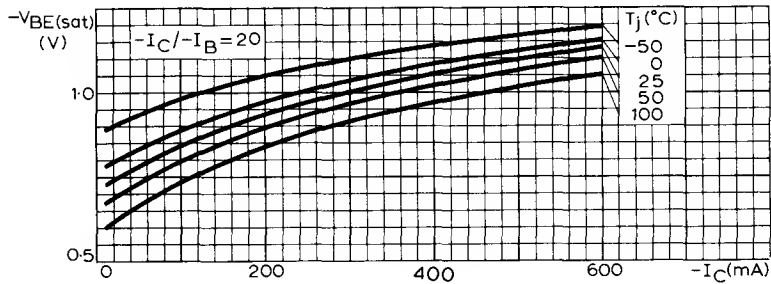
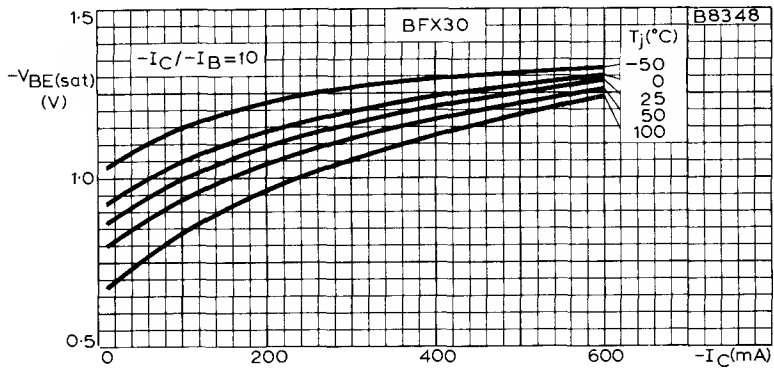
Typical input characteristics



Typical base current versus
junction temperature



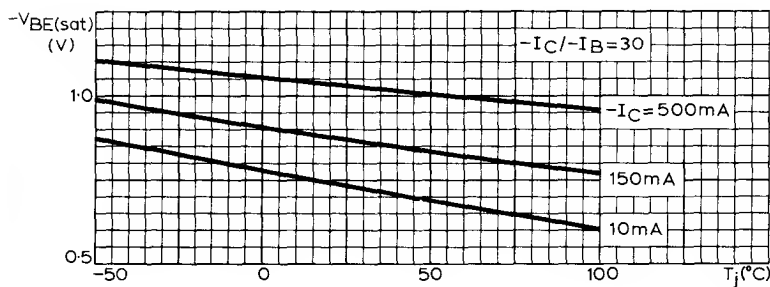
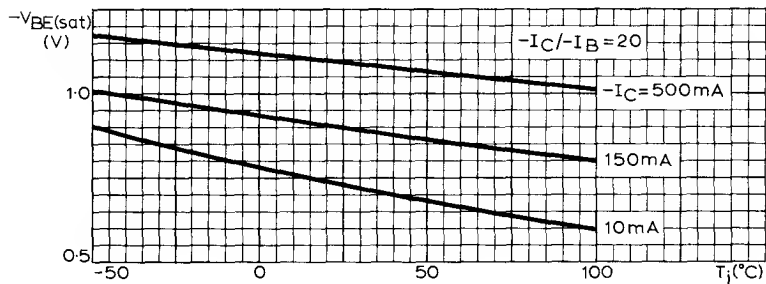
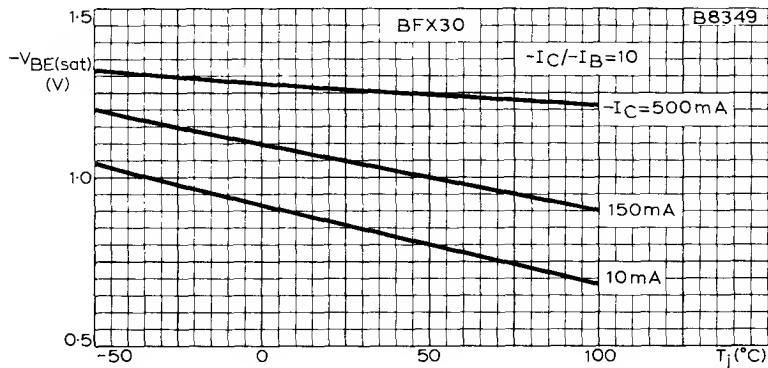
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH COLLECTOR CURRENT AND JUNCTION TEMPERATURE



TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE
WITH COLLECTOR CURRENT AND I_C/I_B RATIO

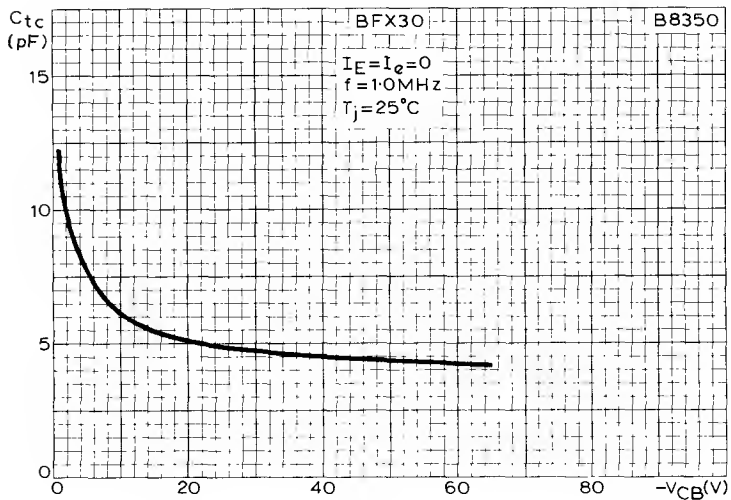
P-N-P SILICON PLANAR EPITAXIAL TRANSISTOR

BFX30

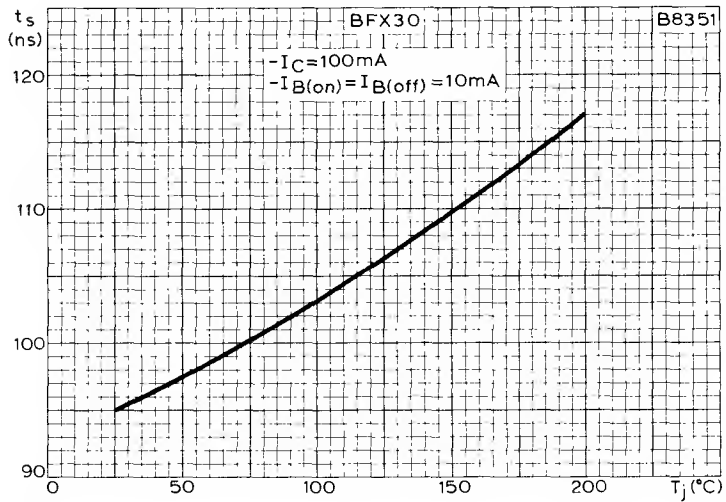


TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE
WITH JUNCTION TEMPERATURE AND I_C/I_B RATIO

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TYPICAL VARIATION OF COLLECTOR CAPACITANCE WITH COLLECTOR-BASE VOLTAGE



TYPICAL VARIATION OF STORAGE TIME WITH JUNCTION TEMPERATURE

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

Silicon n-p-n planar epitaxial transistors for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

QUICK REFERENCE DATA

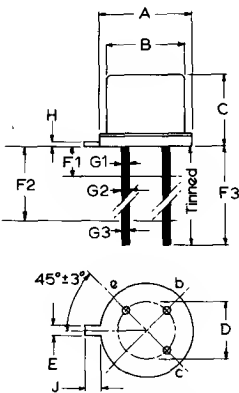
	BFX84	BFX85	BFX86	
V_{CBO} max.	100	100	40	V
V_{CEO} max.	60	60	35	V
I_{CM} max.	1.0	1.0	1.0	A
P_{tot} max. $T_{amb} \leq 25^{\circ}C$	800	800	800	mW
$T_{case} \leq 100^{\circ}C$	2.86	2.86	2.86	W
h_{FE} ($I_C = 150mA$, $V_{CE} = 10V$) min.	30	70	70	
typ.	112	142	142	
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^{\circ}C$)	50	50	50	MHz

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0



The collector is electrically connected to the envelope

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BFX84	BFX85	BFX86	
V_{CBO} max.	100	100	40	V
V_{CE} max. (cut-off, $I_C \leq 1\text{mA}$)	100	100	40	V
V_{CEO} max.	60	60	35	V
V_{EBO} max.		6.0		V
I_C max.		1.0		A
I_{CM} max.		1.0		A
$-I_E$ max.		1.0		A
$-I_{EM}$ max.		1.0		A
I_B max.		100		mA
$\pm I_{BM}$ max.		100		mA
P_{tot} max. $T_{amb} \leq 25^\circ\text{C}$		800		mW
$T_{case} \leq 25^\circ\text{C}$		5.0		W
$T_{case} > 25, < 100^\circ\text{C}$		2.86		W

Temperature

T_{stg}	-65 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	220	degC/W
$R_{th(j-case)}$	35	degC/W

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

BFX84

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{\text{CB}} = 100\text{V}, I_{\text{E}} = 0$	-	10	500	nA
	$V_{\text{CB}} = 100\text{V}, I_{\text{E}} = 0, T_j = 100^{\circ}\text{C}$	-	0.5	30	μA
	$V_{\text{CB}} = 80\text{V}, I_{\text{E}} = 0$	-	2.0	50	nA
I_{EBO}	Emitter cut-off current				
	$V_{\text{EB}} = 6.0\text{V}, I_{\text{C}} = 0$	-	10	500	nA
	$V_{\text{EB}} = 5.0\text{V}, I_{\text{C}} = 0$	-	2.0	50	nA
	$V_{\text{EB}} = 5.0\text{V}, I_{\text{C}} = 0, T_j = 100^{\circ}\text{C}$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_{\text{C}} = 10\text{mA}, V_{\text{CE}} = 10\text{V}$	20	80	-	
	$I_{\text{C}} = 150\text{mA}, V_{\text{CE}} = 10\text{V}$	30	112	-	
	$I_{\text{C}} = 500\text{mA}, V_{\text{CE}} = 10\text{V}$	20	70	-	
	$I_{\text{C}} = 1.0\text{A}, V_{\text{CE}} = 10\text{V}$	15	35	-	
$V_{\text{CE(sat)}}$	Collector-emitter saturation voltage				
	$I_{\text{C}} = 10\text{mA}, I_{\text{B}} = 1.0\text{mA}$	-	0.06	0.15	V
	$I_{\text{C}} = 150\text{mA}, I_{\text{B}} = 15\text{mA}$	-	0.15	0.35	V
	$I_{\text{C}} = 500\text{mA}, I_{\text{B}} = 50\text{mA}$	-	0.35	1.00	V
	$I_{\text{C}} = 1.0\text{A}, I_{\text{B}} = 100\text{mA}$	-	0.66	1.60	V
$V_{\text{BE(sat)}}$	Base-emitter saturation voltage				
	$I_{\text{C}} = 10\text{mA}, I_{\text{B}} = 1.0\text{mA}$	-	0.69	1.2	V
	$I_{\text{C}} = 150\text{mA}, I_{\text{B}} = 15\text{mA}$	-	0.92	1.3	V
	$I_{\text{C}} = 500\text{mA}, I_{\text{B}} = 50\text{mA}$	-	1.15	1.5	V
	$I_{\text{C}} = 1.0\text{A}, I_{\text{B}} = 100\text{mA}$	-	1.40	2.0	V
C_{Tc}	Collector capacitance				
	$V_{\text{CB}} = 10\text{V}, I_{\text{E}} = I_{\text{e}} = 0,$ $f = 1.0\text{MHz}$	-	7.0	12	pF

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ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 35\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	50	185	-	MHz

Saturated switching times

$$I_C = 150\text{mA}, I_{B(on)} = -I_{B(off)} = 15\text{mA},$$

$$-V_{EE} = 10\text{V}, -V_{BE(off)} = 2.0\text{V}$$

t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns

h-parameters

$$h_{fe} \quad I_C = 1.0\text{mA}, V_{CE} = 5.0\text{V},$$

$$f = 1.0\text{kHz}, T_{amb} = 25^\circ\text{C}$$

h_{ie}	$I_C = 10\text{mA}, V_{CE} = 5.0\text{V},$ $f = 1.0\text{kHz}, T_{amb} = 25^\circ\text{C}$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

BFX86

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 40\text{V}, I_E = 0$	-	10	500	nA
	$V_{CB} = 40\text{V}, I_E = 0, T_j = 100^\circ\text{C}$	-	0.5	30	μA
	$V_{CB} = 30\text{V}, I_E = 0$	-	2.0	50	nA
	$V_{CB} = 30\text{V}, I_E = 0, T_j = 100^\circ\text{C}$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0\text{V}, I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0\text{V}, I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0\text{V}, I_C = 0, T_j = 100^\circ\text{C}$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 10\text{mA}, V_{CE} = 10\text{V}$	50	90	-	
	$I_C = 150\text{mA}, V_{CE} = 10\text{V}$	70	142	-	
	$I_C = 500\text{mA}, V_{CE} = 10\text{V}$	30	90	-	
	$I_C = 1.0\text{A}, V_{CE} = 10\text{V}$	15	50	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10\text{mA}, I_B = 1.0\text{mA}$	-	0.06	0.15	V
	$I_C = 150\text{mA}, I_B = 15\text{mA}$	-	0.15	0.35	V
	$I_C = 500\text{mA}, I_B = 50\text{mA}$	-	0.35	1.00	V
	$I_C = 1.0\text{A}, I_B = 100\text{mA}$	-	0.66	1.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10\text{mA}, I_B = 1.0\text{mA}$	-	0.69	1.2	V
	$I_C = 150\text{mA}, I_B = 15\text{mA}$	-	0.92	1.3	V
	$I_C = 500\text{mA}, I_B = 50\text{mA}$	-	1.15	1.5	V
	$I_C = 1.0\text{A}, I_B = 100\text{mA}$	-	1.40	2.0	V
C_{Tc}	Collector capacitance				
	$V_{CB} = 10\text{V}, I_E = I_E = 0,$ $f = 1.0\text{MHz}$	-	7.0	12	pF

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ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 35\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	50	185	-	MHz

Saturated switching times



$I_C = 150\text{mA}$, $I_{B(on)} = -I_{B(off)} = 15\text{mA}$,
 $-V_{EE} = 10\text{V}$, $-V_{BE(off)} = 2.0\text{V}$

t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns

h-parameters

h_{fe} $I_C = 1.0\text{mA}$, $V_{CE} = 5.0\text{V}$,
 $f = 1.0\text{kHz}$, $T_{amb} = 25^\circ\text{C}$

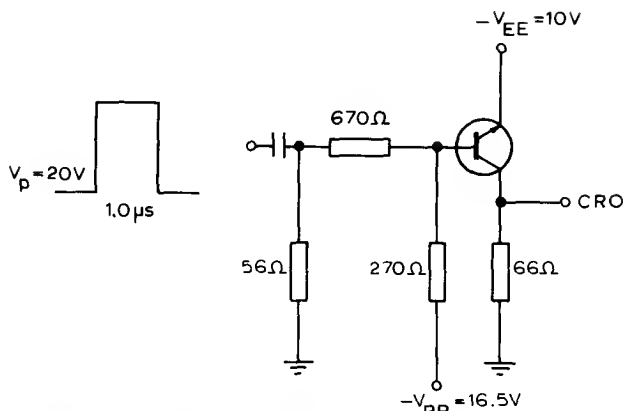
h_{ie}	$I_C = 10\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 1.0\text{kHz}$, $T_{amb} = 25^\circ\text{C}$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

MEASUREMENT OF SATURATED SWITCHING TIMES

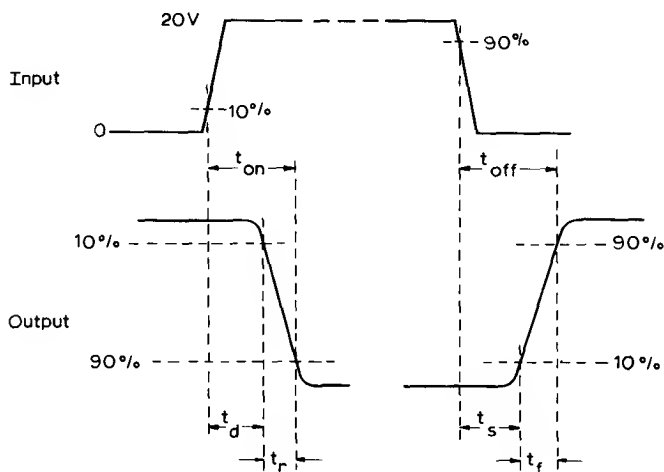
Test circuit



$$I_C = 150 \text{ mA}, I_{B(\text{on})} = -I_{B(\text{off})} = 15 \text{ mA}$$

$$-V_{BE(\text{off})} = 2.0 \text{ V}$$

Switching waveforms



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OPERATING NOTES

1. Dissipation and heatsink considerations

a) Steady-state conditions

The maximum steady-state dissipation P_s is given by the relation-ship:

$$P_s \text{ max.} = \frac{T_j \text{ max.} - T_{\text{amb}}}{R_{\text{th(j-amb)}}$$

Where $T_j \text{ max.}$ is the maximum permissible operating junction temperature,

T_{amb} is the ambient temperature,

$R_{\text{th(j-amb)}}$ is the total thermal resistance between junction and ambient.

Page 13 gives the maximum allowable steady-state dissipation versus ambient temperature for the device mounted in free air and with infinite heatsink.

b) Pulse conditions (rectangular pulses)

The maximum pulse power P_p is given by the formula

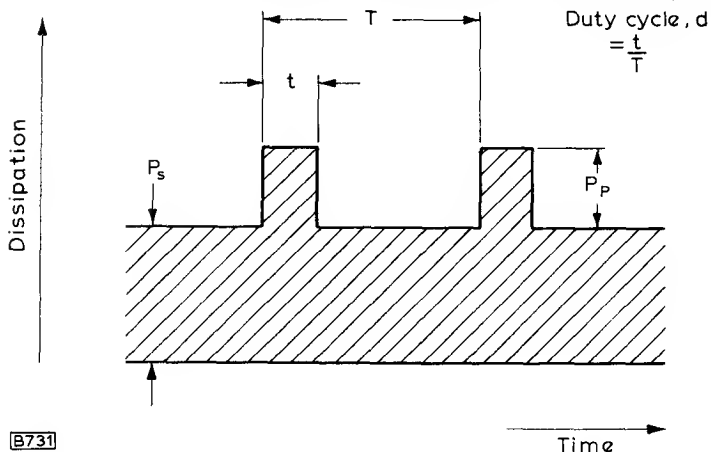
$$P_p = \frac{(T_j \text{ max.} - T_{\text{amb}}) - (P_s \cdot R_{\text{th(j-amb)}})}{R_{\text{th(t)}} + d \cdot R_{\text{th(case-amb)}}$$

Where P_s is the steady-state dissipation excluding that in the pulses,

$R_{\text{th(t)}}$ is effective transient thermal resistance of the device between junction and case, and is a function of the pulse duration t , and duty cycle d ,

d is the duty cycle, and is equal to the pulse duration t divided by the periodic time T ,

$R_{\text{th(case-amb)}}$ is the total thermal resistance between case and ambient and is equal to the difference between $R_{\text{th(j-amb)}}$ and the thermal resistance from junction to case $R_{\text{th(j-case)}}$.



- b) Pulse conditions (rectangular pulses) (cont'd)

Example

The following example shows how to calculate the maximum permissible peak dissipation of a BFX84 mounted in free air at a temperature not exceeding 65°C. The steady-state dissipation under the bottomed condition is 350mW, the pulse width is 1ms and the duty cycle is 0.2.

The transient thermal resistance $R_{th(t)} = 15.5 \text{ degC/W}$ (page 13)

$$\begin{aligned} P_{p \text{ max.}} &= \frac{(200-65) - (0.35 \times 220)}{15.5 + 0.2(220-35)} \\ &= \frac{135-77}{15.5+37} \\ &= 1.1\text{W} \end{aligned}$$

The peak pulse dissipation of 1.1W is therefore allowed provided that the voltage and current ratings of the device are not exceeded.

- c) Pulse conditions (other than rectangular)

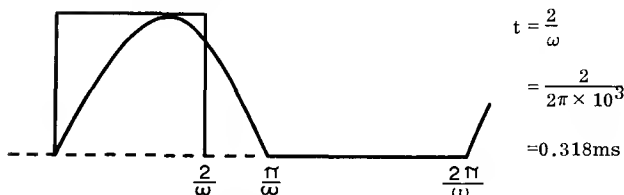
For sinusoidal and irregular shaped waveforms, the power pulse is converted to an equivalent rectangular pulse of the same average and peak values, and treated as in the previous section.

Example

The following example illustrates how to find the maximum permissible peak dissipation of a BFX84 operating in a class 'B' circuit at 1kHz. The device is mounted on a heatsink of thermal resistance equal to 50degC/W and at an ambient temperature not exceeding 100°C. Assuming that the waveform is sinusoidal for half period and zero for the other half.

$$\text{Average of sinewave over half cycle} = 2P_p / \pi$$

Therefore equivalent rectangular pulse width of same amplitude and average value



B3559

$$\text{Duty cycle, } d = \frac{1}{\pi}$$

- c) Pulse conditions (other than rectangular) (cont'd)

$$\text{Duty cycle, } d = \frac{2}{\omega} \bigg/ \frac{2\pi}{\omega} = \frac{1}{\pi} = 0.318$$

From page 13

$$R_{th(t)} = 6.8 \text{degC/W (d=0)}$$

$$R_{th(s)} = 35 \text{degC/W}$$

$$R_{th(t)} \text{ at } d=0.318 = (35-6.8) \times 0.318 + 6.8 \\ = 15.8 \text{degC/W}$$

$$P_p \text{ max.} = \frac{(200-100) - 0}{15.8+0.318 \times 50} \\ = \frac{100}{31.7} = 3.15 \text{W}$$

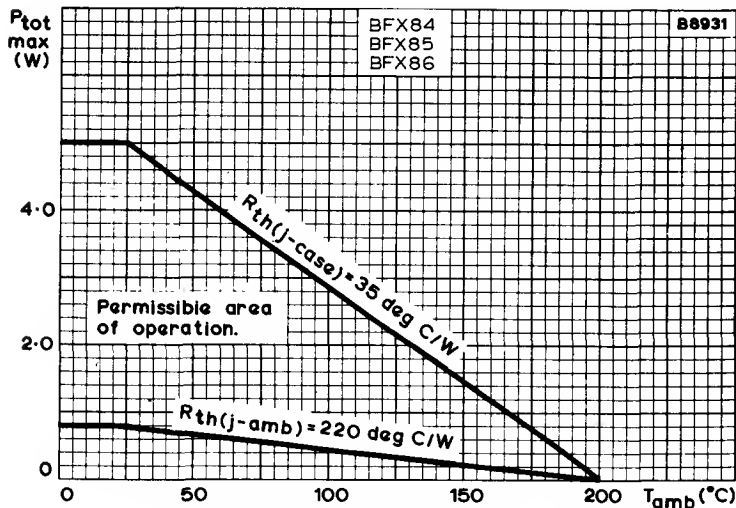
A peak power of 3.15W is therefore permissible provided that the voltage and current ratings of the device are not exceeded.

SOLDERING AND WIRING RECOMMENDATIONS

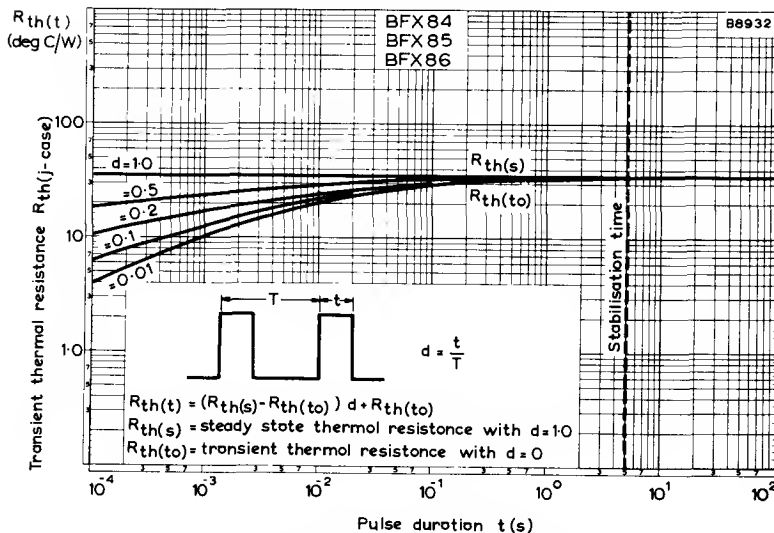
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

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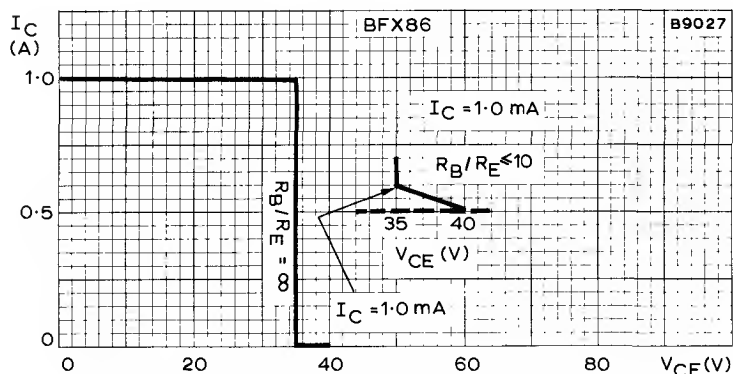
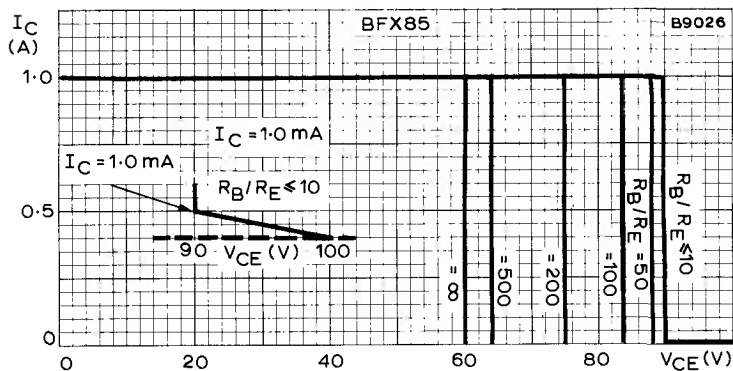
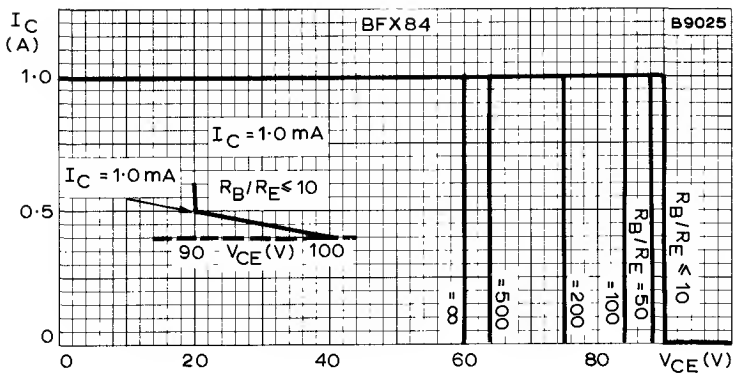


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST
AMBIENT TEMPERATURE



TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS
PLOTTED AGAINST PULSE DURATION

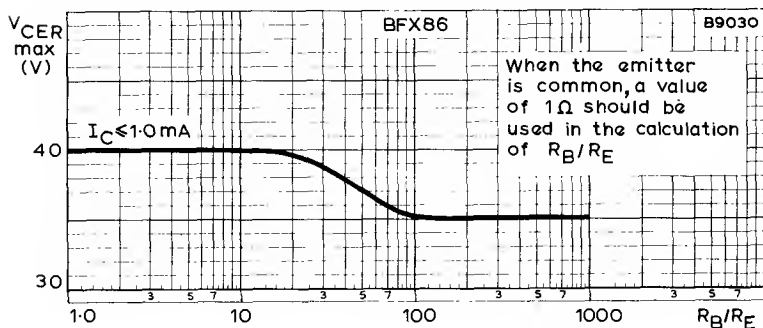
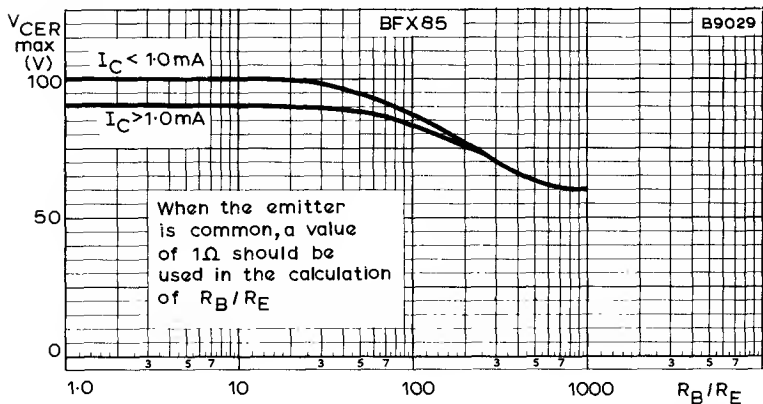
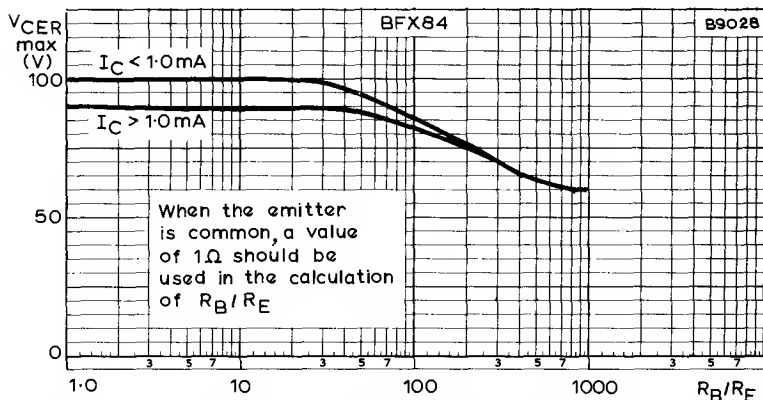
Mullard



COLLECTOR CURRENT PLOTTED AGAINST MAXIMUM
COLLECTOR-EMITTER VOLTAGE WITH R_B/R_E AS PARAMETER

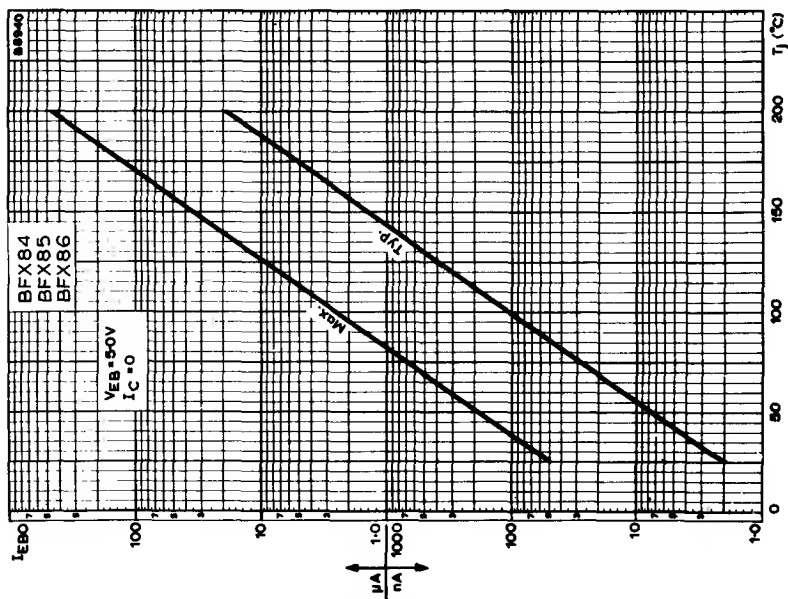
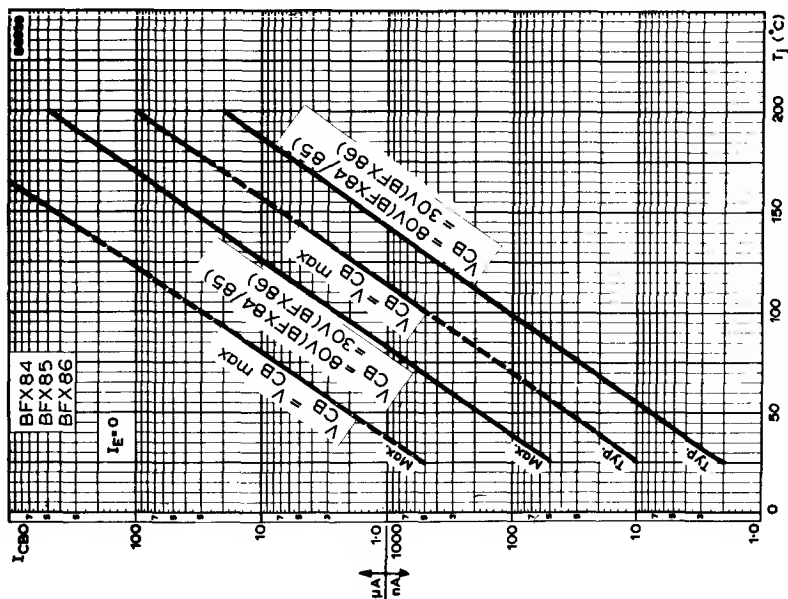
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86



MAXIMUM COLLECTOR-EMITTER VOLTAGE PLOTTED AGAINST
 R_B/R_E RATIO

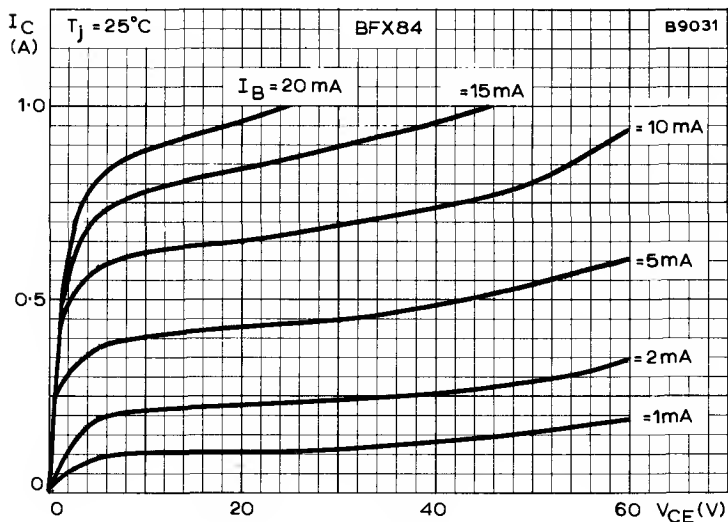
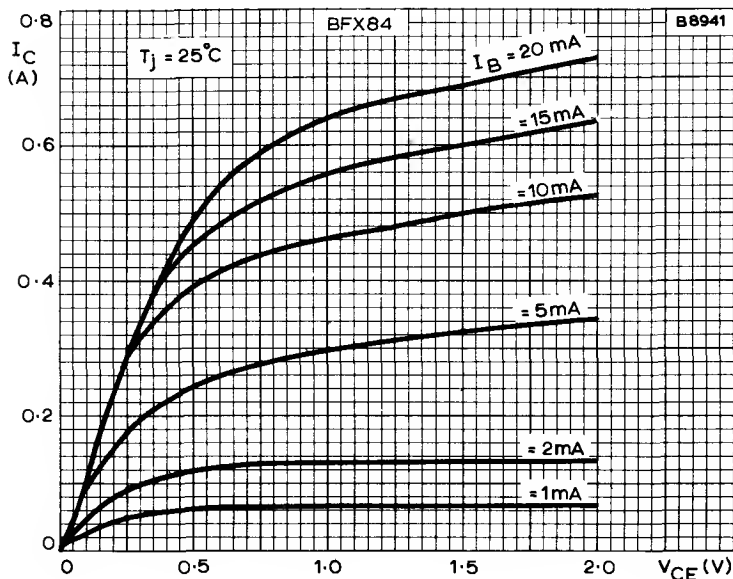
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COLLECTOR AND EMITTER CUT-OFF CURRENTS PLOTTED
AGAINST JUNCTION TEMPERATURE

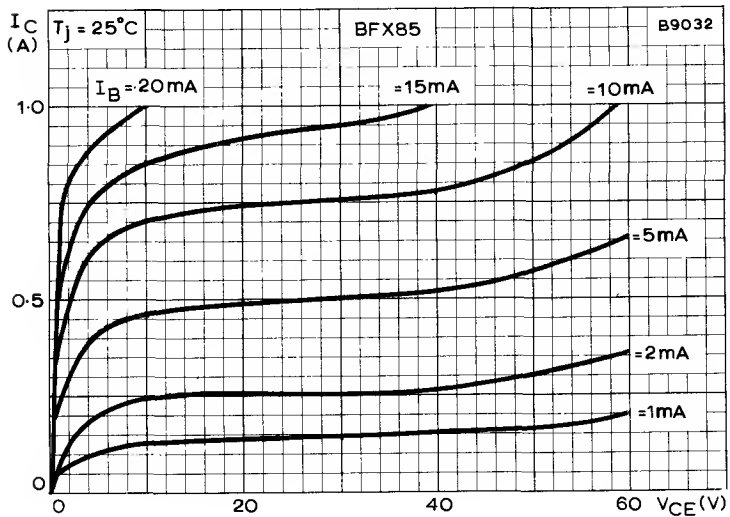
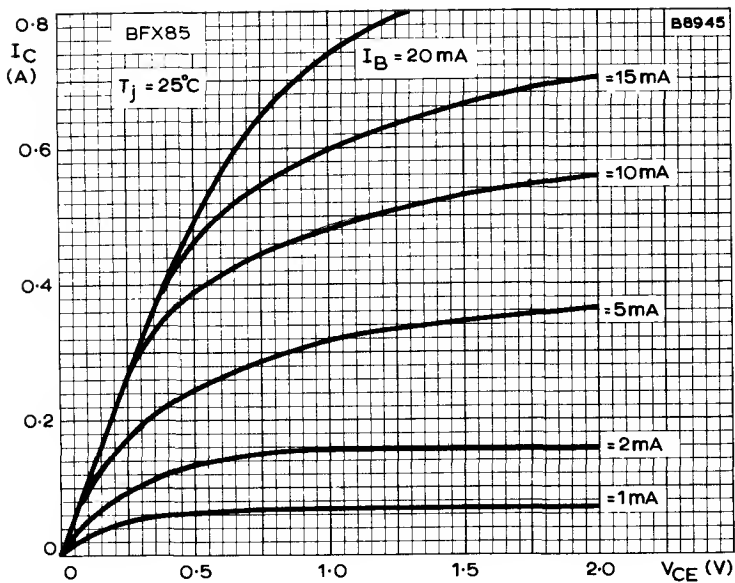
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86



TYPICAL OUTPUT CHARACTERISTICS

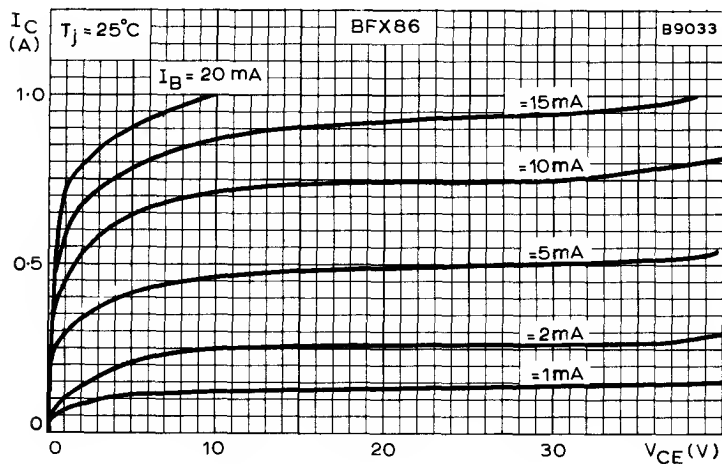
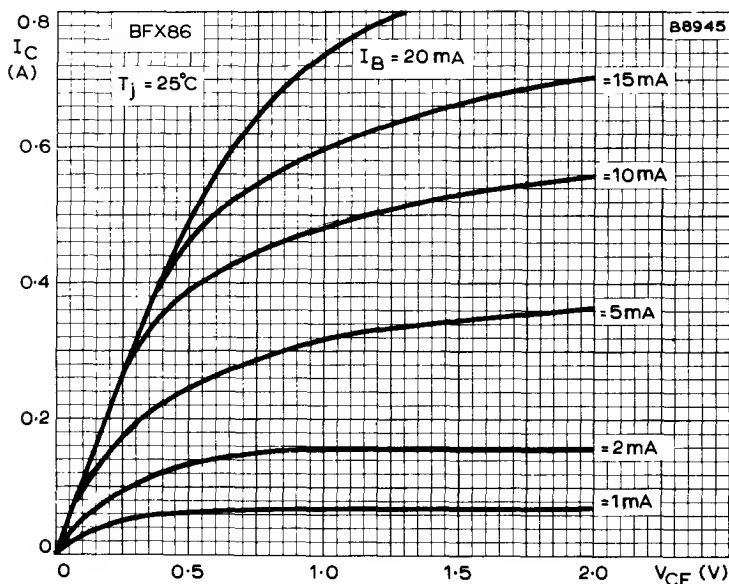
Mullard



TYPICAL OUTPUT CHARACTERISTICS

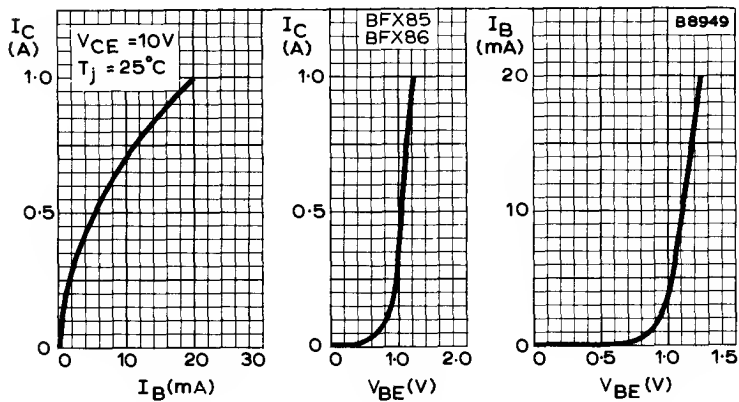
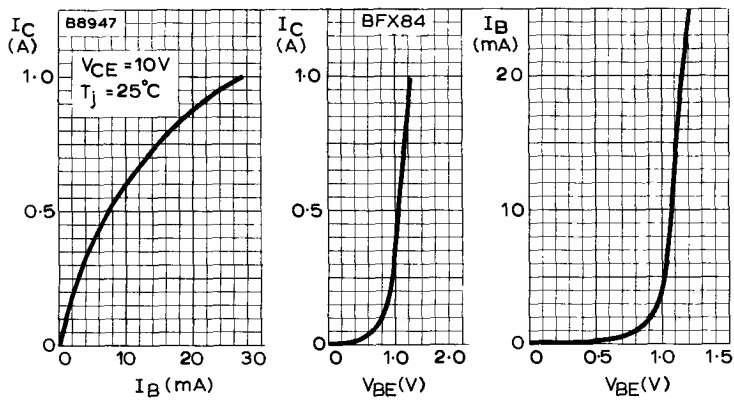
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

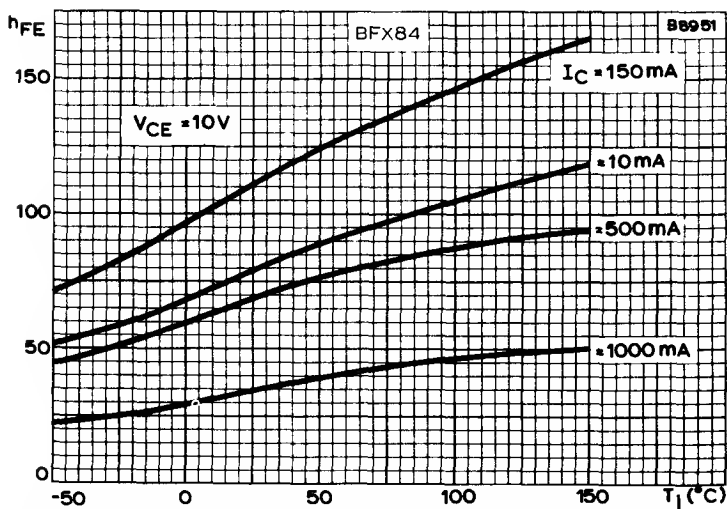
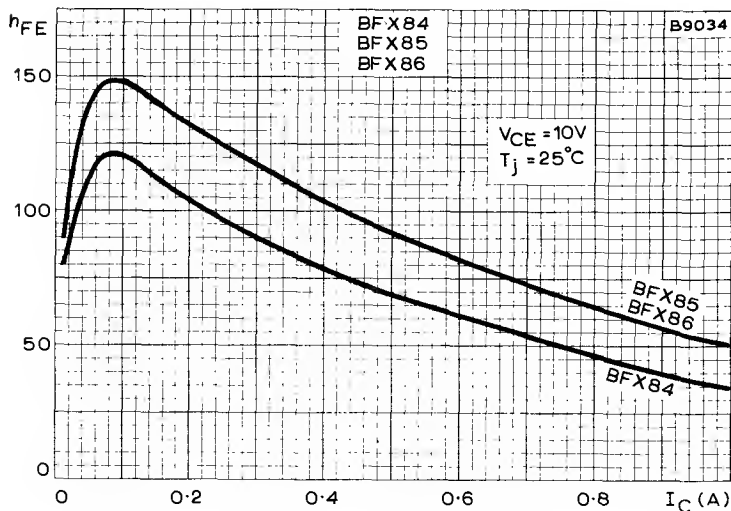


TYPICAL OUTPUT CHARACTERISTICS

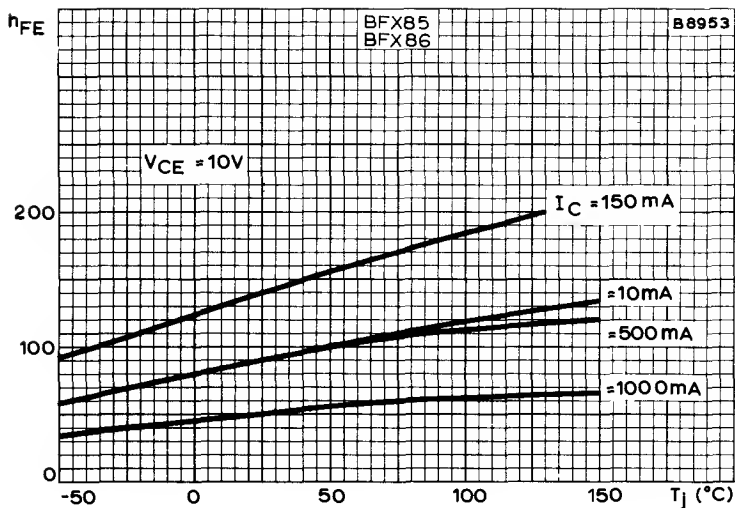
Mullard



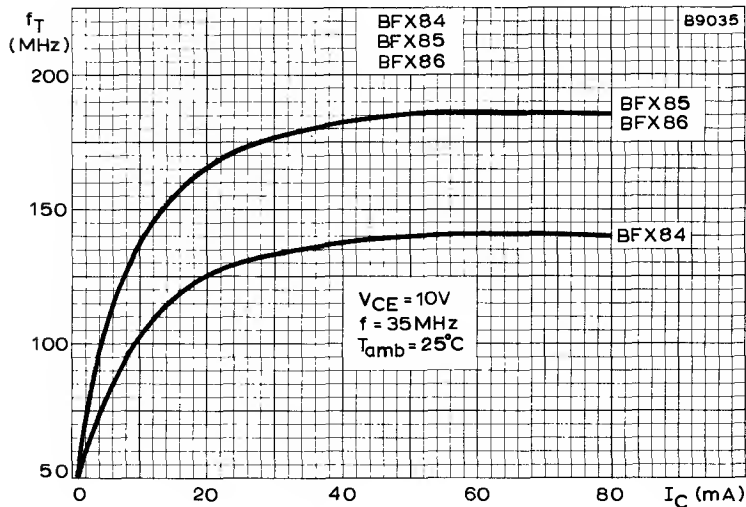
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED
AGAINST COLLECTOR CURRENT AND JUNCTION TEMPERATURE



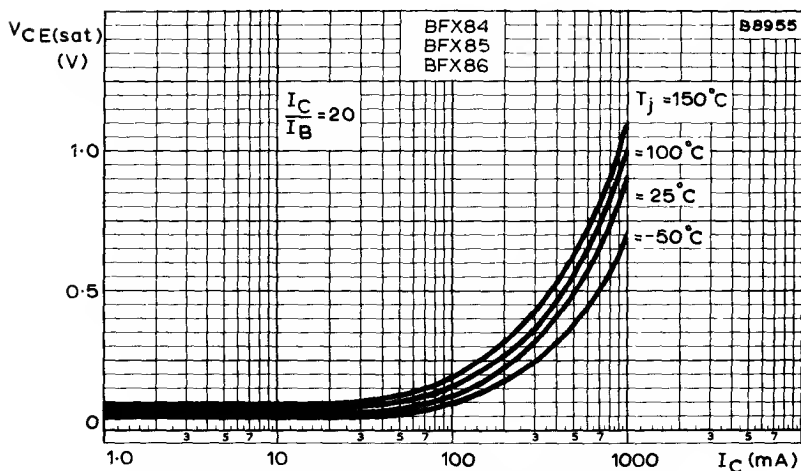
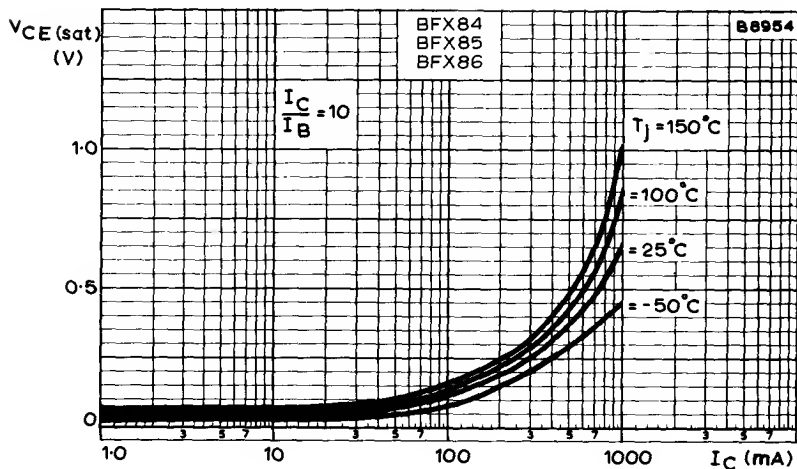
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED
AGAINST JUNCTION TEMPERATURE



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST
COLLECTOR CURRENT

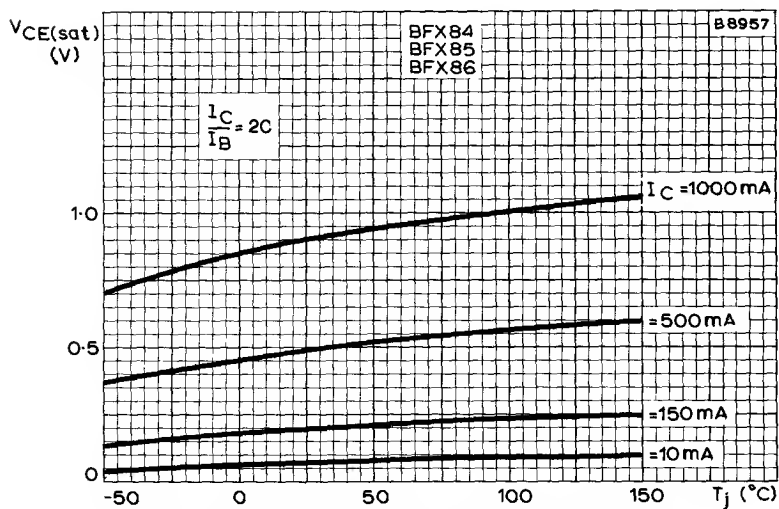
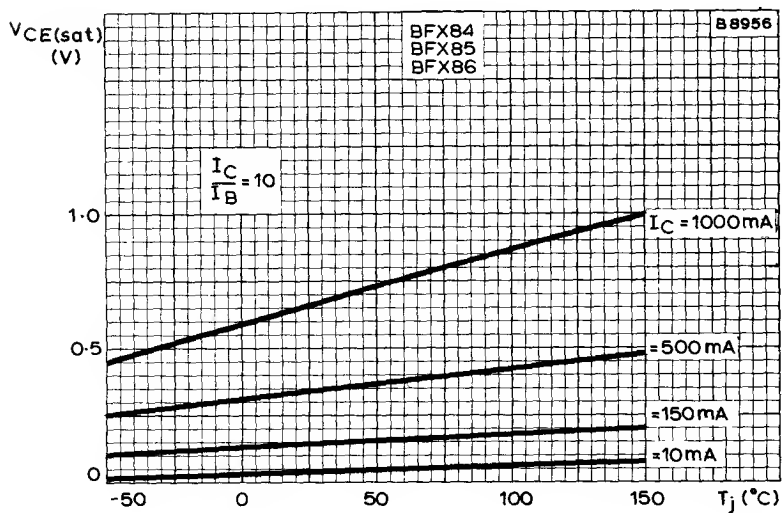
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT

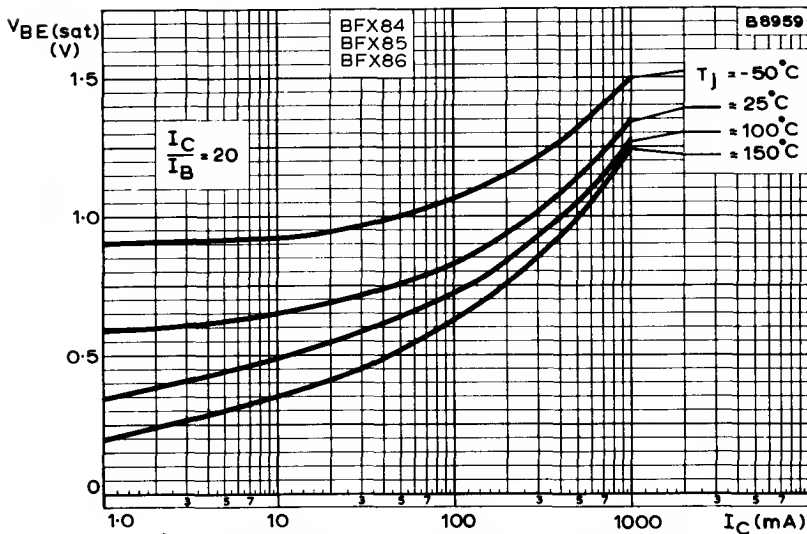
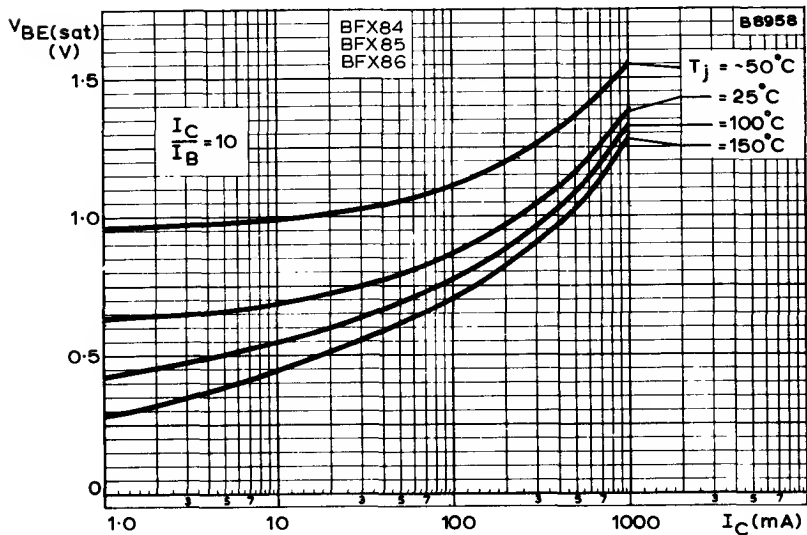
Mullard



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
 PLOTTED AGAINST JUNCTION TEMPERATURE

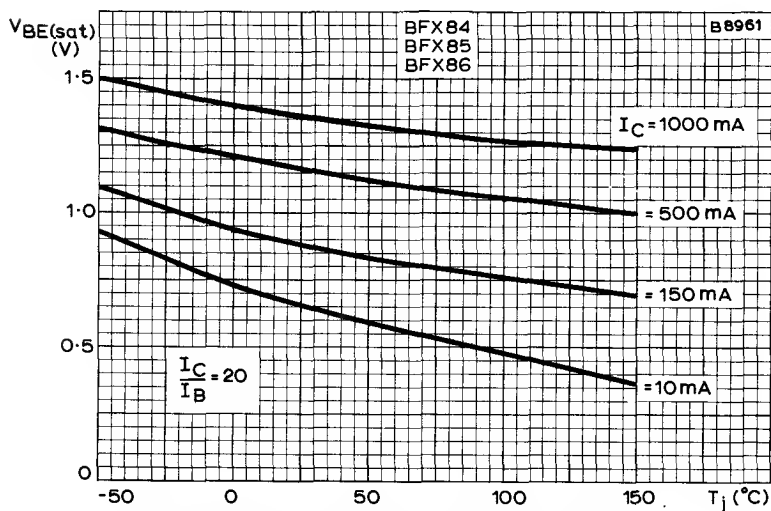
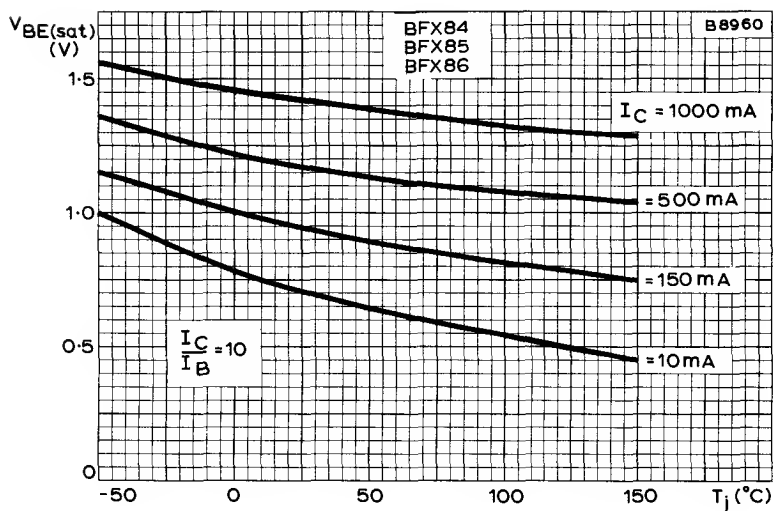
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

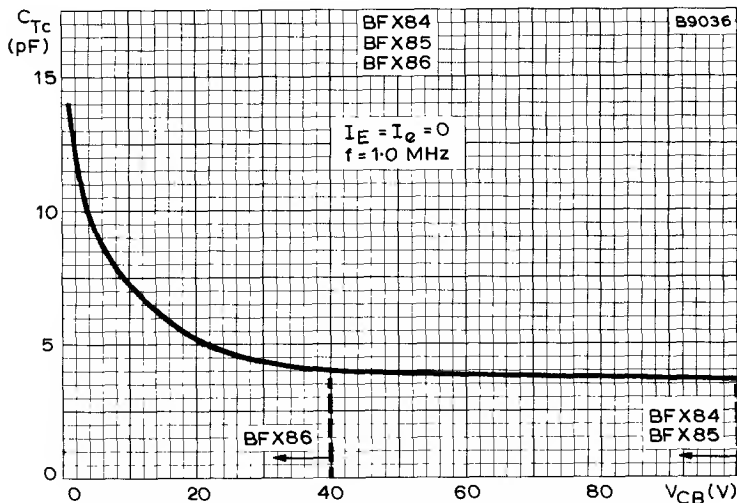


TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT

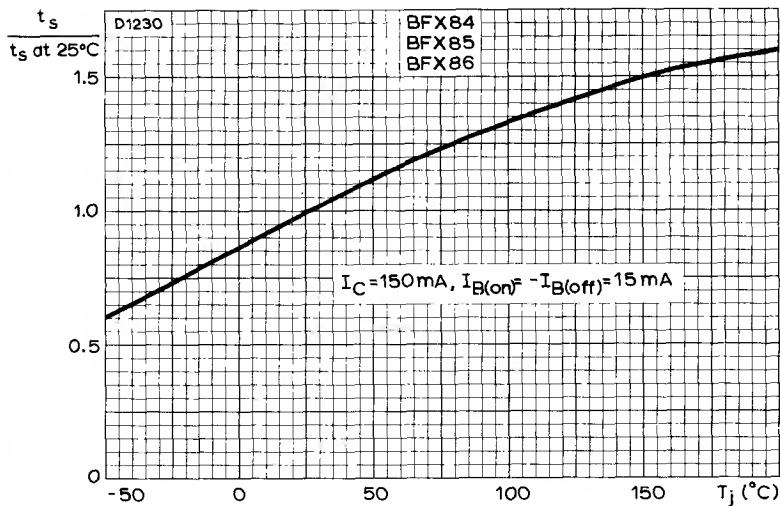
Mullard



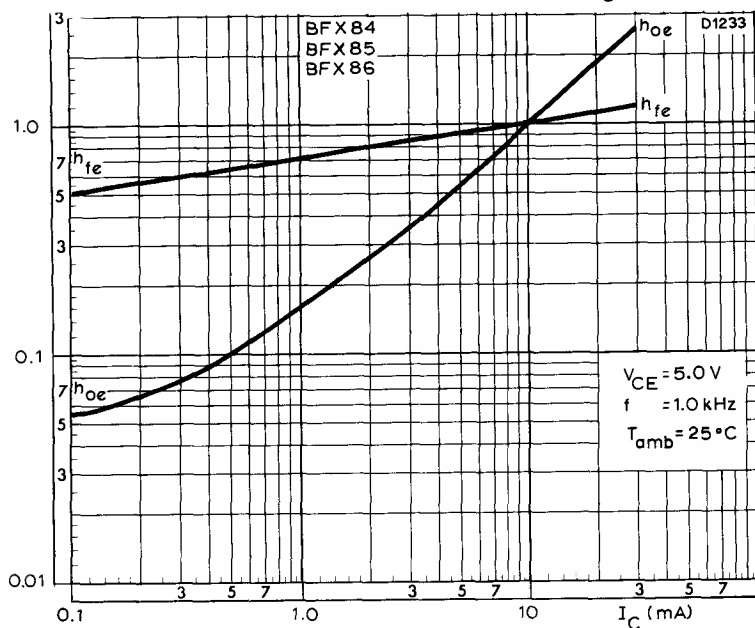
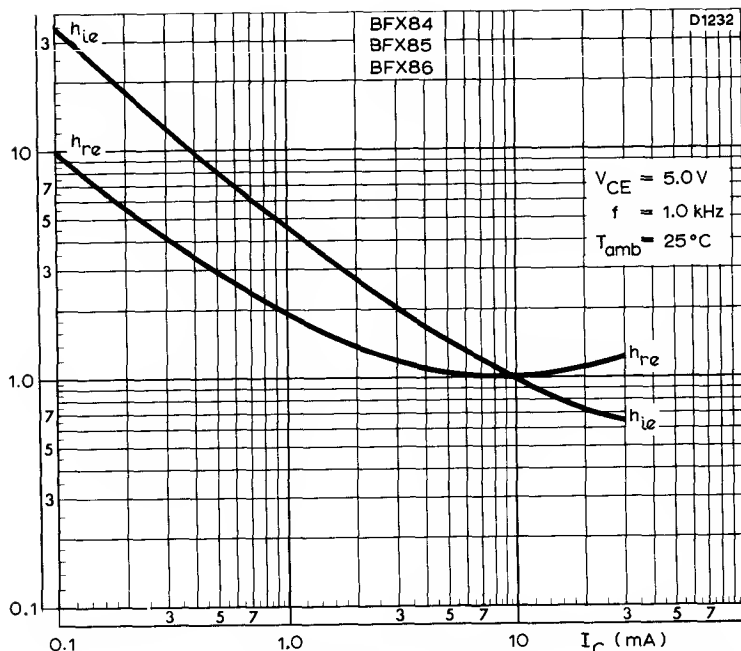
TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL COLLECTOR CAPACITANCE PLOTTED AGAINST
COLLECTOR-BASE VOLTAGE



TYPICAL STORAGE TIME NORMALISED AT 25°C



TYPICAL h-PARAMETERS NORMALISED AT $I_C = 10\text{mA}$

Mullard

**P-N-P SILICON PLANAR
EPITAXIAL TRANSISTORS**

**BFX87
BFX88**

For ratings, characteristics and mechanical
details see BFX29 data sheet

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFX89

N-P-N silicon planar epitaxial transistor designed for u.h.f. and v.h.f. applications. It has extremely good noise and intermodulation properties and a very high power gain and transition frequency. It is therefore particularly suitable for wideband aerial and distribution amplifiers.

QUICK REFERENCE DATA

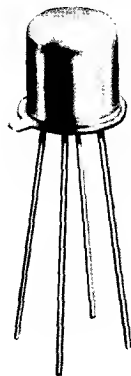
V_{CBOM} max. (peak)	30	V
V_{CEO} max.	15	V
I_{CM} max. ($f > 1.0$ MHz)	50	mA
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	200	mW
T_j max.	200	$^{\circ}C$
f_T typ. ($I_C = 25$ mA, $V_{CE} = 5$ V, $f = 500$ MHz)	1.2	GHz
$-C_{re}$ typ. ($I_C = 2$ mA, $V_{CE} = 5$ V, $f = 1$ MHz)	0.6	pF
N typ. ($I_C = 2$ mA, $V_{CE} = 10$ V, Z_S opt.)	$f = 200$ MHz	3.3 dB
	$f = 800$ MHz	7.0 dB
G_p typ. ($I_C = 8$ mA, $V_{CE} = 10$ V)	$f = 200$ MHz	22 dB
	$f = 800$ MHz	7.0 dB
P_o typ. ($I_C = 8$ mA, $V_{CE} = 10$ V, $d_{im} = -30$ dB, v.s.w.r. at output ≈ 2)	$f = 200$ MHz	6.0 mW
	$f = 800$ MHz	6.0 mW

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72

B.S. 3934 SO-12A/SB4-3

For details see page 6



Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	30	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10\text{mA}$)	30	V
V_{CEO} max. ($I_C = 10\text{mA}$)	15	V
V_{EBO} max.	2.5	V
I_C max. (d.c.)	25	mA
I_{CM} max. (peak, $f > 1\text{MHz}$)	50	mA
P_{tot} max. ($T_{amb} \leq 25^\circ\text{C}$)	200	mW

Temperature

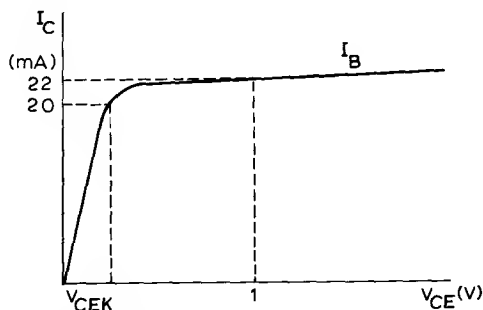
T_{stg} range	-65 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	0.88	degC/mW
$R_{th(j-case)}$	0.58	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 15\text{V}$	-	-	10 nA
V_{CEK}	Collector-emitter knee voltage $I_C = 20\text{mA}$, $I_B = \text{the value for}$ $I_C = 22\text{mA}$ at $V_{CE} = 1\text{V}$	-	-	0.75 V



h_{FE}	Static forward current transfer ratio			
	$I_C = 2\text{mA}$, $V_{CE} = 1\text{V}$	25	-	150
	$I_C = 25\text{mA}$, $V_{CE} = 1\text{V}$	20	-	125

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFX89

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
f_T	*Transition frequency				
	$I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$	-	1.0	-	GHz
	$I_C = 25\text{mA}$, $V_{CE} = 5\text{V}$, $f = 500\text{MHz}$	-	1.1	-	GHz
C_{tc}	**Collector capacitance				
	$I_E = I_e = 0$, $V_{CB} = 10\text{V}$, $f = 1\text{MHz}$	-	-	1.7	pF
$-C_{re}$	*Feedback capacitance				
	$I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$, $f = 1\text{MHz}$	-	0.6	-	pF
N	*Noise figure				
	$I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$,				
	$f = 200\text{MHz}$, $Z_S = \text{opt.}$	-	-	4.0	dB
	$f = 500\text{MHz}$, $R_S = 50\Omega$	-	-	6.5	dB
	$f = 800\text{MHz}$, $Z_S = \text{opt.}$	-	7.0	-	dB
G_p	*Power gain (not neutralised)				
	$I_C = 8\text{mA}$, $V_{CE} = 10\text{V}$, $f = 200\text{MHz}$	19	22	-	dB
	$f = 800\text{MHz}$	-	7.0	-	dB

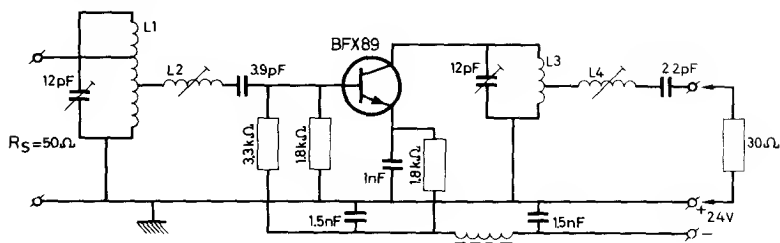
*Fourth lead (case) grounded.

**Fourth lead (case) not connected.

Intermodulation characteristics

P_o	*Output power (see test circuits 1 and 2)				
	$I_C = 8\text{mA}$, $V_{CE} = 10\text{V}$, v.s.w.r. at output < 2,				
	$d_{im} = -30\text{dB}$				
	$f = 200\text{MHz}$, $f_p = 202\text{MHz}$, $f_q = 205\text{MHz}$,				
	$f_{(2q-p)} = 208\text{MHz}$ (channel 9)	-	6.0	-	mW
	$f = 800\text{MHz}$, $f_p = 798\text{MHz}$, $f_q = 802\text{MHz}$,				
	$f_{(2q-p)} = 806\text{MHz}$ (channel 62)	-	6.0	-	mW
d_{im}	Intermodulation distortion (see test circuit 3)				
	$I_C = 8\text{mA}$, $V_{CE} = 6\text{V}$, $R_L = 37.5\Omega$,				
	$V_o = 100\text{mV}$ at $f_p = 183\text{MHz}$				
	$V_o = 100\text{mV}$ at $f_q = 200\text{MHz}$				
	$f_{(2q-p)} = 217\text{MHz}$	-	-40	-	dB

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TEST CIRCUIT 1 - OUTPUT POWER TEST CIRCUIT ($f = 200\text{MHz}$)

L1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.

L2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.

L3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.

L4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

ADJUSTMENT OF TEST CIRCUIT

Technical considerations

Intermodulation distortion is caused by clipping in h.f. output current and voltage.

The maximum undistorted output power is attained when

- a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{\text{load}} = (V_{\text{CE}} - V_{\text{cek}})/I_{\text{C}}$$

Where V_{cek} is the high frequency knee voltage

- b) The h.f. collector current is as low as possible; this occurs if

$$-C_{\text{load}} = +C_{\text{oe}}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input.

Experimentally obtained values of R_{load} and C_{load} , for maximum output power at an intermodulation factor of -30dB, are:

$$R_{\text{load}} = 1\text{k}\Omega, C_{\text{load}} = -1.8\text{pF}$$

Procedure

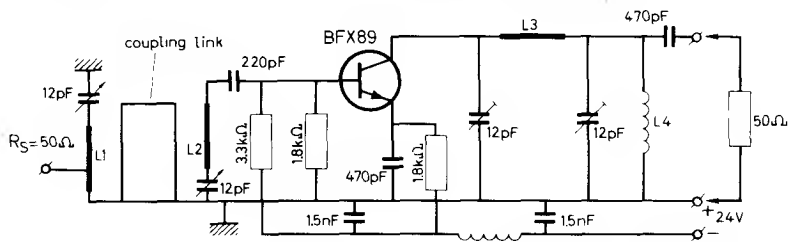
1. Remove the transistor and connect a dummy, consisting of a 220Ω resistor in parallel with a 5.6pF capacitor, between the collector and the emitter connections of the output circuit.
2. Tune and match the output circuit for zero reflection at 205MHz (i.e. v.s.w.r. = 1). After this adjustment no further change should be made in the output circuit.
3. Replace the dummy by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L2.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFX89

ELECTRICAL CHARACTERISTICS (cont'd)

TEST CIRCUIT 2 - OUTPUT POWER TEST CIRCUIT ($f = 800\text{MHz}$)



L1 = $24 \times 6 \times 0.5\text{mm}$ silver plated copper strip, input tap at 5mm from earth.

L2 = $15 \times 6 \times 0.5\text{mm}$ silver plated copper strip.

L3 = $20 \times 8 \times 0.5\text{mm}$ silver plated copper strip.

L4 = 4 turns of 0.5mm enamelled copper wire, winding pitch 1.5mm, int. dia. 4mm.

Coupling link = 42mm of 1mm silver plated copper wire.

ADJUSTMENT OF TEST CIRCUIT

At 800MHz a dummy cannot be used to adjust for optimum collector load, because at these frequencies the impedance transformations of the dummy are too high.

A small signal with a frequency of the midchannel 802MHz is fed to the input. The signal is increased until clipping occurs, that is until the output power no longer increases linearly with increasing input signal. Care should be taken not to allow the voltage swing to exceed the V_{CEr} value as this may result in the destruction of the transistor by second breakdown. The output circuit is then tuned to eliminate clipping.

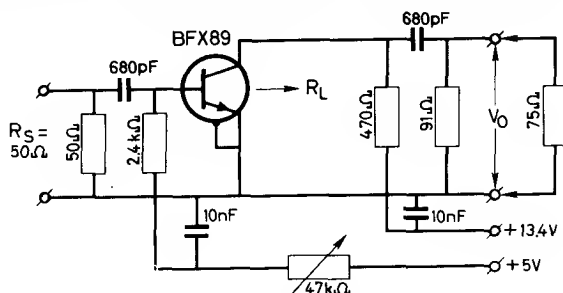
The output power P_o is given by

$$P_o = I_C (V_{CE} - V_{cek}) / 2 = 35\text{mW}$$

Where V_{cek} is the high frequency knee voltage

Keeping the input signal as small as possible at $P_o = 35\text{mW}$, the output circuit is adjusted for minimum intermodulation. The input circuit is then adjusted for maximum gain and good bandpass curve. The v.s.w.r. is found to be ≤ 2 over the whole channel.

TEST CIRCUIT 3 - INTERMODULATION DISTORTION TEST CIRCUIT

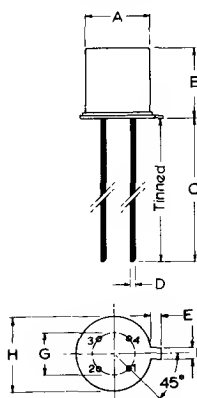


SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

OUTLINE, DIMENSIONS AND CONNECTIONS

Conforms to J.E.D.E.C. TO-72



Viewed from underside

Millimetres

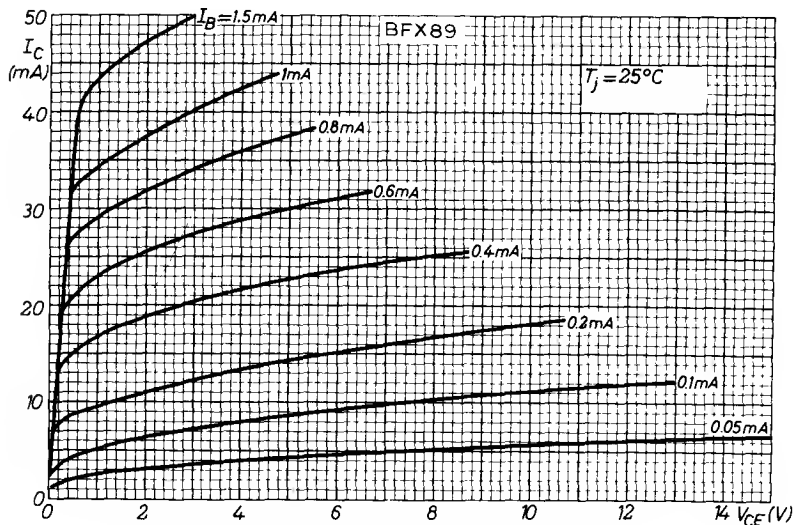
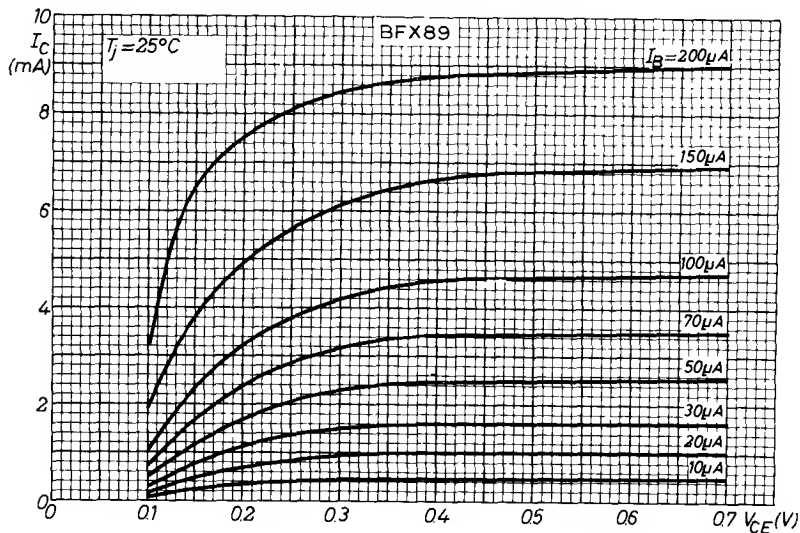
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections

- | | |
|------------|---------------------------------|
| 1. Emitter | 3. Collector |
| 2. Base | 4. Shield connected to envelope |

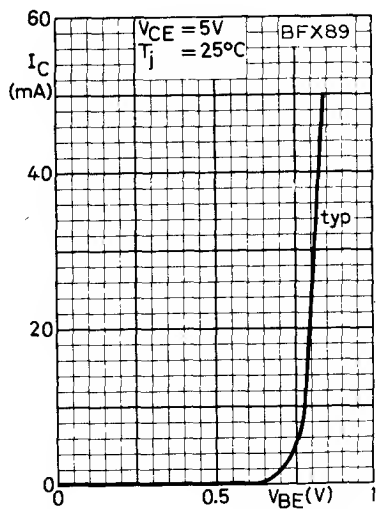
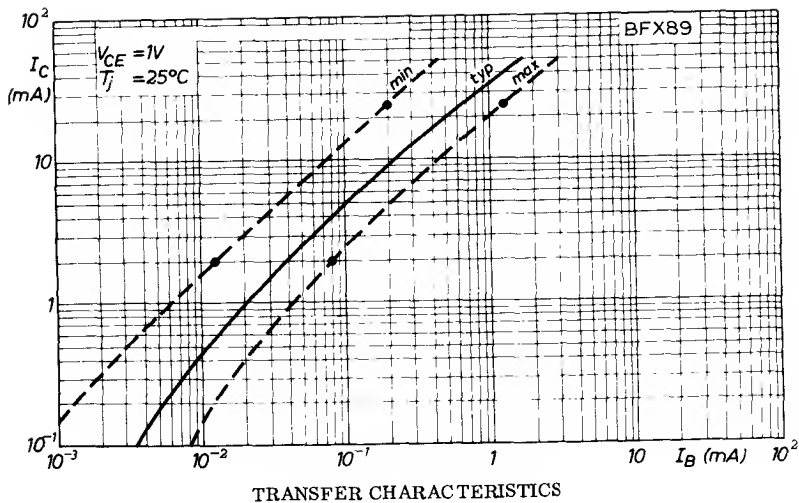
**N-P-N SILICON
PLANAR EPITAXIAL TRANSISTOR**

BFX89



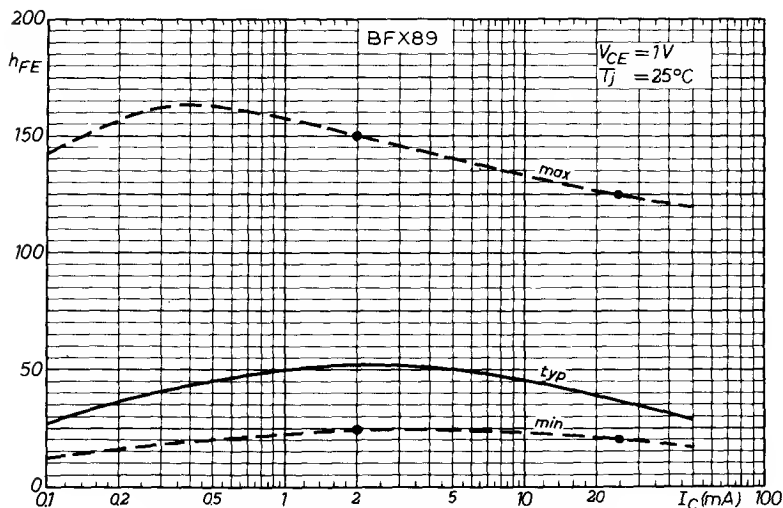
TYPICAL OUTPUT CHARACTERISTICS AT LOW AND HIGH
COLLECTOR-EMITTER VOLTAGES

Mullard

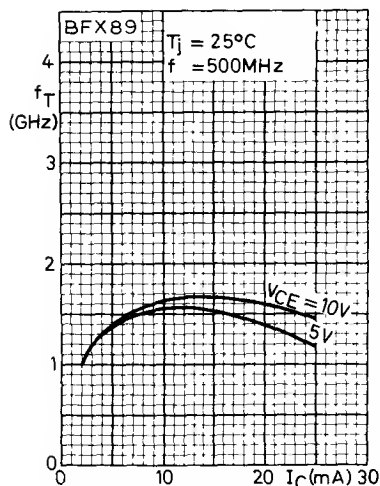


N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

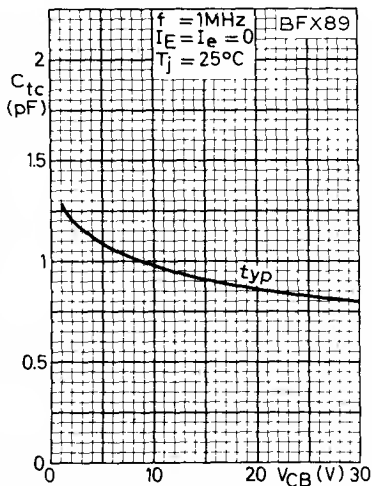
BFX89



STATIC FORWARD CURRENT TRANSFER RATIO
PLOTTED AGAINST COLLECTOR CURRENT

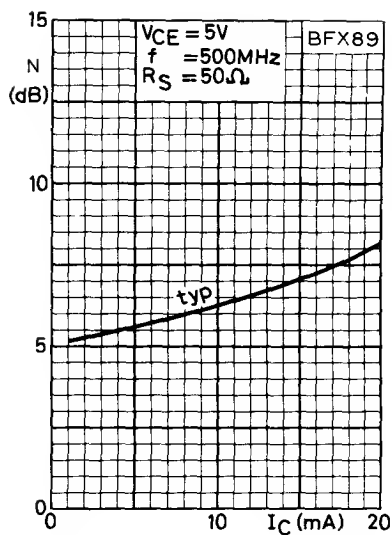


Typical transition frequency versus
collector current

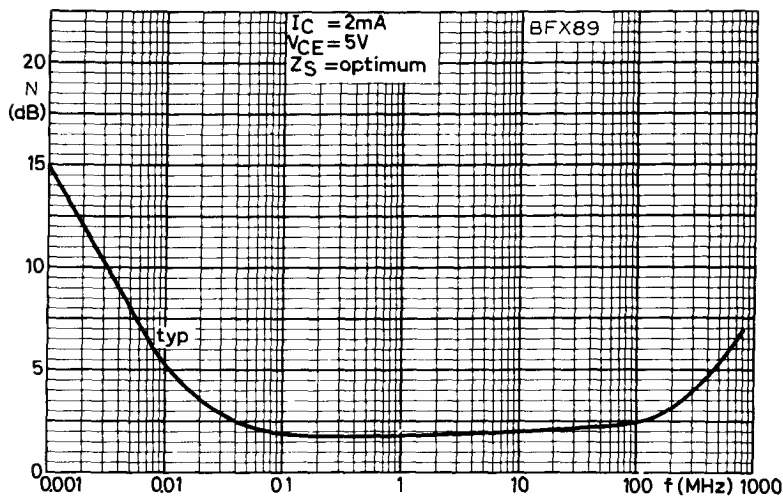


Typical collector capacitance versus
collector-base voltage

Mullard



TYPICAL NOISE FIGURE PLOTTED AGAINST COLLECTOR CURRENT



TYPICAL NOISE FIGURE PLOTTED AGAINST FREQUENCY

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52

Also available to BS9365—F012

Silicon n-p-n planar epitaxial transistors for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

QUICK REFERENCE DATA

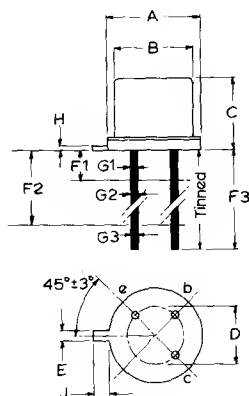
	BFY50	BFY51	BFY52	
V_{CBO} max.	80	60	40	V
V_{CEO} max.	35	30	20	V
I_{CM} max.	1.0	1.0	1.0	A
P_{tot} max. $T_{amb} \leq 25^{\circ}C$	800	800	800	mW
$T_{case} \leq 100^{\circ}C$	2.86	2.86	2.86	W
h_{FE} ($I_C = 150mA$, $V_{CE} = 10V$) min.	30	40	60	
typ.	112	123	142	
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^{\circ}C$)	50	50	50	MHz

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

Millimetres



	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

The collector is electrically connected to the envelope

Mullard

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 35\text{MHz}$, $T_{\text{amb}} = 25^\circ\text{C}$	60	140	-	MHz

Saturated switching times

$I_C = 150\text{mA}$, $I_{B(\text{on})} = -I_{B(\text{off})} = 15\text{mA}$,
 $-V_{EE} = 10\text{V}$, $-V_{BE(\text{off})} \approx 2.0\text{V}$

t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns

h-parameters

h_{fe}	$I_C = 1.0\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 1.0\text{kHz}$, $T_{\text{amb}} = 25^\circ\text{C}$	10	65	-	
h_{ie}	$I_C = 10\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 1.0\text{kHz}$, $T_{\text{amb}} = 25^\circ\text{C}$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		15	80	-	
h_{oe}		-	35	80	μmho

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52

BFY51

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 60\text{V}, I_E = 0$	-	10	500	nA
	$V_{CB} = 60\text{V}, I_E = 0, T_j = 100^\circ\text{C}$	-	0.5	30	μA
	$V_{CB} = 40\text{V}, I_E = 0$	-	2.0	50	nA
	$V_{CB} = 40\text{V}, I_E = 0, T_j = 100^\circ\text{C}$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0\text{V}, I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0\text{V}, I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0\text{V}, I_C = 0, T_j = 100^\circ\text{C}$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 10\text{mA}, V_{CE} = 10\text{V}$	30	85	-	
	$I_C = 150\text{mA}, V_{CE} = 10\text{V}$	40	123	-	
	$I_C = 500\text{mA}, V_{CE} = 10\text{V}$	25	79	-	
	$I_C = 1.0\text{A}, V_{CE} = 10\text{V}$	15	40	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10\text{mA}, I_B = 1.0\text{mA}$	-	0.06	0.15	V
	$I_C = 150\text{mA}, I_B = 15\text{mA}$	-	0.15	0.35	V
	$I_C = 500\text{mA}, I_B = 50\text{mA}$	-	0.35	1.00	V
	$I_C = 1.0\text{A}, I_B = 100\text{mA}$	-	0.66	1.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10\text{mA}, I_B = 1.0\text{mA}$	-	0.69	1.2	V
	$I_C = 150\text{mA}, I_B = 15\text{mA}$	-	0.92	1.3	V
	$I_C = 500\text{mA}, I_B = 50\text{mA}$	-	1.15	1.5	V
	$I_C = 1.0\text{A}, I_B = 100\text{mA}$	-	1.40	2.0	V
C_{Tc}	Collector capacitance				
	$V_{CB} = 10\text{V}, I_E = I_e = 0,$ $f = 1.0\text{MHz}$	-	7.0	12	pF

Mullard

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 35\text{MHz}$, $T_{\text{amb}} = 25^\circ\text{C}$	50	160	-	MHz

Saturated switching times

$$I_C = 150\text{mA}, I_{B(\text{on})} = -I_{B(\text{off})} = 15\text{mA},$$

$$-V_{EE} = 10\text{V}, -V_{BE(\text{off})} = 2.0\text{V}$$

t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns

h-parameters

h_{fe}	$I_C = 1.0\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 1.0\text{kHz}$, $T_{\text{amb}} = 25^\circ\text{C}$	20	65	-	
h_{ie}	$I_C = 10\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 1.0\text{kHz}$, $T_{\text{amb}} = 25^\circ\text{C}$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52

BFY52

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{\text{CB}} = 40\text{V}, I_{\text{E}} = 0$	-	10	500	nA
	$V_{\text{CB}} = 40\text{V}, I_{\text{E}} = 0, T_j = 100^{\circ}\text{C}$	-	0.5	30	μA
	$V_{\text{CB}} = 30\text{V}, I_{\text{E}} = 0$	-	2.0	50	nA
	$V_{\text{CB}} = 30\text{V}, I_{\text{E}} = 0, T_j = 100^{\circ}\text{C}$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{\text{EB}} = 6.0\text{V}, I_{\text{C}} = 0$	-	10	500	nA
	$V_{\text{EB}} = 5.0\text{V}, I_{\text{C}} = 0$	-	2.0	50	nA
	$V_{\text{EB}} = 5.0\text{V}, I_{\text{C}} = 0, T_j = 100^{\circ}\text{C}$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_{\text{C}} = 10\text{mA}, V_{\text{CE}} = 10\text{V}$	30	90	-	
	$I_{\text{C}} = 150\text{mA}, V_{\text{CE}} = 10\text{V}$	60	142	-	
	$I_{\text{C}} = 500\text{mA}, V_{\text{CE}} = 10\text{V}$	30	90	-	
	$I_{\text{C}} = 1.0\text{A}, V_{\text{CE}} = 10\text{V}$	15	50	-	
$V_{\text{CE(sat)}}$	Collector-emitter saturation voltage				
	$I_{\text{C}} = 10\text{mA}, I_{\text{B}} = 1.0\text{mA}$	-	0.06	0.15	V
	$I_{\text{C}} = 150\text{mA}, I_{\text{B}} = 15\text{mA}$	-	0.15	0.35	V
	$I_{\text{C}} = 500\text{mA}, I_{\text{B}} = 50\text{mA}$	-	0.35	1.00	V
	$I_{\text{C}} = 1.0\text{A}, I_{\text{B}} = 100\text{mA}$	-	0.66	1.60	V
$V_{\text{BE(sat)}}$	Base-emitter saturation voltage				
	$I_{\text{C}} = 10\text{mA}, I_{\text{B}} = 1.0\text{mA}$	-	0.69	1.2	V
	$I_{\text{C}} = 150\text{mA}, I_{\text{B}} = 15\text{mA}$	-	0.92	1.3	V
	$I_{\text{C}} = 500\text{mA}, I_{\text{B}} = 50\text{mA}$	-	1.15	1.5	V
	$I_{\text{C}} = 1.0\text{A}, I_{\text{B}} = 100\text{mA}$	-	1.40	2.0	V
C_{Tc}	Collector capacitance				
	$V_{\text{CB}} = 10\text{V}, I_{\text{E}} = I_{\text{C}} = 0,$ $f = 1.0\text{MHz}$	-	7.0	12	pF

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ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency				
	$I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$,				
	$f = 35\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	50	185	-	MHz

Saturated switching times

$$I_C = 150\text{mA}, I_{B(on)} = -I_{B(off)} = 15\text{mA},$$

$$-V_{EE} = 10\text{V}, -V_{BE(off)} = 2.0\text{V}$$

t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns

h-parameters

$$h_{fe} \quad I_C = 1.0\text{mA}, V_{CE} = 5.0\text{V},$$

$$f = 1.0\text{kHz}, T_{amb} = 25^\circ\text{C}$$

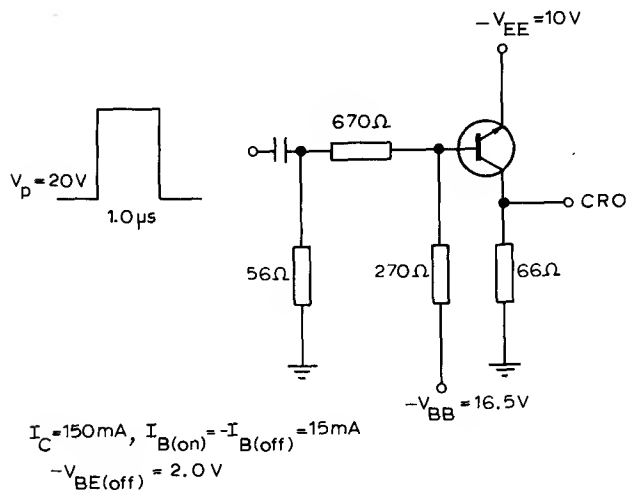
h_{ie}	$\left. \begin{array}{l} \\ \\ \\ \end{array} \right\} \quad I_C = 10\text{mA}, V_{CE} = 5.0\text{V},$ $f = 1.0\text{kHz}, T_{amb} = 25^\circ\text{C}$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

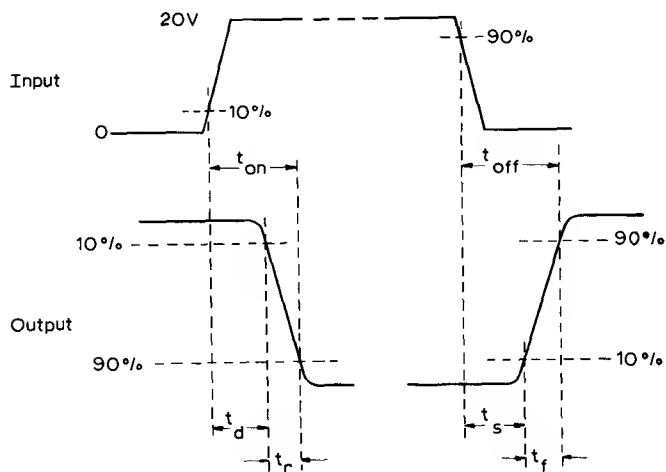
BFY50
BFY51
BFY52

MEASUREMENT OF SATURATED SWITCHING TIMES

Test circuit



Switching waveforms



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OPERATING NOTES

1. Dissipation and heatsink considerations

a) Steady-state conditions

The maximum steady-state dissipation P_s is given by the relationship:

$$P_{s \text{ max.}} = \frac{T_{j \text{ max.}} - T_{\text{amb}}}{R_{\text{th(j-amb)}}$$

Where $T_{j \text{ max.}}$ is the maximum permissible operating junction temperature,

T_{amb} is the ambient temperature,

$R_{\text{th(j-amb)}}$ is the total thermal resistance between junction and ambient.

Page 13 gives the maximum allowable steady-state dissipation versus ambient temperature for the device mounted in free air and with infinite heatsink.

b) Pulse conditions (rectangular pulses)

The maximum pulse power P_p is given by the formula

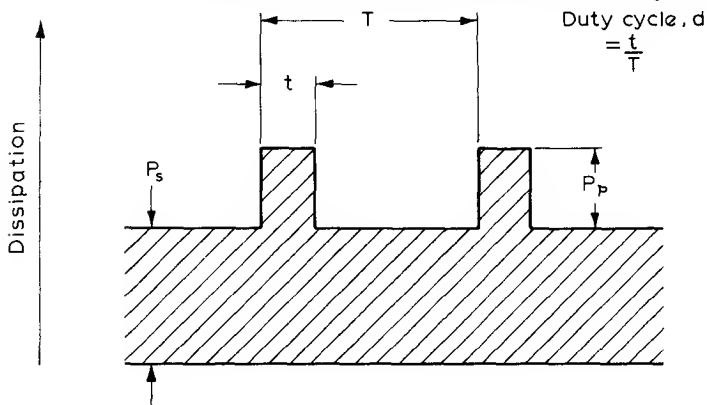
$$P_p = \frac{(T_{j \text{ max.}} - T_{\text{amb}}) - (P_s \cdot R_{\text{th(j-amb)})}}{R_{\text{th(t)}} + d \cdot R_{\text{th(case-amb)}}$$

Where P_s is the steady-state dissipation excluding that in the pulses,

$R_{\text{th(t)}}$ is effective transient thermal resistance of the device between junction and case, and is a function of the pulse duration t , and duty cycle d ,

d is the duty cycle, and is equal to the pulse duration t divided by the periodic time T ,

$R_{\text{th(case-amb)}}$ is the total thermal resistance between case and ambient and is equal to the difference between $R_{\text{th(j-amb)}}$ and the thermal resistance from junction to case $R_{\text{th(j-case)}}$.



- b) Pulse conditions (rectangular pulses) (cont'd)

Example

The following example shows how to calculate the maximum permissible peak dissipation of a BFY50 mounted in free air at a temperature not exceeding 65°C. The steady-state dissipation under the bottomed condition is 350mW, the pulse width is 1ms and the duty cycle is 0.2.

The transient thermal resistance $R_{th(t)} = 15.5 \text{ degC/W}$ (page 13)

$$\begin{aligned} P_p \text{ max.} &= \frac{(200-65) - (0.35 \times 220)}{15.5 + 0.2(220-35)} \\ &= \frac{135-77}{15.5+37} \\ &= 1.1\text{W} \end{aligned}$$

The peak pulse dissipation of 1.1W is therefore allowed provided that the voltage and current ratings of the device are not exceeded.

- c) Pulse conditions (other than rectangular)

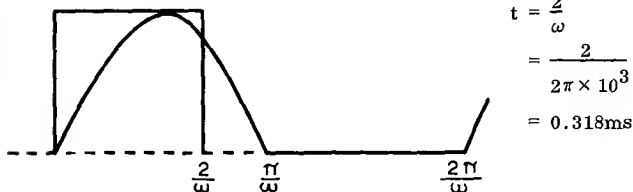
For sinusoidal and irregular shaped waveforms, the power pulse is converted to an equivalent rectangular pulse of the same average and peak values, and treated as in the previous section.

Example

The following example illustrates how to find the maximum permissible peak dissipation of a BFY52 operating in a class 'B' circuit at 1kHz. The device is mounted on a heatsink of thermal resistance equal to 50degC/W and at an ambient temperature not exceeding 100°C. Assuming that the waveform is sinusoidal for half period and zero for the other half.

$$\text{Average of sinewave over half cycle} = \frac{2P_p}{\pi}$$

Therefore equivalent rectangular pulse width of same amplitude and average value



83559

$$\text{Duty cycle, } d = \frac{1}{\pi}$$

c) Pulse conditions (other than rectangular) (cont'd)

$$\text{Duty cycle, } d = \frac{2}{\omega} \left/ \frac{2\pi}{\omega} \right. = \frac{1}{\pi} = 0.318$$

From page 13

$$R_{th(t)} = 6.8 \text{degC/W (d=0)}$$

$$R_{th(s)} = 35 \text{degC/W}$$

$$\begin{aligned} R_{th(t)} \text{ at } d=0.318 &= (35-6.8) \times 0.318 + 6.8 \\ &= 15.8 \text{degC/W} \end{aligned}$$

$$P_p \text{ max.} = \frac{(200 - 100) - 0}{15.8 + 0.318 \times 50}$$

$$= \frac{100}{31.7} = 3.15 \text{W}$$

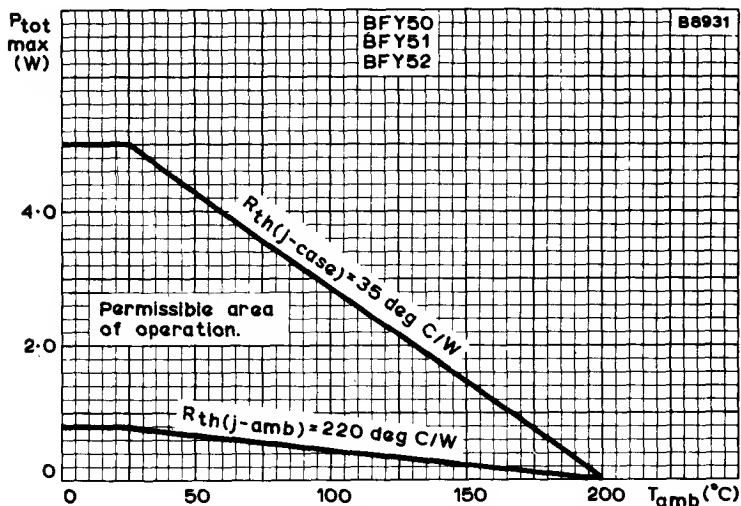
A peak power of 3.15W is therefore permissible provided that the voltage and current ratings of the device are not exceeded.

SOLDERING AND WIRING RECOMMENDATIONS

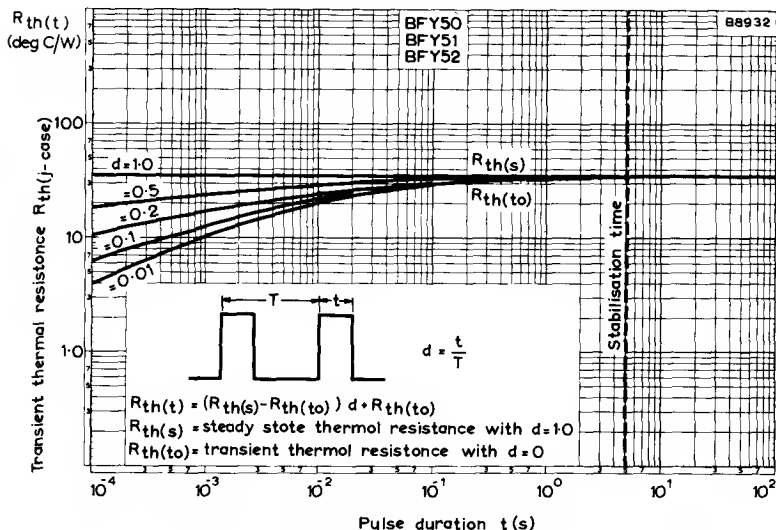
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
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BFY52

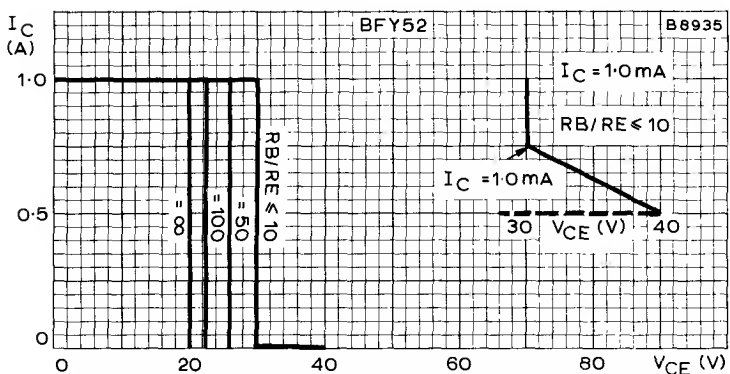
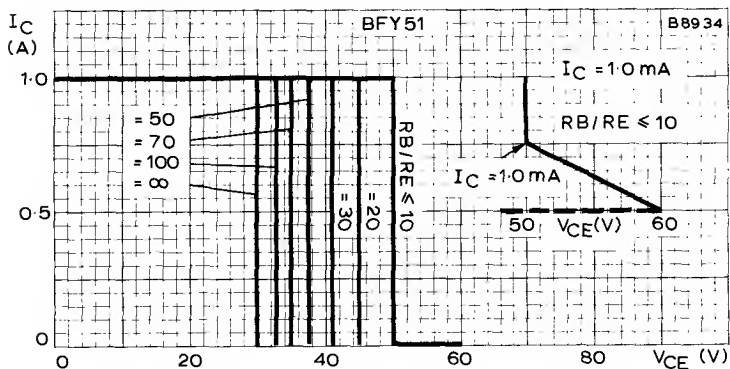
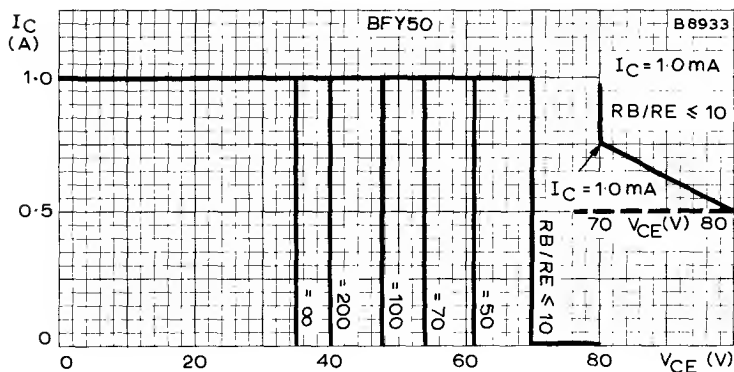


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST
AMBIENT TEMPERATURE



TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS
PLOTTED AGAINST PULSE DURATION

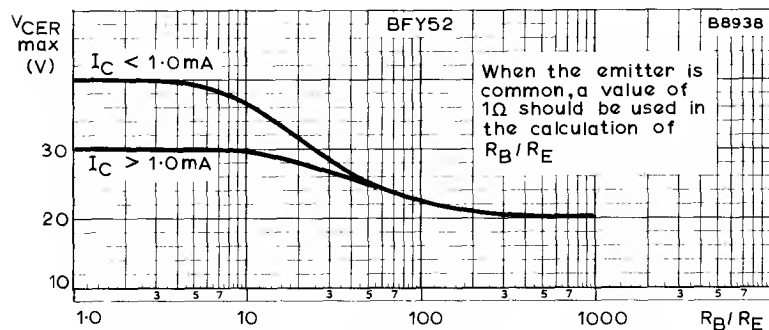
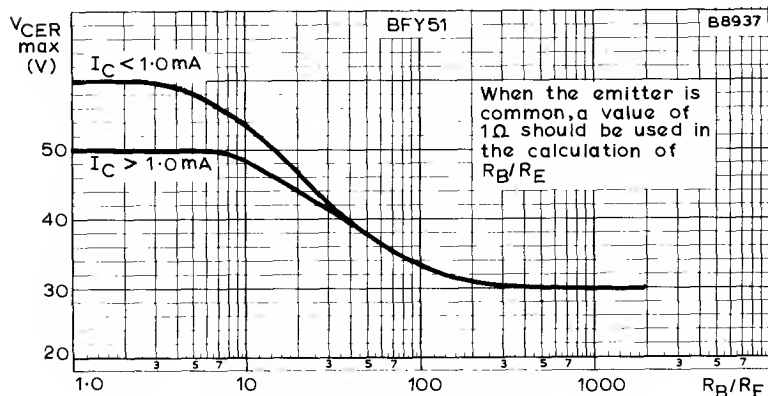
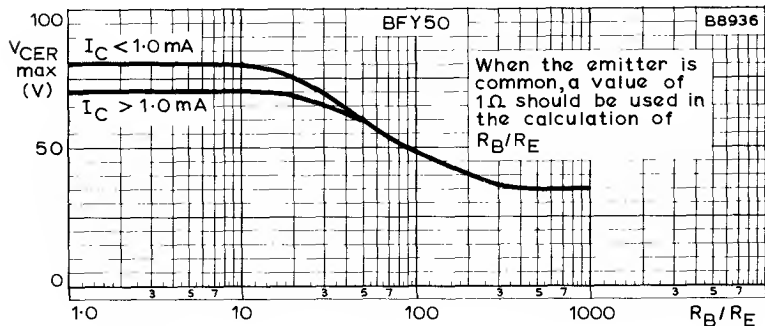
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COLLECTOR CURRENT PLOTTED AGAINST MAXIMUM
COLLECTOR-EMITTER VOLTAGE WITH R_B/R_E AS PARAMETER

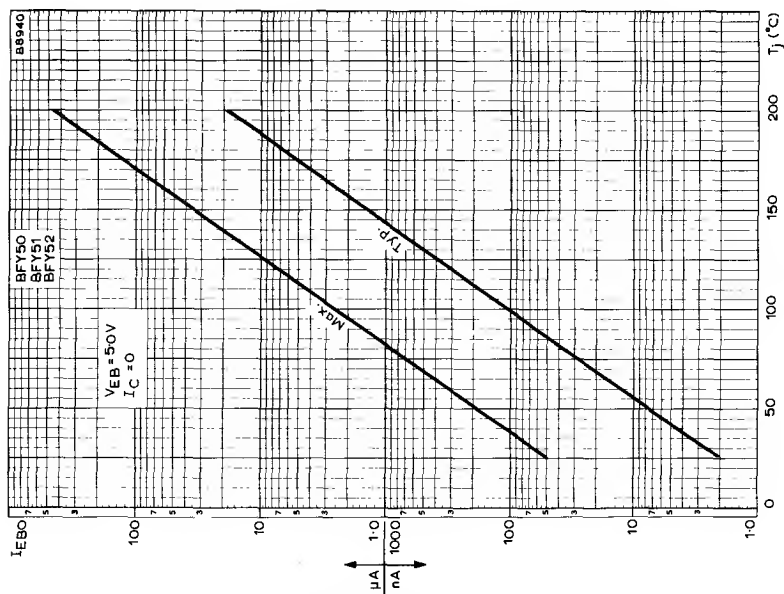
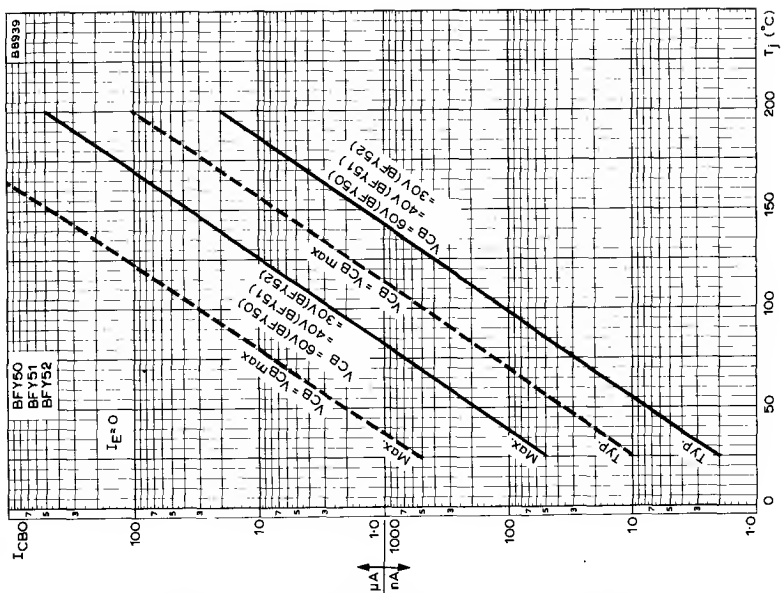
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52



MAXIMUM COLLECTOR-EMITTER VOLTAGE PLOTTED AGAINST
 R_B/R_E RATIO

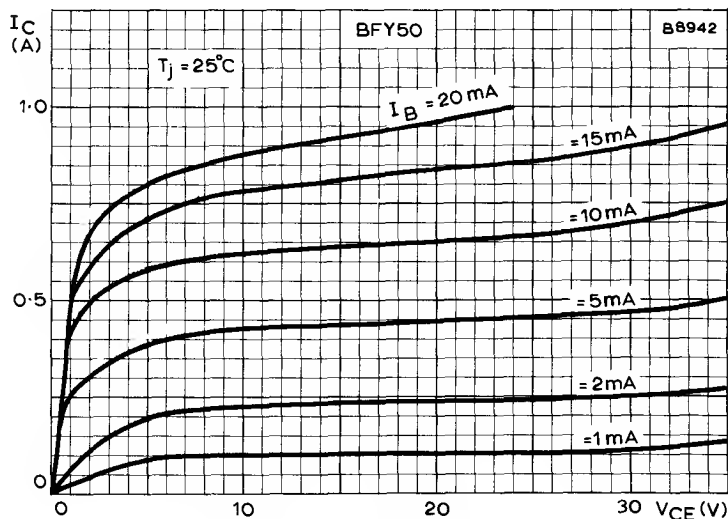
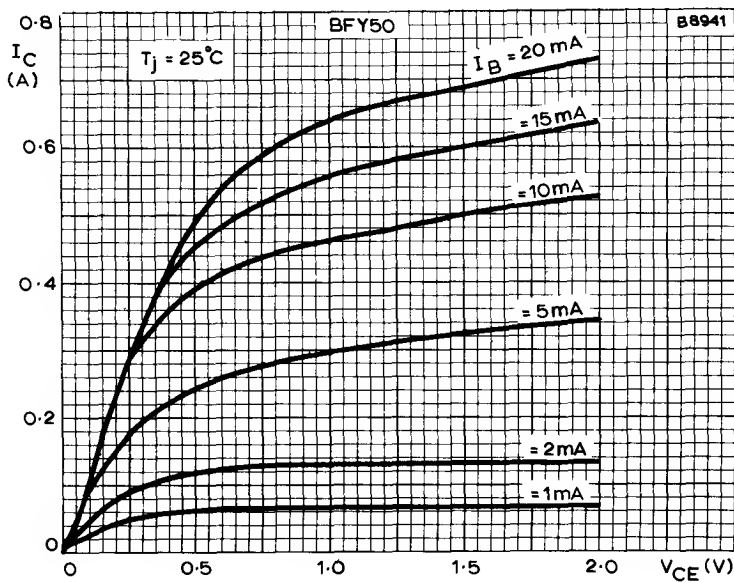
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COLLECTOR AND EMITTER CUT-OFF CURRENTS PLOTTED
AGAINST JUNCTION TEMPERATURE

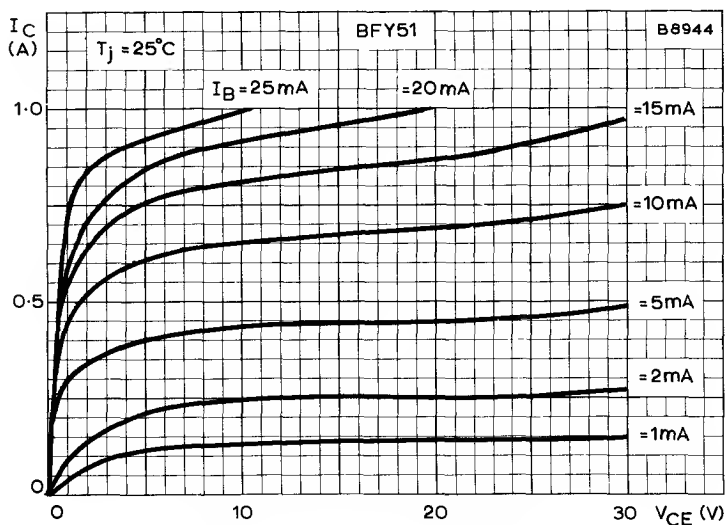
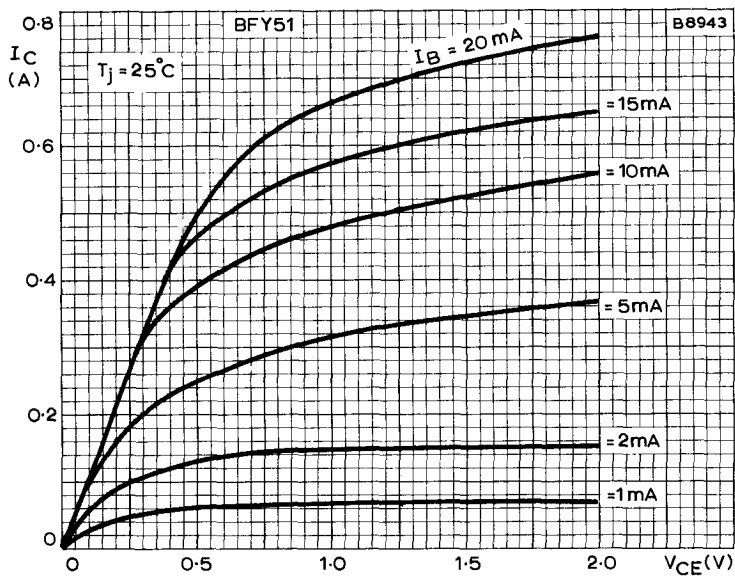
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52



TYPICAL OUTPUT CHARACTERISTICS

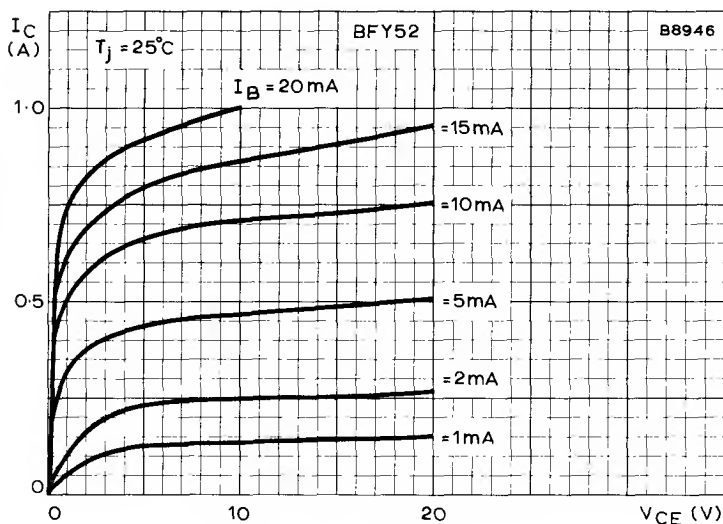
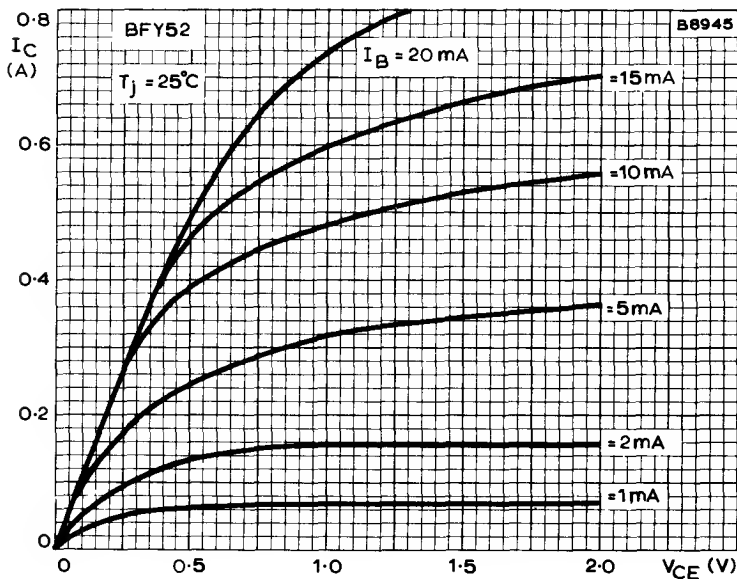
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TYPICAL OUTPUT CHARACTERISTICS

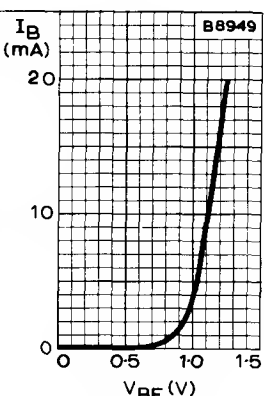
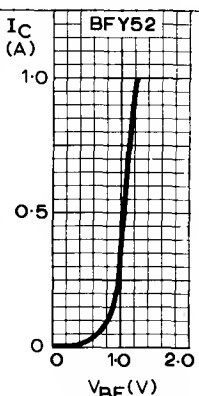
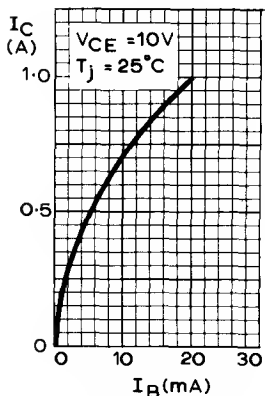
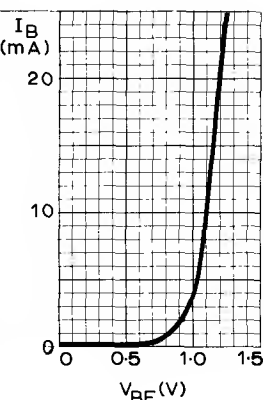
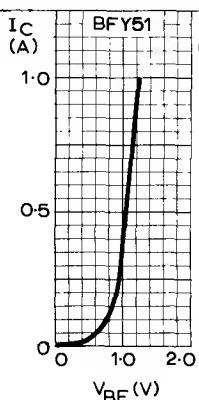
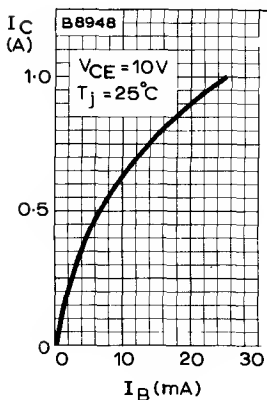
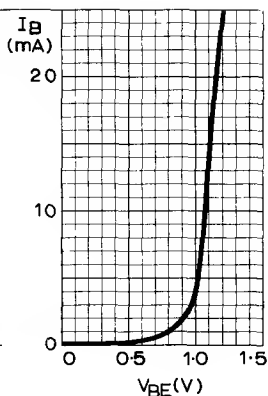
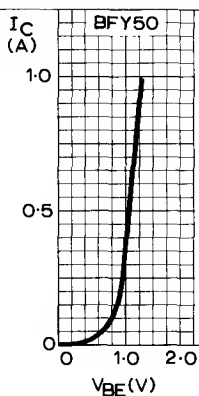
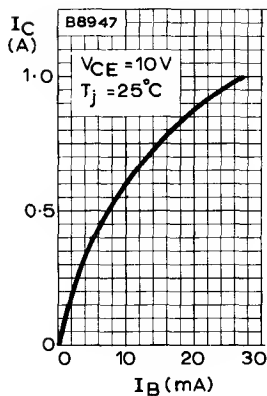
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52



TYPICAL OUTPUT CHARACTERISTICS

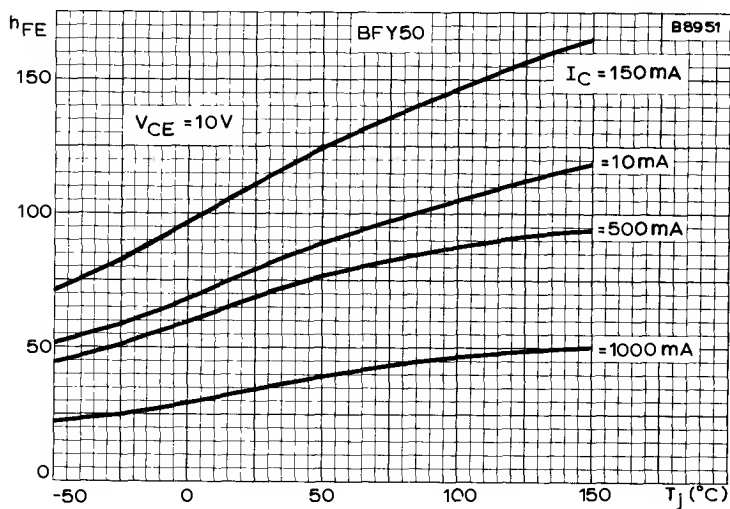
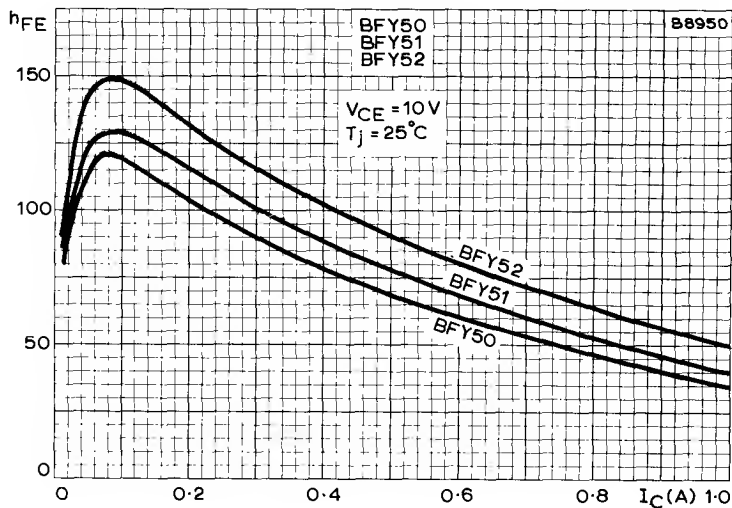
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TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS

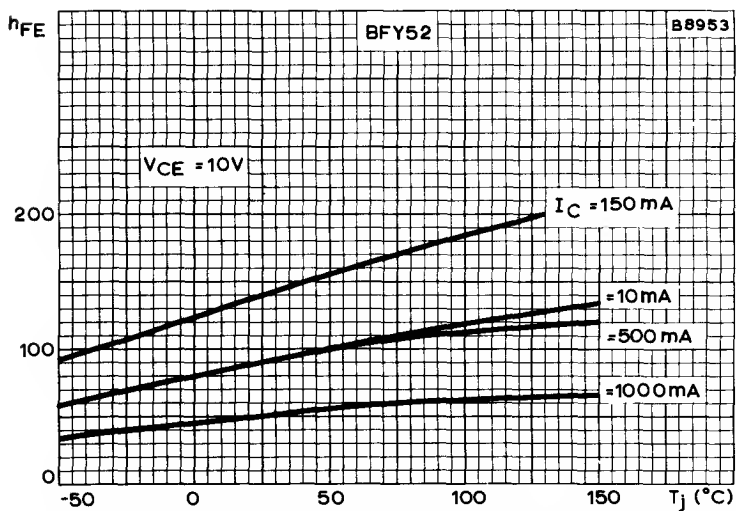
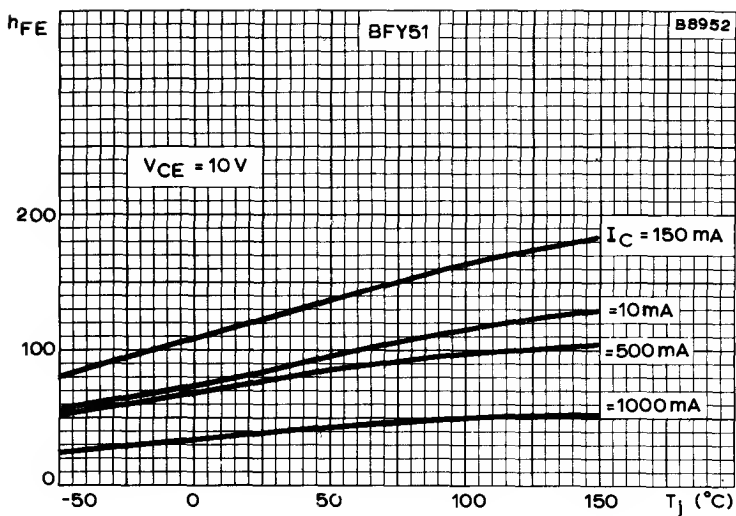
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52



TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED
AGAINST COLLECTOR CURRENT AND JUNCTION TEMPERATURE

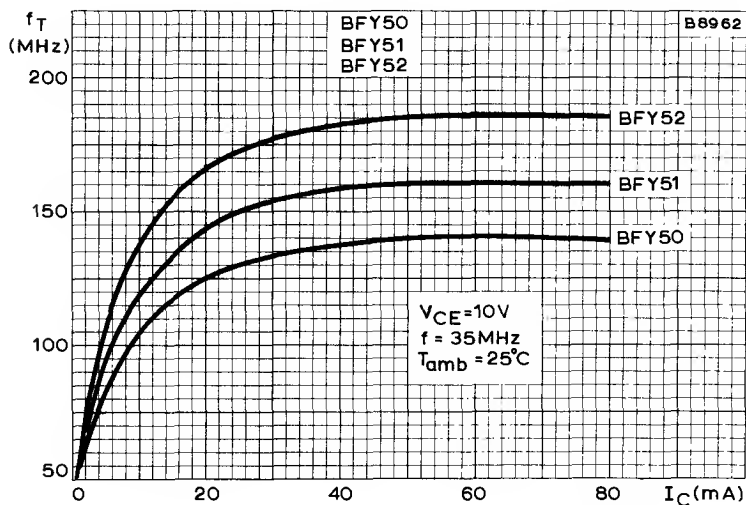
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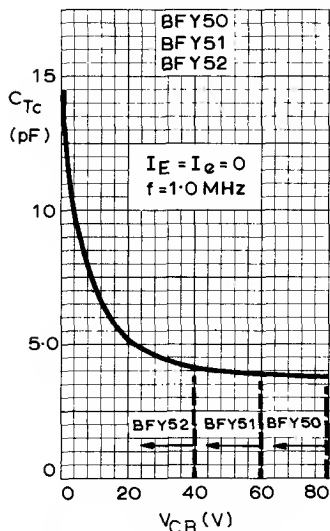
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED
 AGAINST JUNCTION TEMPERATURE

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

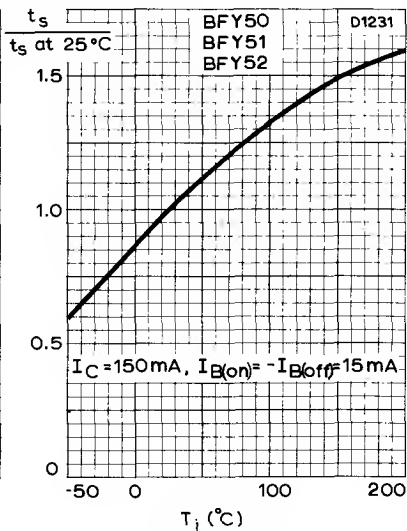
BFY50
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BFY52



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST
COLLECTOR CURRENT

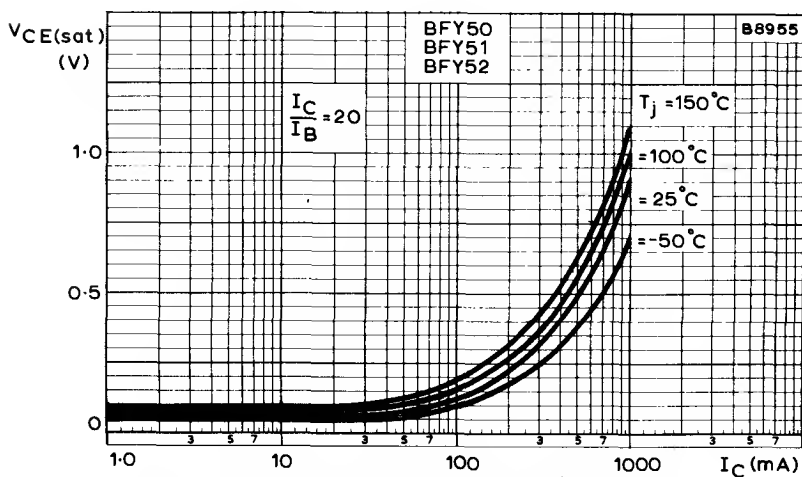
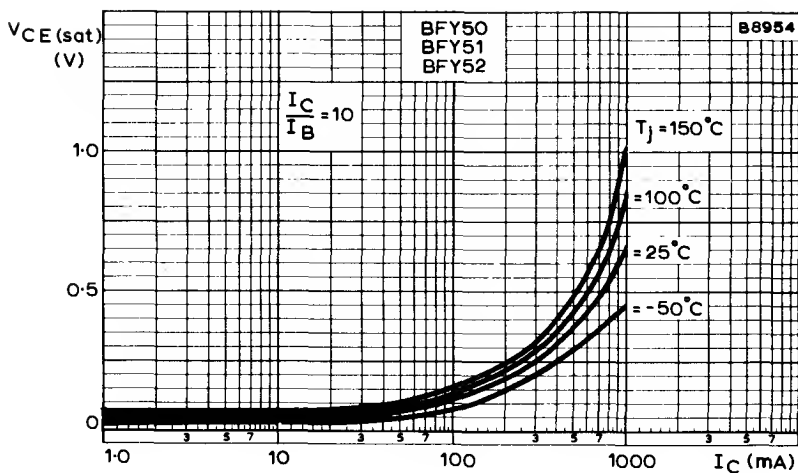


Typical collector capacitance versus
collector-base voltage



Typical storage time
normalised at $25^\circ C$

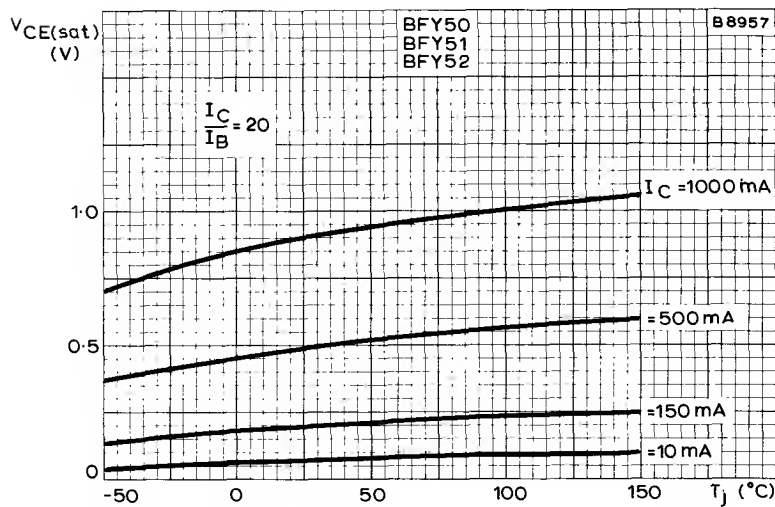
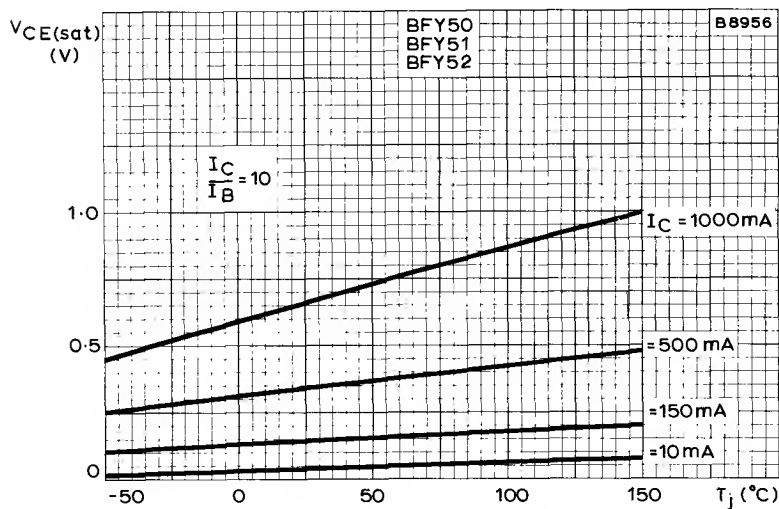
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TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT

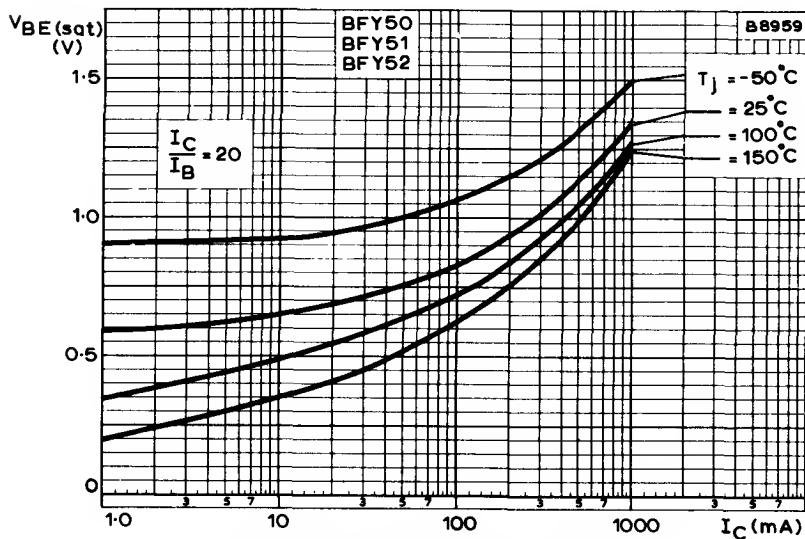
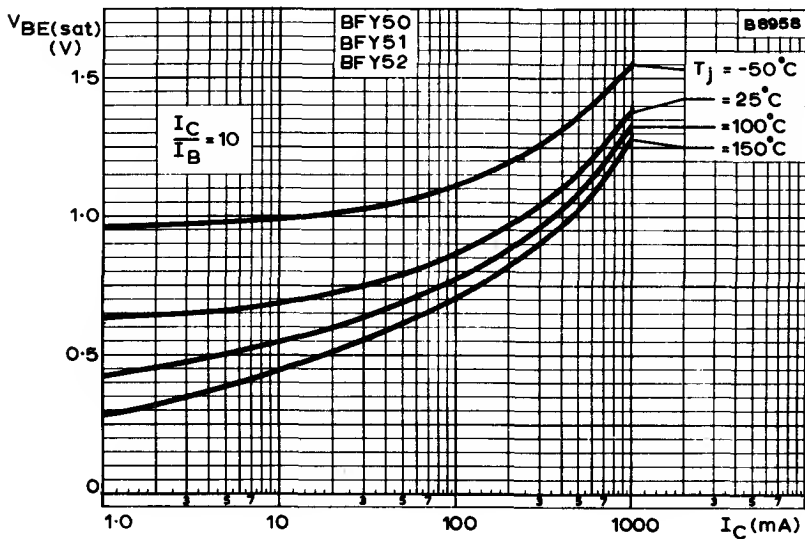
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE

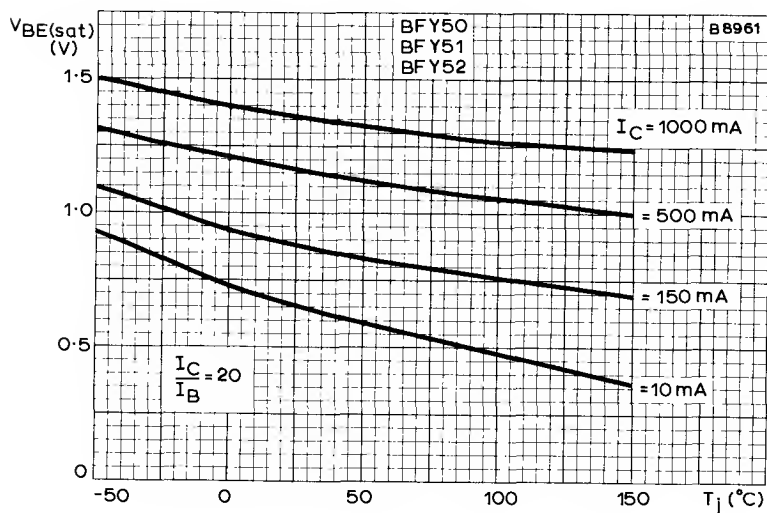
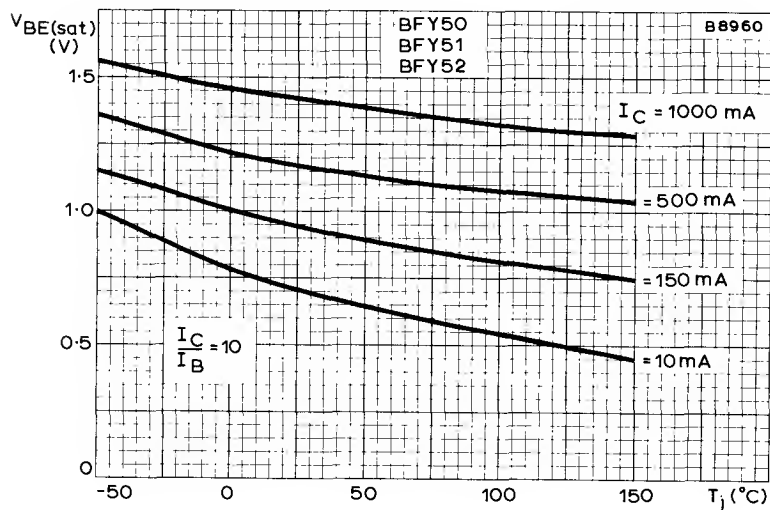
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TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT

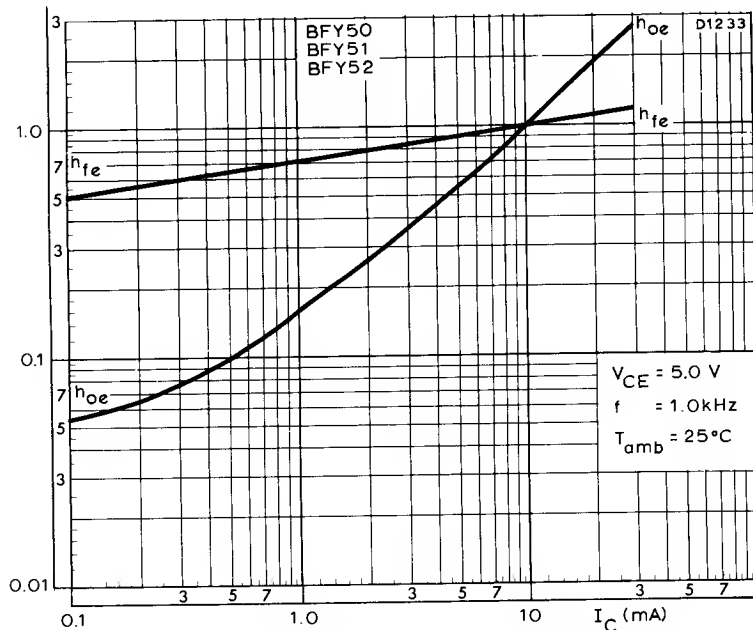
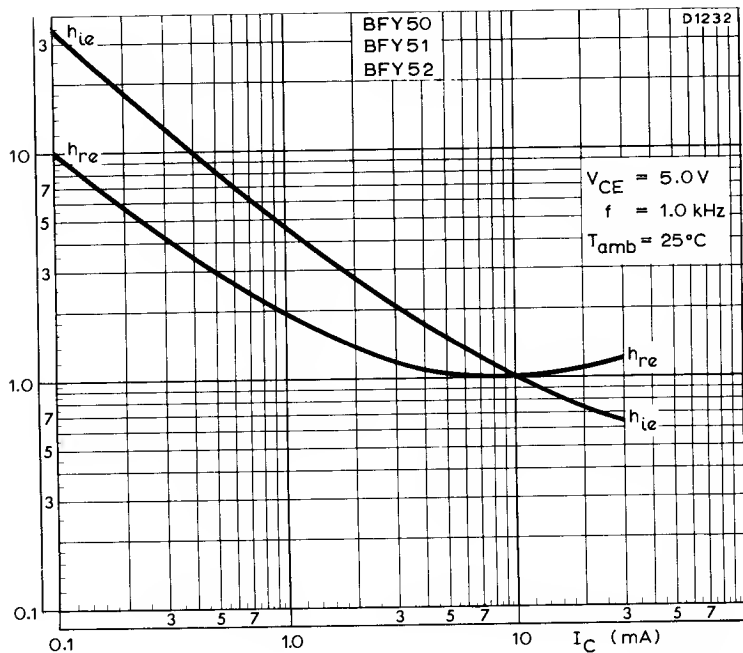
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52



TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE

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TYPICAL h-PARAMETERS NORMALISED AT $I_C = 10\text{mA}$

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFY53

Silicon n-p-n planar epitaxial transistor for general purpose industrial applications.
Encapsulated in TO-5 envelope with the collector connected to can.

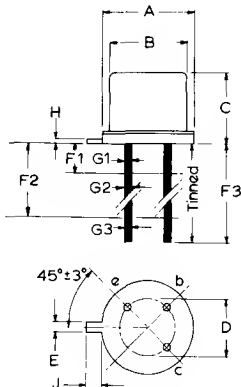
QUICK REFERENCE DATA

V_{CBO} max.	40	V
V_{CEO} max.	20	V
I_{CM} max.	1.0	A
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	800	mW
($T_{case} \leq 25^{\circ}C$)	5.0	W
h_{FE} ($I_C = 150mA$, $V_{CE} = 10V$) min.	30	
typ.	75	
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^{\circ}C$)	50	MHz

OUTLINE AND DIMENSIONS

Conforms to BS3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

	Millimetres		
	Min.	Nom.	Max.
A	9.1	-	9.4
B	8.2	-	8.5
C	6.1	-	6.6
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	0.3	-	0.8
J	0.74	-	1.0



Collector connected to can

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	40	V
V_{CE} max. (cut-off, $I_C \leq 1\text{mA}$)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	6.0	V
I_C max.	1.0	A
I_{CM} max.	1.0	A
$-I_E$ max.	1.0	A
$-I_{EM}$ max.	1.0	A
I_B max.	100	mA
$\pm I_{BM}$ max.	100	mA
P_{tot} max. ($T_{amb} \leq 25^\circ\text{C}$)	800	mW
$(T_{case} \leq 25^\circ\text{C})$	5.0	W

Temperature

T_{stg} range	-65 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	220	degC/W
$R_{th(j-case)}$	35	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 40\text{V}, I_E = 0$	-	10	500	nA
	$V_{CB} = 40\text{V}, I_E = 0, T_j = 100^\circ\text{C}$	-	0.5	30	μA
	$V_{CB} = 30\text{V}, I_E = 0$	-	2.0	50	nA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0\text{V}, I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0\text{V}, I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0\text{V}, I_C = 0, T_j = 100^\circ\text{C}$	-	0.1	2.5	μA

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFY53

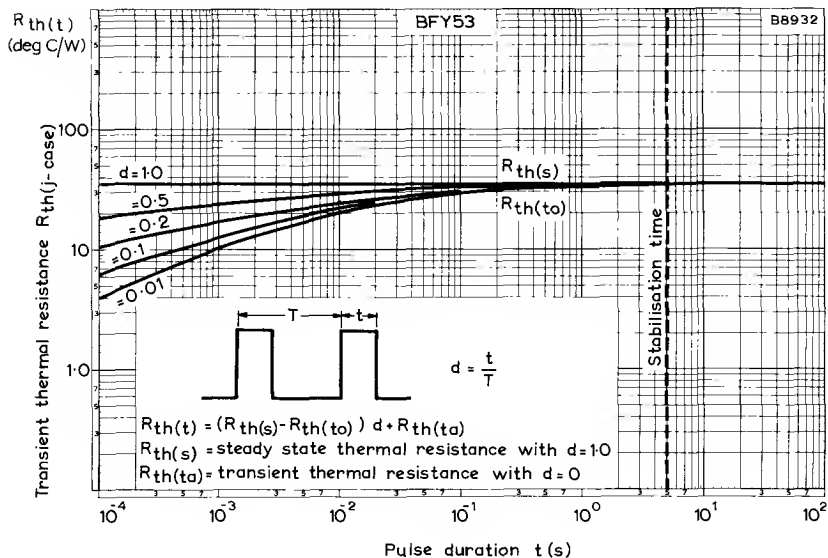
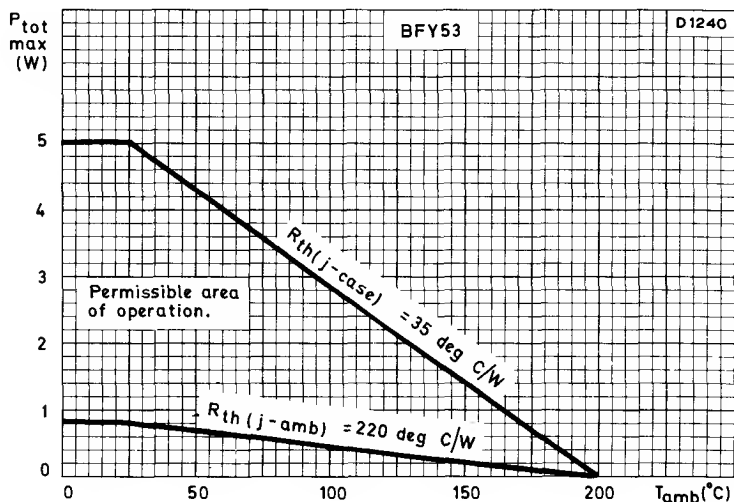
ELECTRICAL CHARACTERISTICS (contd.)

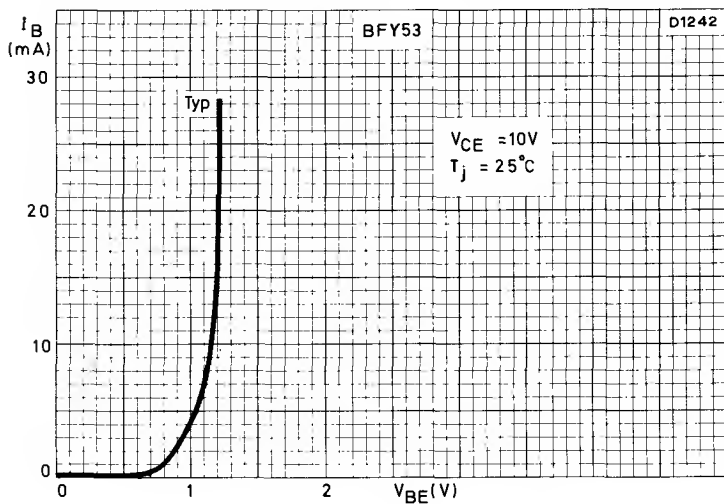
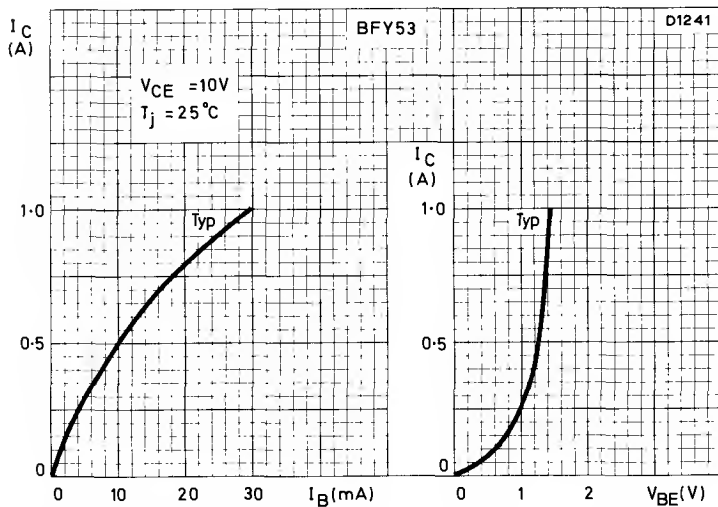
		Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio				
	$I_C = 10\text{mA}$, $V_{CE} = 10\text{V}$	20	55	-	
	$I_C = 150\text{mA}$, $V_{CE} = 10\text{V}$	30	75	-	
	$I_C = 500\text{mA}$, $V_{CE} = 10\text{V}$	18	50	-	
	$I_C = 1.0\text{A}$, $V_{CE} = 10\text{V}$	10	35	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10\text{mA}$, $I_B = 1.0\text{mA}$	-	0.06	0.15	V
	$I_C = 150\text{mA}$, $I_B = 15\text{mA}$	-	0.15	0.35	V
	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$	-	0.35	1.00	V
	$I_C = 1.0\text{A}$, $I_B = 100\text{mA}$	-	0.66	2.00	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10\text{mA}$, $I_B = 1.0\text{mA}$	-	0.69	1.2	V
	$I_C = 150\text{mA}$, $I_B = 15\text{mA}$	-	0.92	1.3	V
	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$	-	1.15	1.5	V
	$I_C = 1.0\text{A}$, $I_B = 100\text{mA}$	-	1.40	2.0	V
C_{Tc}	Collector capacitance				
	$V_{CB} = 10\text{V}$, $I_E = I_C = 0$, $f = 1.0\text{MHz}$	-	7.0	12	pF
f_T	Transition frequency				
	$I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 35\text{MHz}$, $T_{amb} = 25^\circ\text{C}$	50	140	-	MHz
h_{fe}	Small signal forward current transfer ratio				
	$I_C = 1.0\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 1.0\text{kHz}$, $T_{amb} = 25^\circ\text{C}$	10	70	-	

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SOLDERING AND WIRING RECOMMENDATIONS

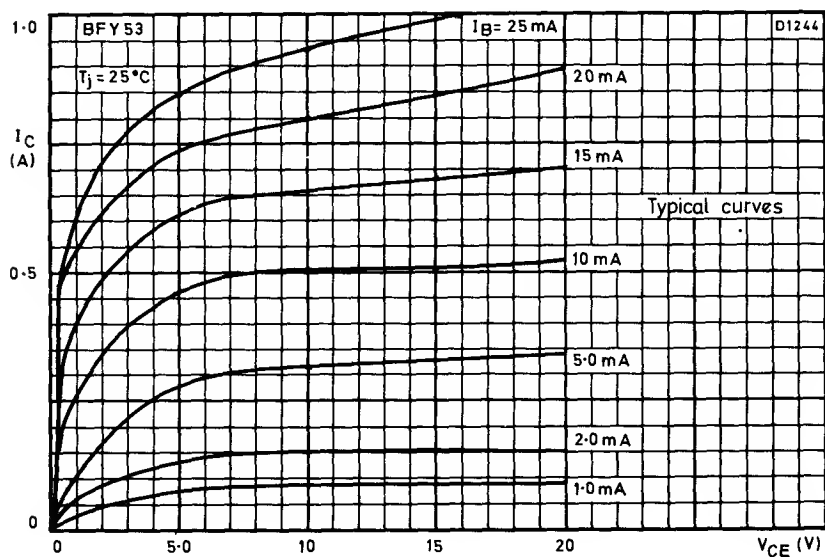
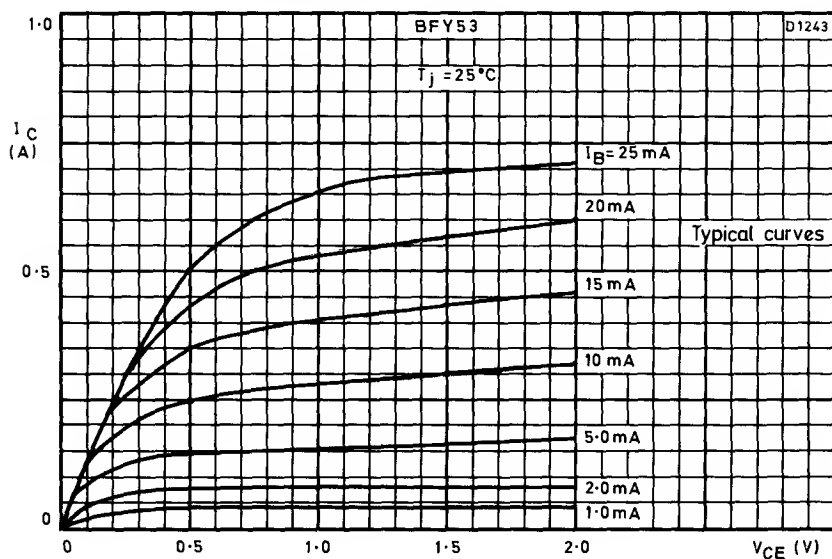
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.



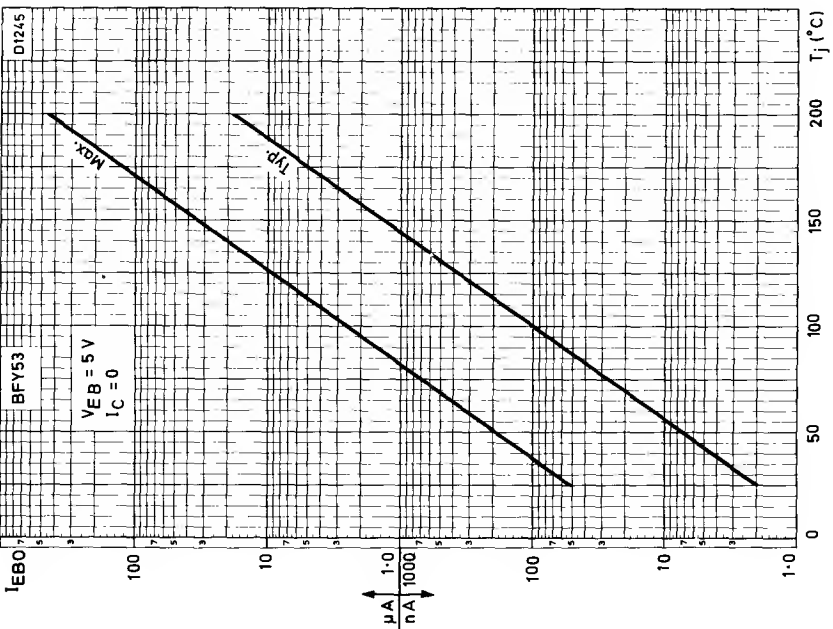
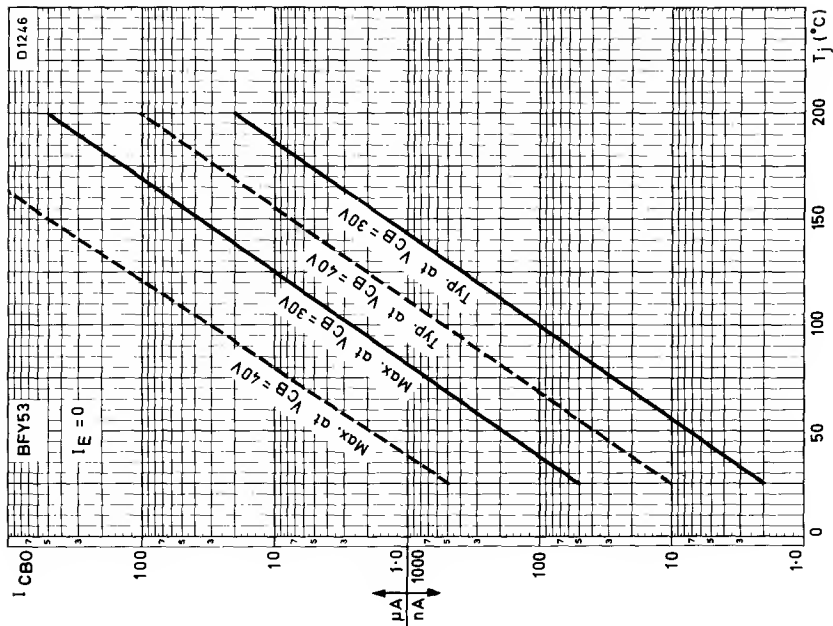


N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

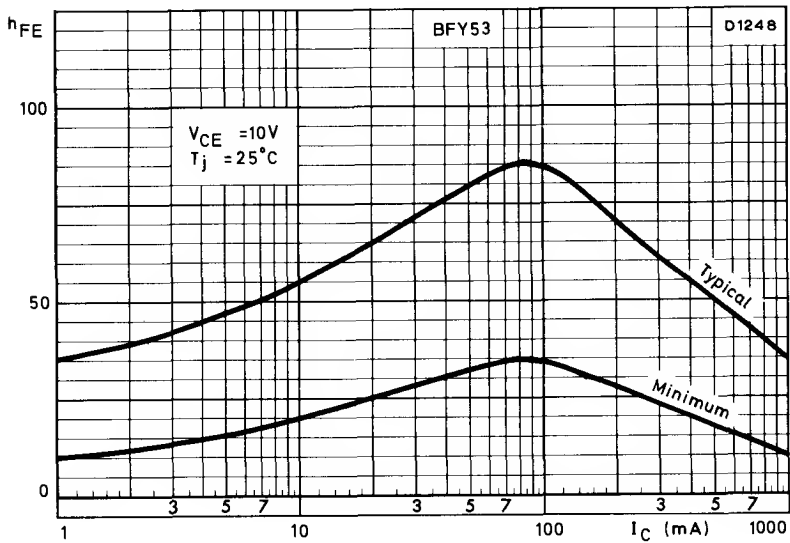
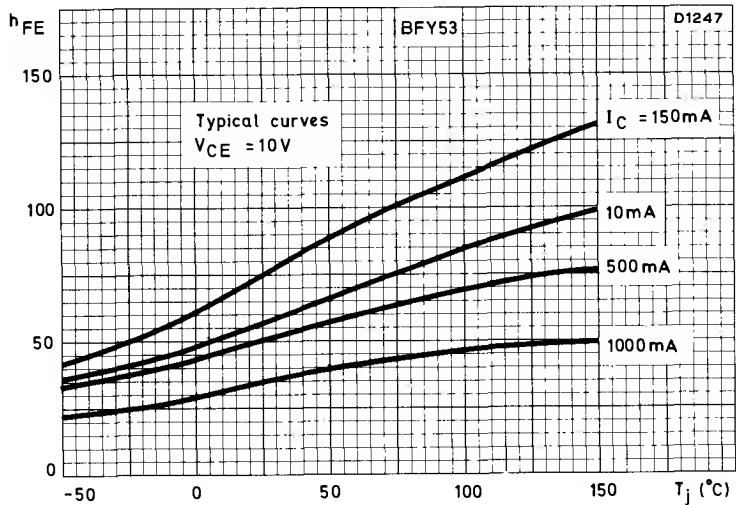
BFY53

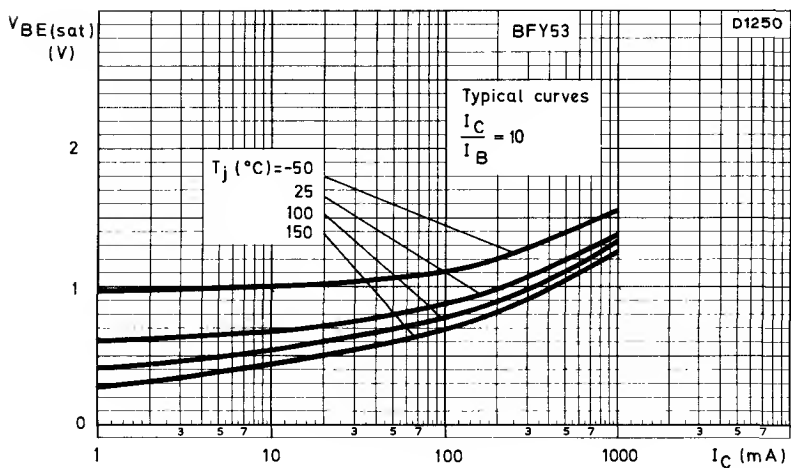
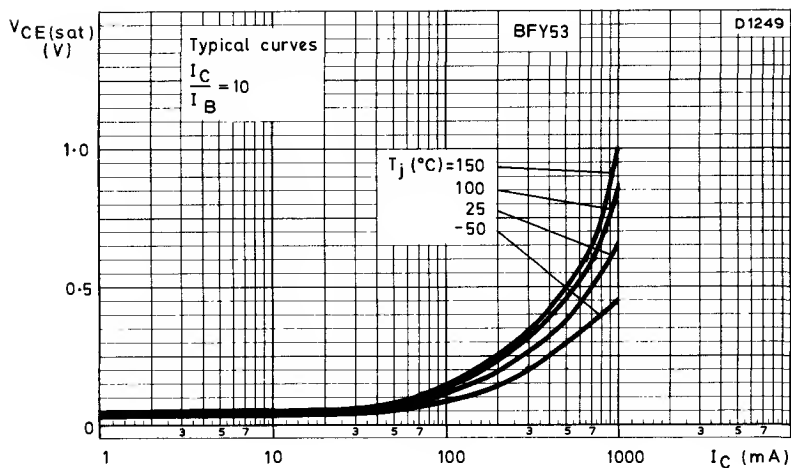


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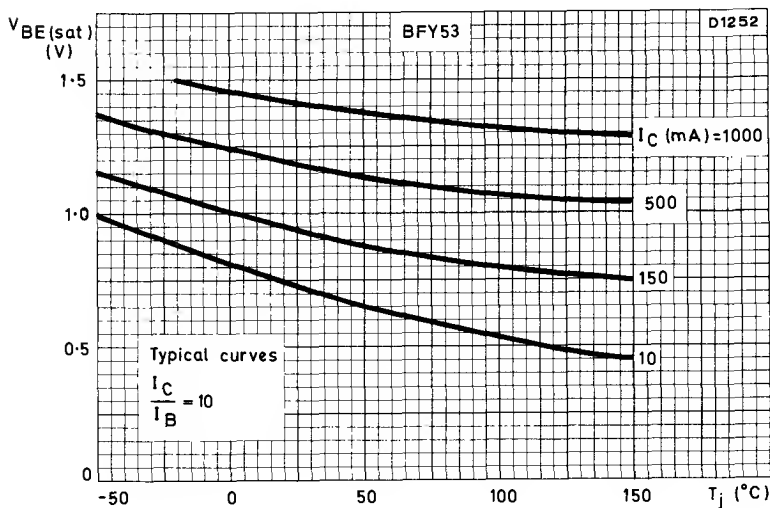
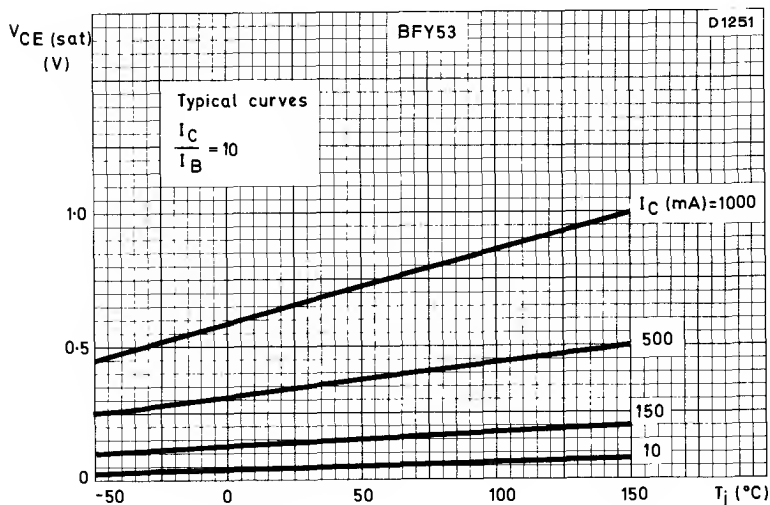
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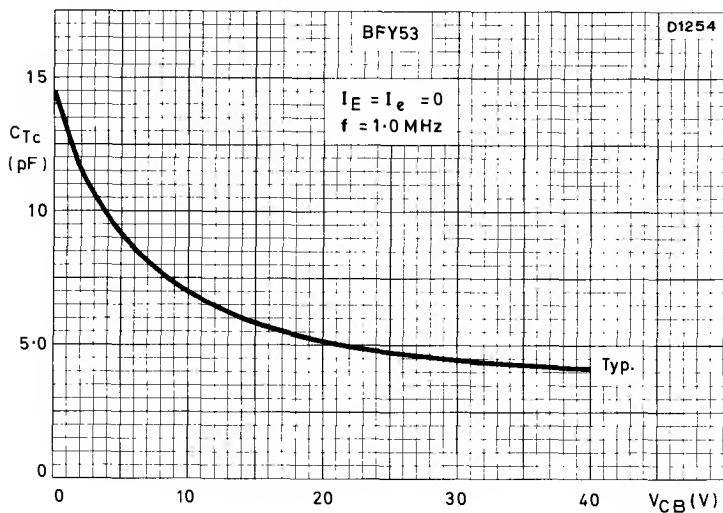
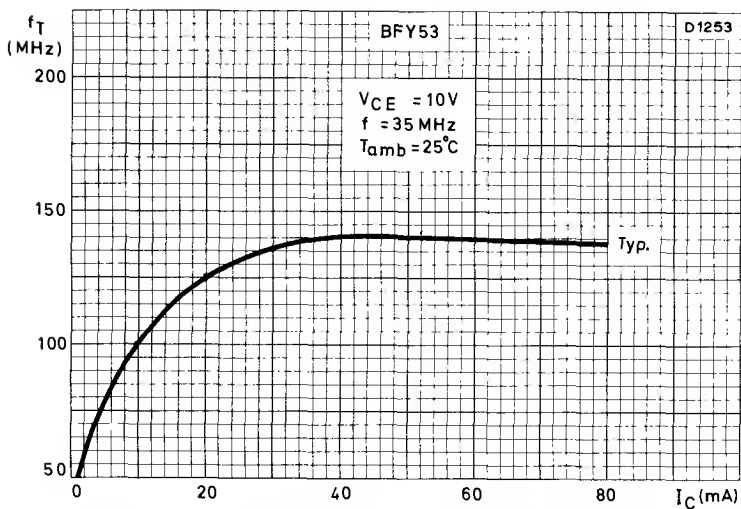


N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFY53



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SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BFY90

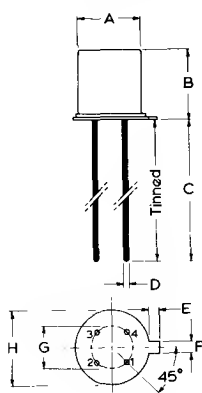
N-P-N silicon planar epitaxial transistor featuring low noise, low inter-modulation distortion and a high transition frequency. Intended for military and industrial applications.

QUICK REFERENCE DATA

V_{CBO} max.	30	V
V_{CEO} max.	15	V
I_{CM} max.	50	mA
P_{tot} max. ($T_{amb} = 25^{\circ}\text{C}$)	200	mW
T_j max.	200	$^{\circ}\text{C}$
f_T min. $I_C = 2.0\text{mA}$, $V_{CE} = 5.0\text{V}$	1.0	Gc/s
$I_C = 25\text{mA}$, $V_{CE} = 5.0\text{V}$	1.3	Gc/s
$-c_{re}$ max. $I_C = 2.0\text{mA}$, $f = 1.0\text{Mc/s}$	0.8	pF
Max. noise figure, $I_C = 2.0\text{mA}$, $f = 500\text{Mc/s}$	5.0	dB

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



Millimetres

	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.33
C	12.7	-	-
D	-	-	0.48
E	-	-	1.17
F	-	-	1.16
G	-	2.54	-
H	-	-	5.83

Viewed from underside

Connections: 1. Emitter 3. Collector
 2. Base 4. Shield connected to envelope

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max. ($I_E = 0$)	30	V
V_{CEO} max. ($I_B = 0, I_C = 10\text{mA}$)	15	V
V_{EBO} max. ($I_C = 0$)	2.5	V
I_{CM} max.	50	mA
$I_{C(AV)}$ max. (averaged over any 100 μs period)	25	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)	200	mW

Temperature

T_{stg} max.	200	$^\circ\text{C}$
T_{stg} min.	-65	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

θ_{j-amb} (in free air)	0.88	deg C/mW
θ_{j-case}	0.58	deg C/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

		Min.	Typ.	Max.	
	Collector cut-off current				
I_{CBO}	$V_{CB} = 15\text{V}, I_E = 0$	-	-	10*	nA
I_{CES}	$V_{CE} = 15\text{V}, V_{BE} = 0$	-	-	10	μA
I_B	Base current				
	$-I_E = 2.0\text{mA}, V_{CB} = 0$	13.2*	-	77*	μA
	$-I_E = 25\text{mA}, V_{CB} = 0$	200*	-	1200*	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 2.0\text{mA}, V_{CE} = 1.0\text{V}$	25	-	130	
	$I_C = 25\text{mA}, V_{CE} = 1.0\text{V}$	20	-	125	
f_T	Transition frequency†				
	$I_C = 2.0\text{mA}, V_{CE} = 5.0\text{V}$	1.0	-	-	Gc/s
	$I_C = 25\text{mA}, V_{CE} = 5.0\text{V}$	1.3	-	-	Gc/s
c_{tc}	Collector capacitance**				
	$V_{CB} = 10\text{V}, I_E = I_e = 0, f = 1.0\text{Mc/s}$	-	-	1.5	pF
c_{te}	Emitter capacitance				
	$V_{EB} = 0.5\text{V}, I_C = I_c = 0,$ $f = 1.0\text{Mc/s}$	-	-	2.0	pF

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BFY90

		Min.	Typ.	Max.	
$V_{CEO(sust)}$	Collector-emitter sustaining voltage				
	$I_C = 10\text{mA}, I_B = 0$	15	-	-	V
$-c_{re}$	Feedback capacitance				
	$I_C = 2.0\text{mA}, V_{CE} = 5.0\text{V},$ $f = 1.0\text{Mc/s}$	-	-	0.8	pF
$r_{bb'}c_{b'c}$	Feedback time constant†				
	$-I_E = 2.0\text{mA}, V_{CB} = 5.0\text{V},$ $f = 10.7\text{Mc/s}$	2.0	-	12	ps
NF	Noise figure‡, $I_C = 2.0\text{mA},$ $V_{CE} = 5.0\text{V}$				
	$f = 100\text{kc/s}$, optimum R_s	-	-	4.0	dB
	$f = 200\text{Mc/s}$, optimum Z_s	-	-	3.5	dB
	$f = 500\text{Mc/s}, R_s = 50\Omega$	-	-	5.0	dB
d_{lm}	Intermodulation distortion (See fig. 1)				
	$I_C = 14\text{mA}, V_{CE} = 6.0\text{V},$ $f = 217\text{Mc/s}$				
	$V_o = 100\text{mV}, R_L = 37.5\Omega$ $f_1 = 183\text{Mc/s}, f_2 = 200\text{Mc/s}$	-	-53	-	dB
P_o	Output power‡ (See fig. 2)				
	$I_C = 22.5\text{mA}, V_{CE} = 13.5\text{V},$ $P_i = 25\text{mW}$				
	$f = 500\text{Mc/s}, T_{case} = 25^\circ\text{C}$	175	-	-	mW

*These are the characteristics which are recommended for acceptance testing purposes.

†Shield lead grounded.

**Shield lead not connected

‡Care must be taken to reduce steady state current when no h.f. signal is applied.

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$$I_C = 2.0\text{mA}, V_{CE} = 5.0\text{V}, f = 500\text{Mc/s}$$

G_{UM} Max. unilateralised power gain

$$10 \log \frac{|y_{fe}|^2}{4g_{ie}g_{oe}}$$

$$I_C = 2.0\text{mA}, V_{CE} = 5.0\text{V},$$

$$f = 500\text{Mc/s}$$

Min.	Typ.	Max.
-	16	- mmho
-	3.75	- pF
-	1.55	- mmho
-	258	- deg
-	45	- mmho
-	285	- deg
-	0.19	- mmho
-	1.9	- pF
-	22	- dB

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SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BFY90

CIRCUIT FOR MEASUREMENT OF THE OUTPUT POWER

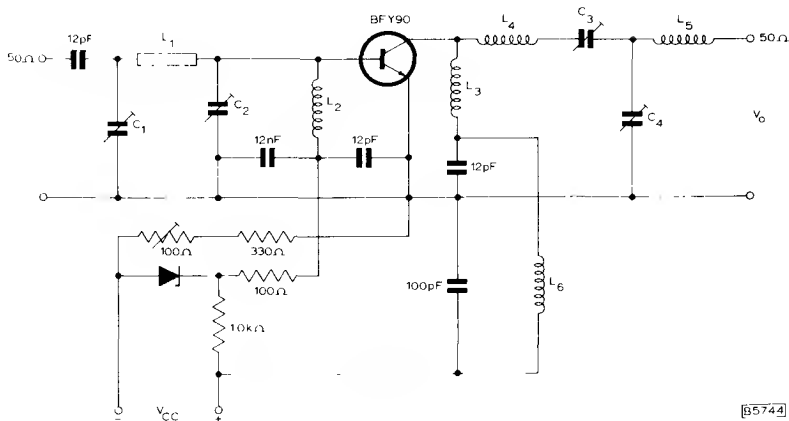


Fig. 2.

C_1 = 16 pF air-gap trimmer

C_2, C_3, C_4 = 6 pF ceramic trimmer

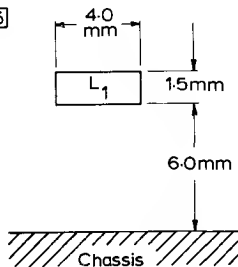
L_1 = copper strip $20 \times 4 \times 1.5$ mm

L_2, L_6 = 10 turns of 0.7 mm en. copper wire, dia = 4 mm

L_3 = 1 turn of 1 mm copper wire, dia = 8 mm

L_4, L_5 = 1 turn of 1 mm copper wire dia = 7 mm

B5745



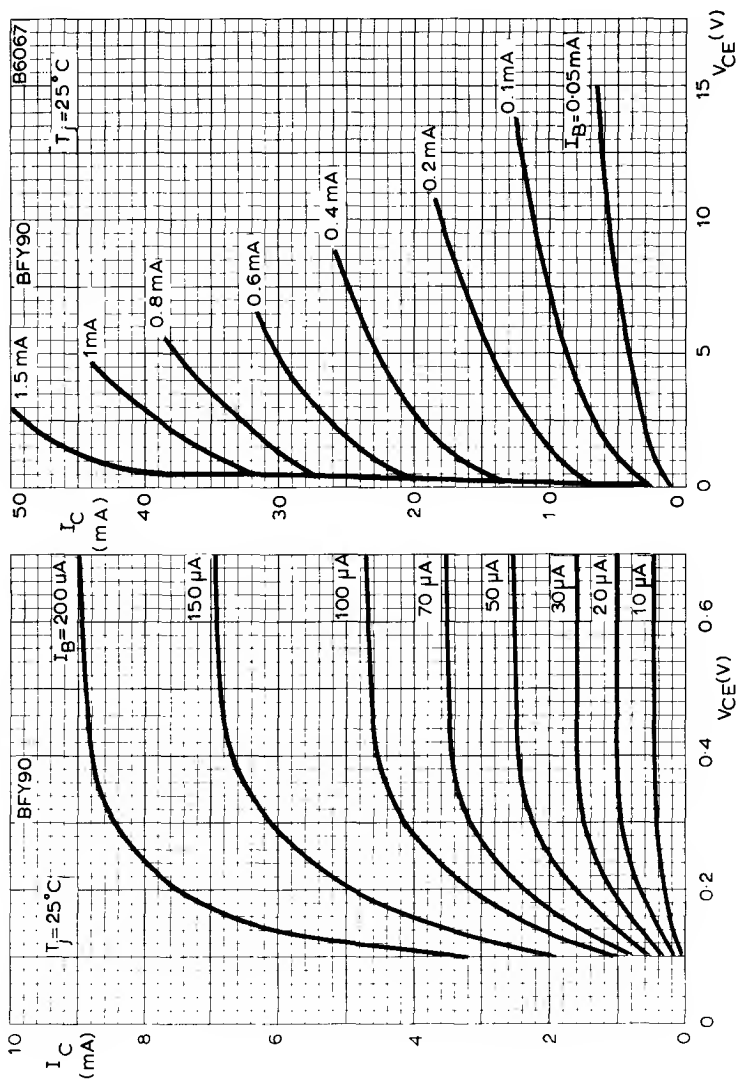
Mullard

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

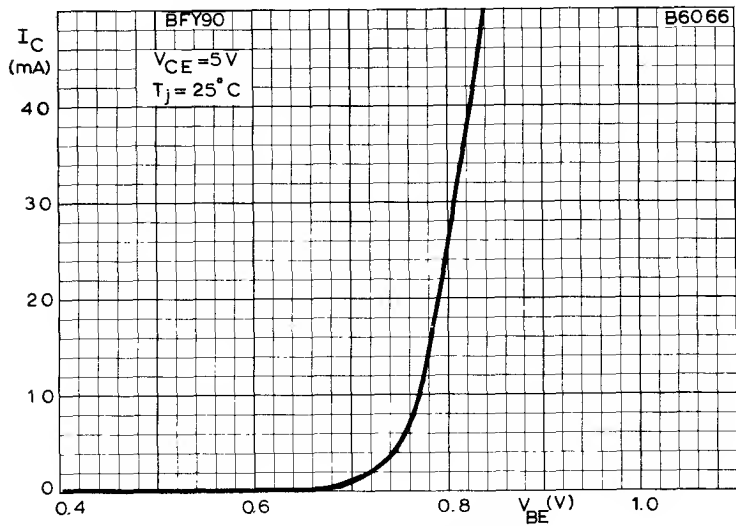
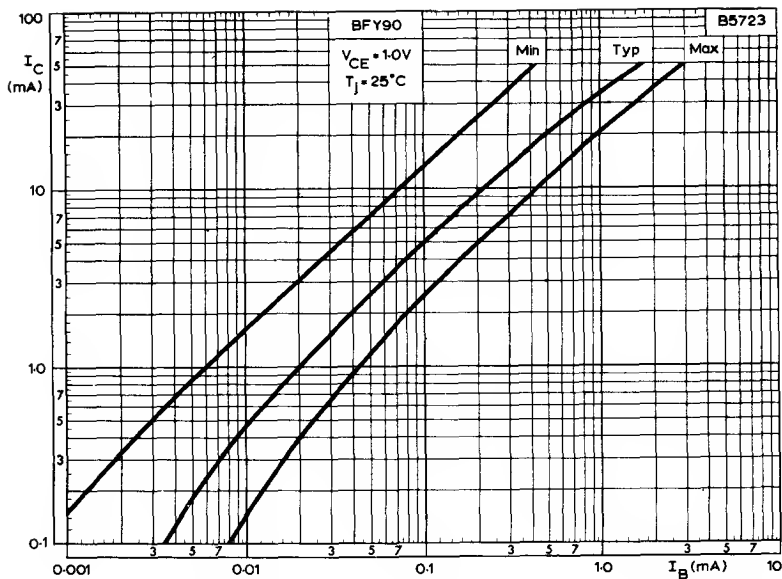
SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BFY90

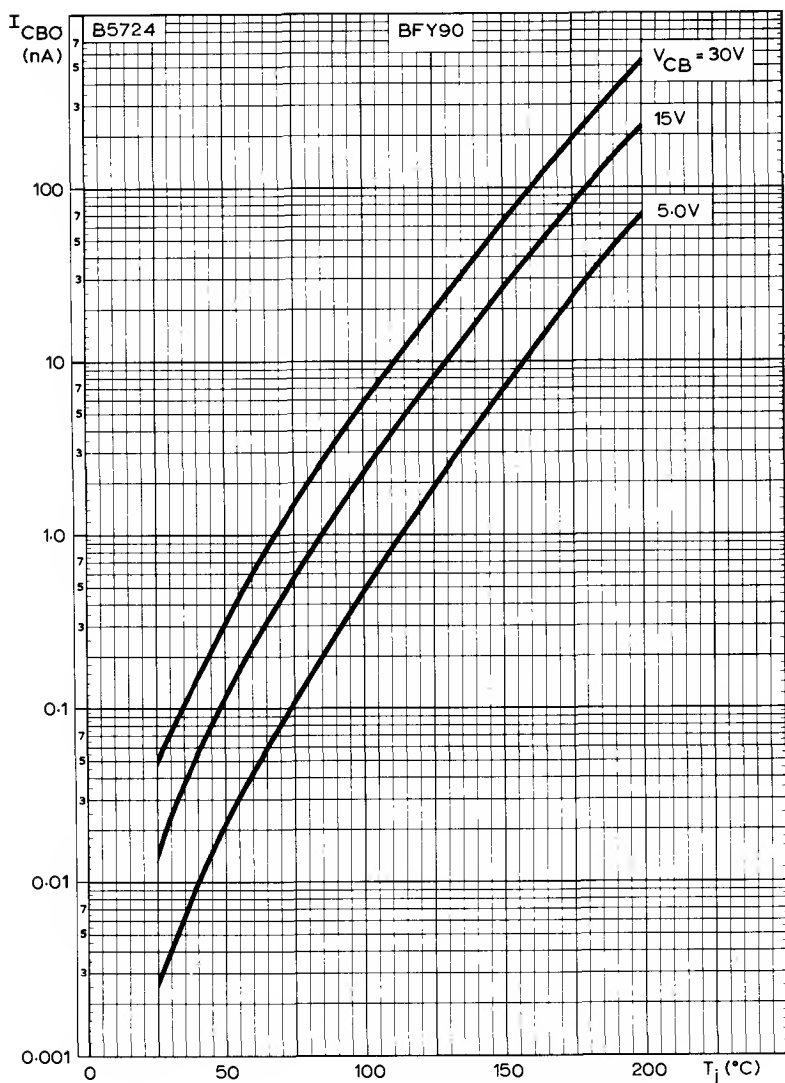


TYPICAL OUTPUT CHARACTERISTICS

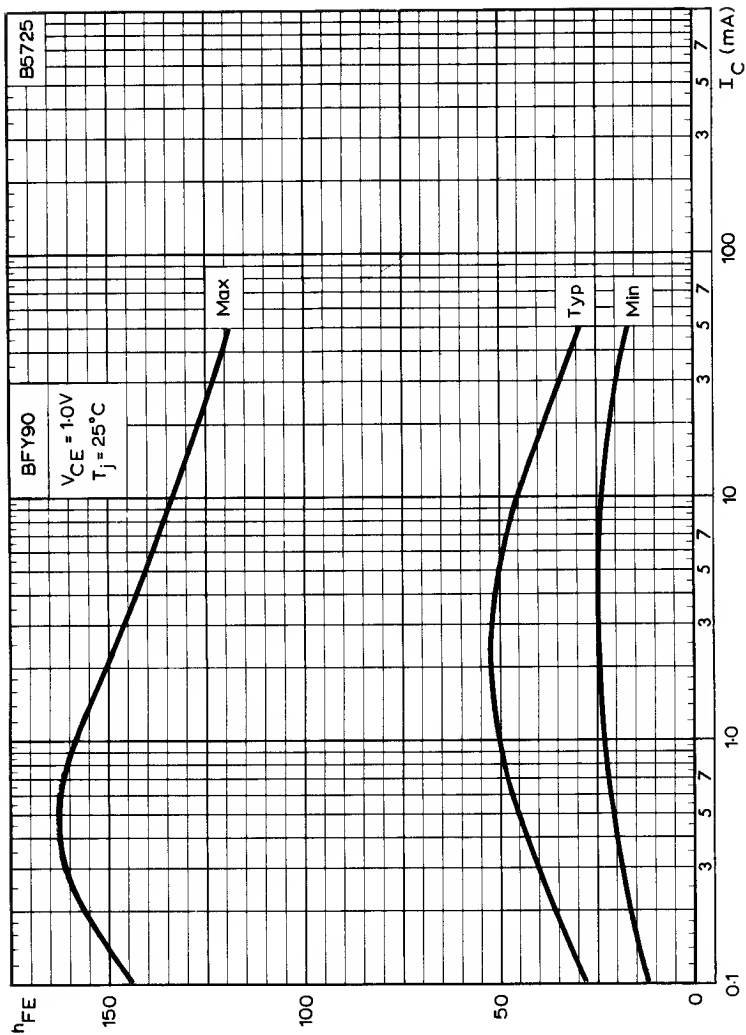
Mullard



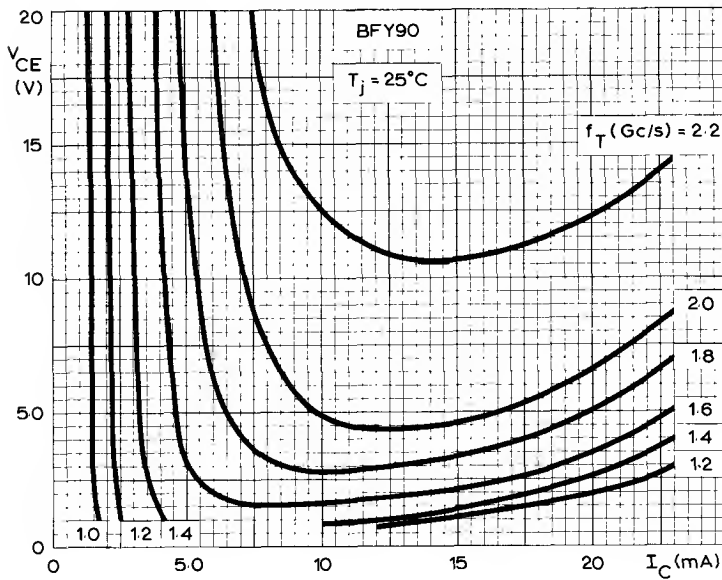
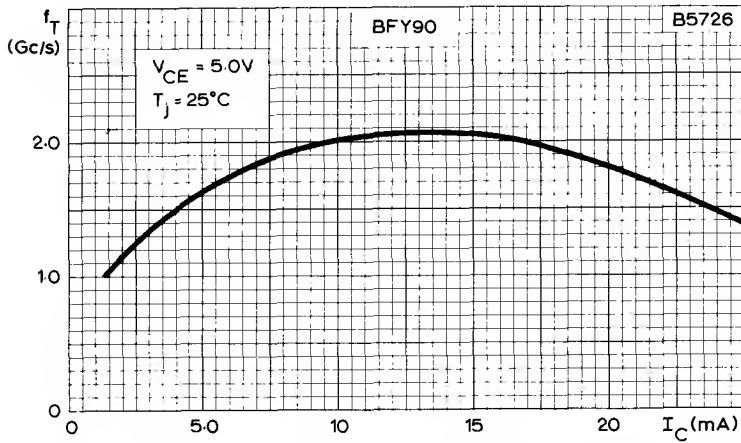
TRANSFER CHARACTERISTICS
TYPICAL INPUT CHARACTERISTIC



TYPICAL VARIATION OF COLLECTOR CUT-OFF CURRENT
WITH JUNCTION TEMPERATURE

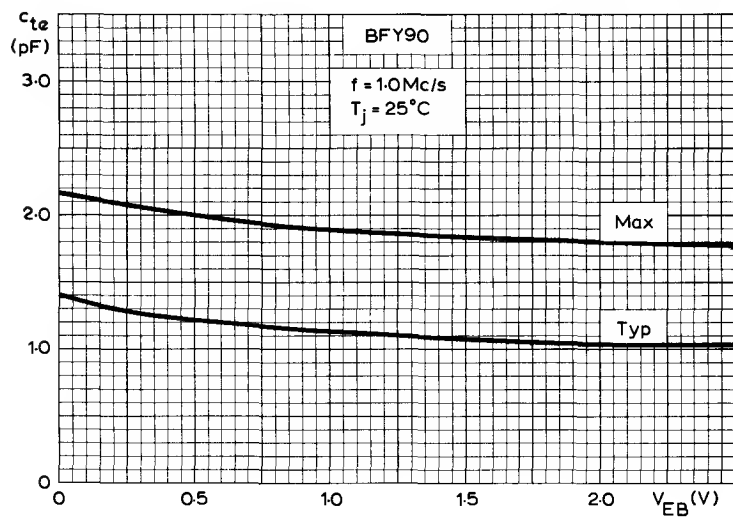
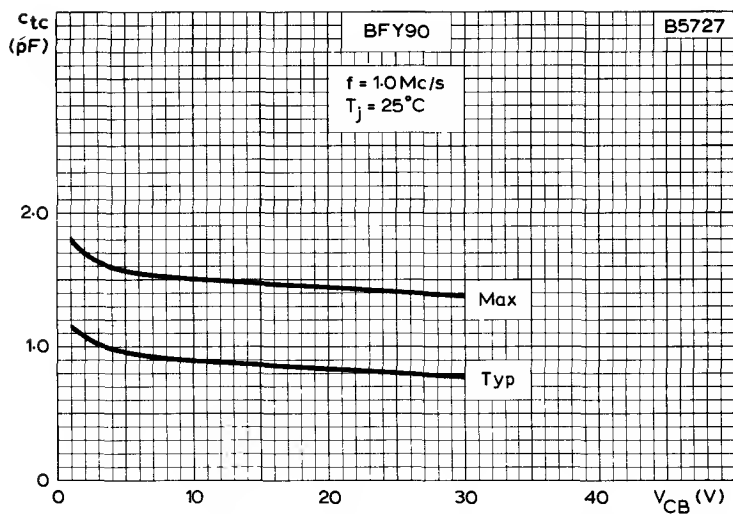


STATIC FORWARD CURRENT TRANSFER RATIO
PLOTTED AGAINST COLLECTOR CURRENT



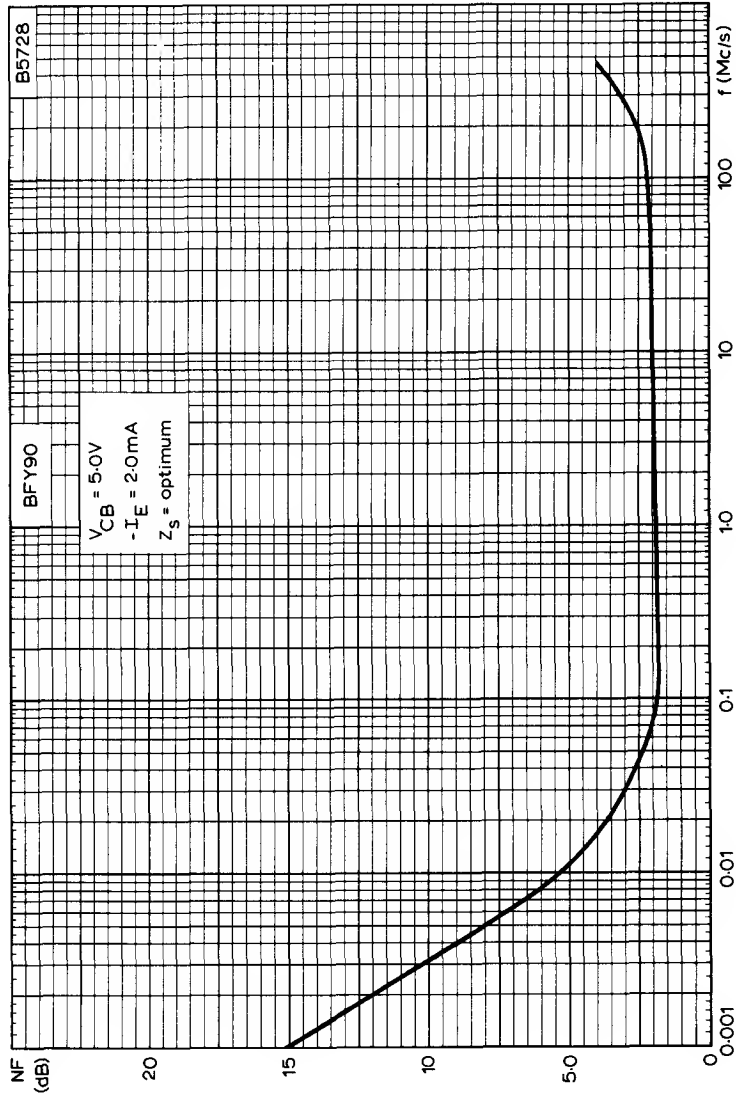
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST
COLLECTOR CURRENT

CONTOURS OF CONSTANT TRANSITION FREQUENCY

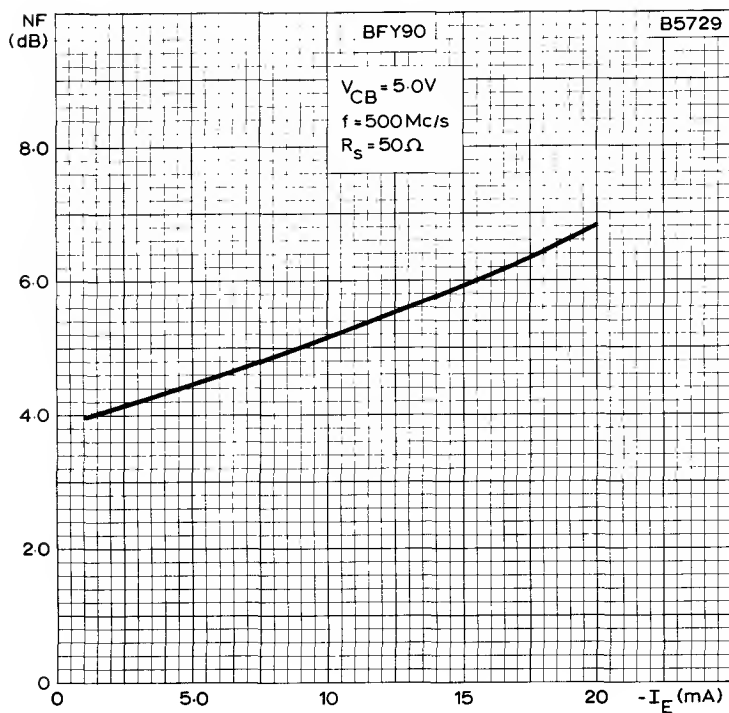


COLLECTOR CAPACITANCE PLOTTED AGAINST
COLLECTOR-BASE VOLTAGE

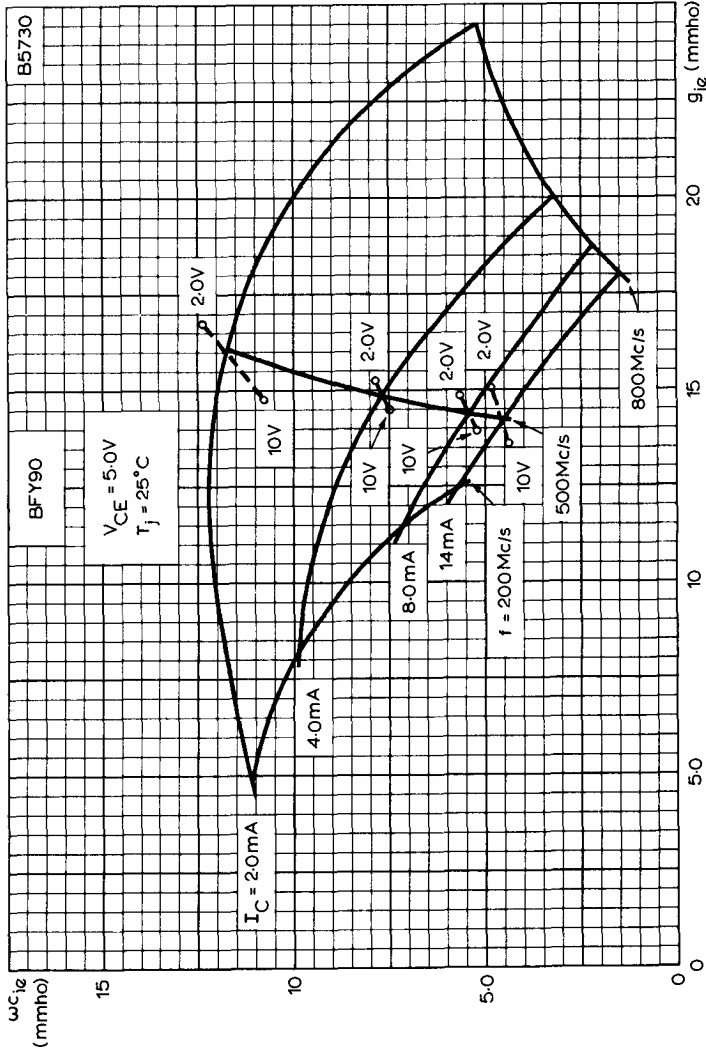
EMITTER CAPACITANCE PLOTTED AGAINST
EMITTER-BASE VOLTAGE



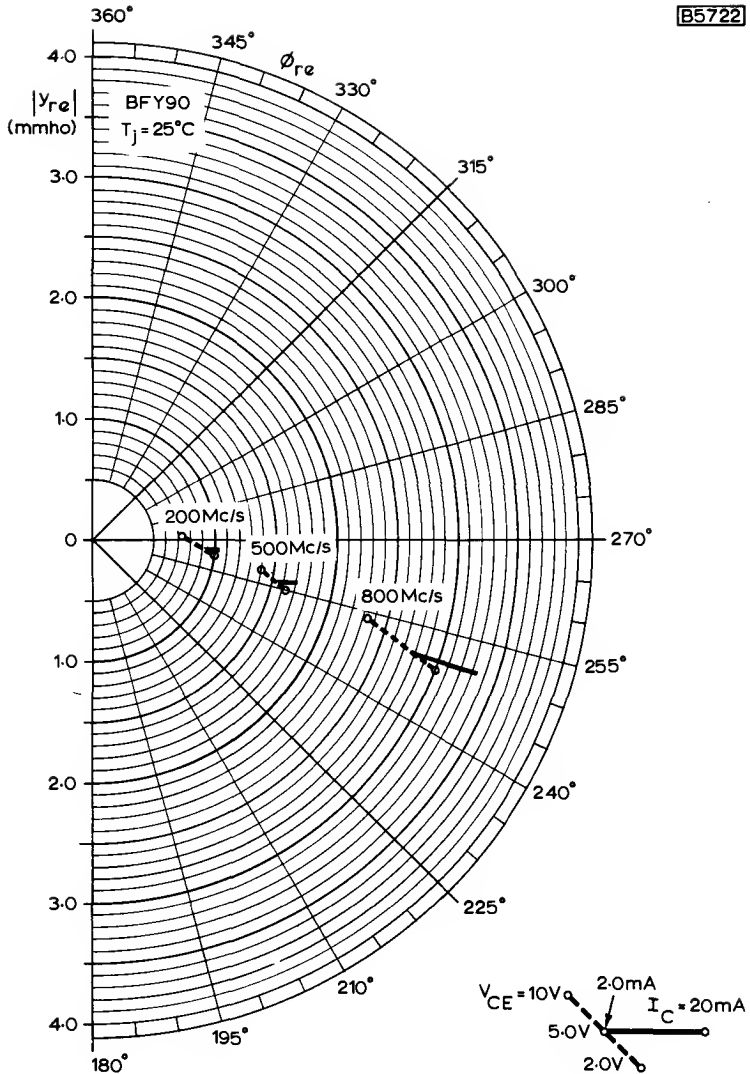
TYPICAL NOISE FIGURE PLOTTED AGAINST FREQUENCY



TYPICAL NOISE FIGURE PLOTTED AGAINST EMITTER CURRENT



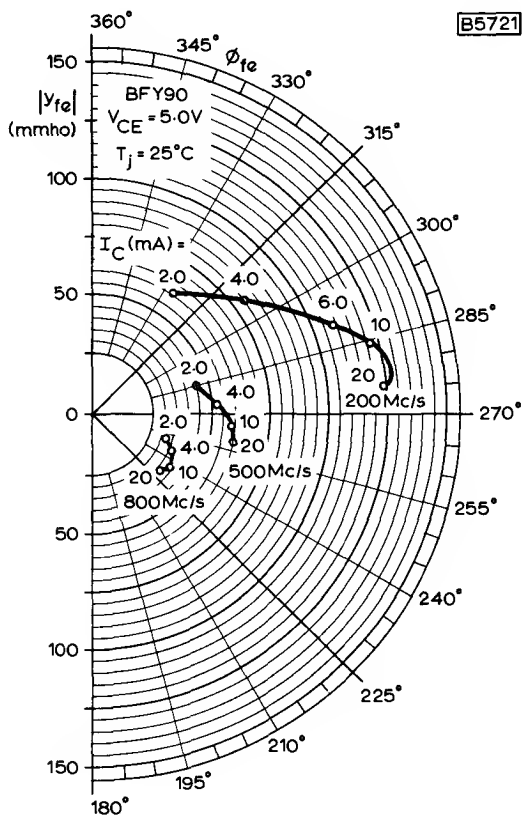
TYPICAL INPUT ADMITTANCE PLOTTED AGAINST
COLLECTOR CURRENT AND FREQUENCY



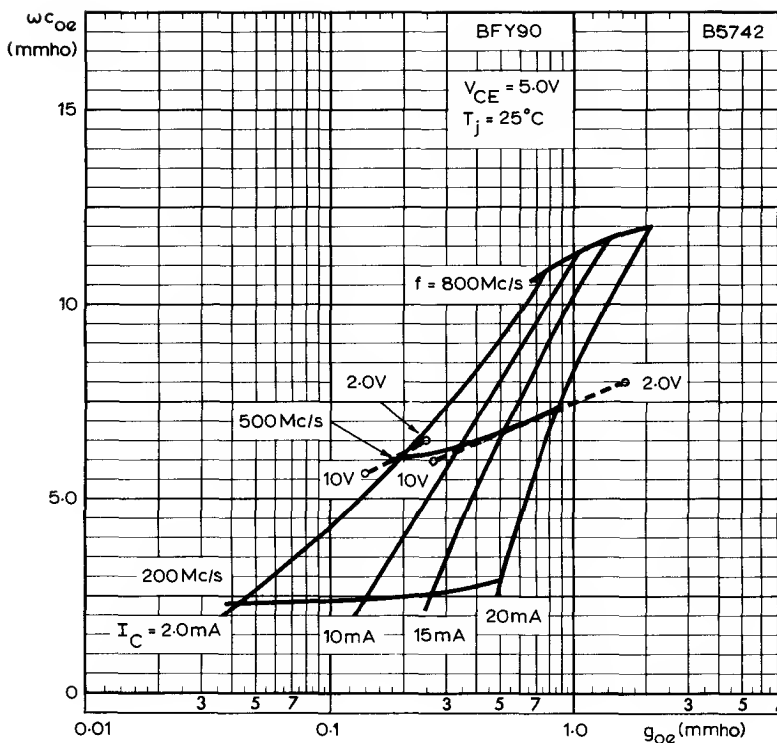
TYPICAL FEEDBACK ADMITTANCE PLOTTED AGAINST
COLLECTOR CURRENT AND FREQUENCY

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BFY90



TYPICAL FORWARD TRANSFER ADMITTANCE PLOTTED AGAINST
COLLECTOR CURRENT AND FREQUENCY



TYPICAL OUTPUT ADMITTANCE PLOTTED AGAINST
COLLECTOR CURRENT AND FREQUENCY

U.H.F. POWER AMPLIFIER MODULES

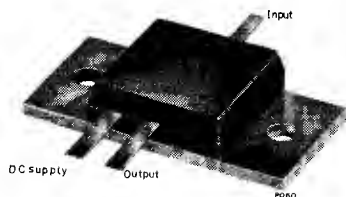
BGY22 BGY22A

TENTATIVE DATA

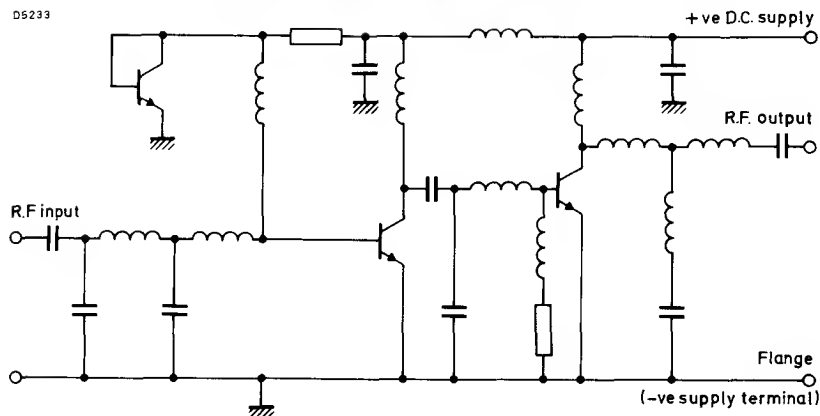
Broadband u.h.f. amplifier modules primarily designed for mobile applications operating directly from 12V vehicle electrical systems. The modules will produce 2.5W output into a 50Ω load over the bands 380-512MHz (BGY22), and 420-480MHz (BGY22A).

QUICK REFERENCE DATA							
Type	Mode	Freq. range (MHz)	V _{CC} (V)	P _D (mW)	P _L (W)	η (%)	Matched input and output Z (Ω)
BGY22	f. m.	380-512	13.5	50	2.5 min.	40 min.	50
BGY22	f. m.	380-512	13.5	50	2.9 typ.	50 typ.	50
BGY22A	f. m.	420-480	12.5	50	2.5 min.	40 min.	50

Mechanical details
on page 10.



D5233



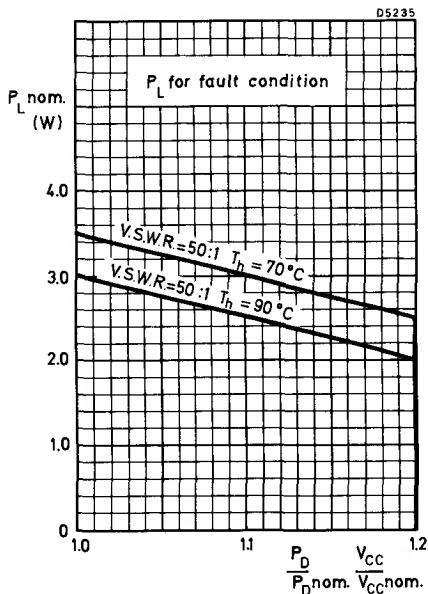
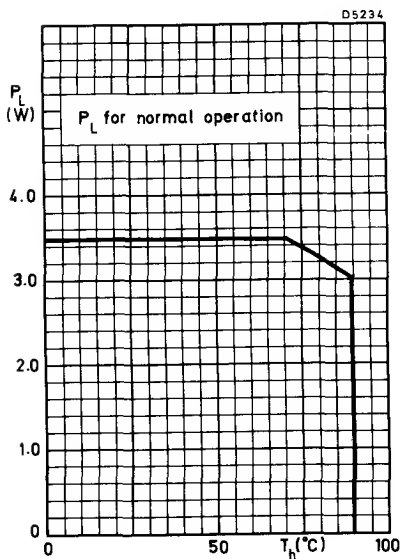
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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CC} max.	D.C. voltage - supply terminal to flange	18	V
V_{in} max.	D.C. voltage - input terminal to flange	± 25	V
V_{out} max.	D.C. voltage - output terminal to flange	± 25	V
I_{in} max.	D.C. supply terminal current	800	mA
P_D max.	$V_{CC} = 13.5V, Z_L = 50\Omega$	150	mW



Where $P_{L nom} = P_L$ at $V_{CC} = 13.5V, Z_L = 50\Omega$ (BGY22),
 and $P_{L nom} = P_L$ at $V_{CC} = 12.5V, Z_L = 50\Omega$ (BGY22A).

OPERATING CHARACTERISTICS (At $T_h = 25^{\circ}\text{C}$ unless otherwise stated)

Reference planes at RF input and output terminals are 1mm from the plastic encapsulation.

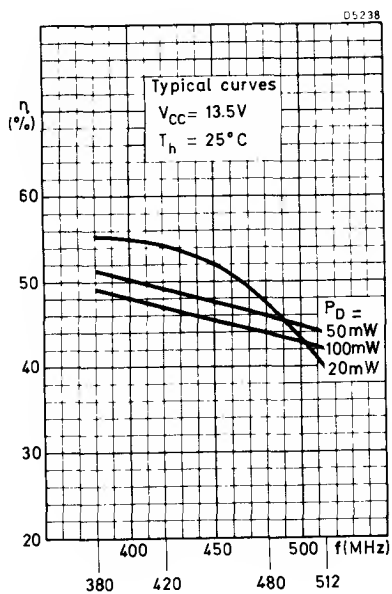
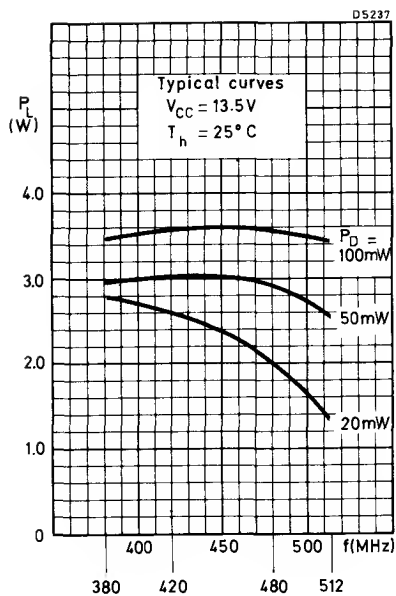
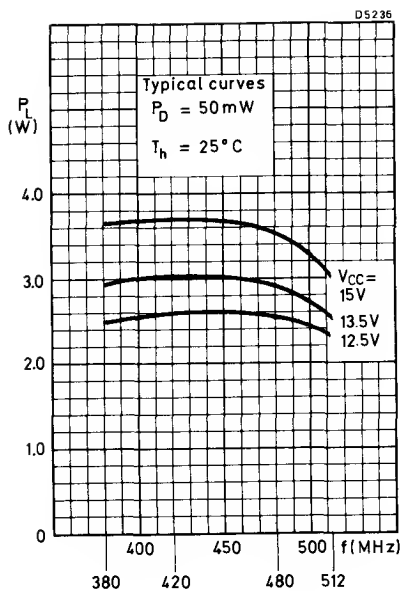
Frequency range 380 - 512MHz, $V_{CC} = 13.5\text{V}$ (BGY22)

Frequency range 420 - 480MHz, $V_{CC} = 12.5\text{V}$ (BGY22A)

		Min.	Typ.	Max.
I_Q	Quiescent current			
	$P_D = 0$	4.0	-	12 mA
P_L	Load power			
	$P_D = 50\text{mW}$	2.5	-	3.5 W
η	Efficiency			
	$P_D = 50\text{mW}$	40	-	%
I_{in}	Module current			
	$P_D = 50\text{mW}$	-	475	- mA
	Harmonic content			
	$P_D = 50\text{mW}$	Any harmonic is at least 20dB down relative to carrier		
	Input V.S.W.R. with respect to 50Ω			
	$P_D = 50\text{mW}$	-	-	2:1
	Temperature coefficient of P_L			
	$P_D = 50\text{mW}$, $T_h = 25$ to 70°C	-	-10	- mW/ $^{\circ}\text{C}$
	Stability			
	$V_{CC} = 10.5$ to 15V , $P_D = 10\text{mW}$ to 100mW			
	$T_h = -40$ to $+90^{\circ}\text{C}$			
	Output load V.S.W.R. $\leq 3:1$, all phases		No instabilities	
	Output load V.S.W.R. $\leq 10:1$, all phases		No appreciable instabilities	

THERMAL CHARACTERISTICS

T_{stg} range	-40 to +100	$^{\circ}\text{C}$
T_h range	-40 to +90	$^{\circ}\text{C}$



APPLICATION INFORMATION

R.F. performance in c.w. operation, $T_h = 25^{\circ}\text{C}$.

Drive source and Load Impedance = 50Ω .

Type	Freq. range (MHz)	V_{CC} (V)	P_D (mW)	P_L (W)	η (%)
BGY22	380-512	15	50	3.5 typ.	47 typ.
BGY22	380-512	13.5	50	2.5 min.	40 min.
BGY22	380-512	13.5	50	2.9 typ.	47 typ.
BGY22	380-512	12.5	50	2.5 typ.	47 typ.
BGY22A	420-480	12.5	50	2.5 min.	40 min.

The modules are designed to withstand full load mismatch under the following conditions.

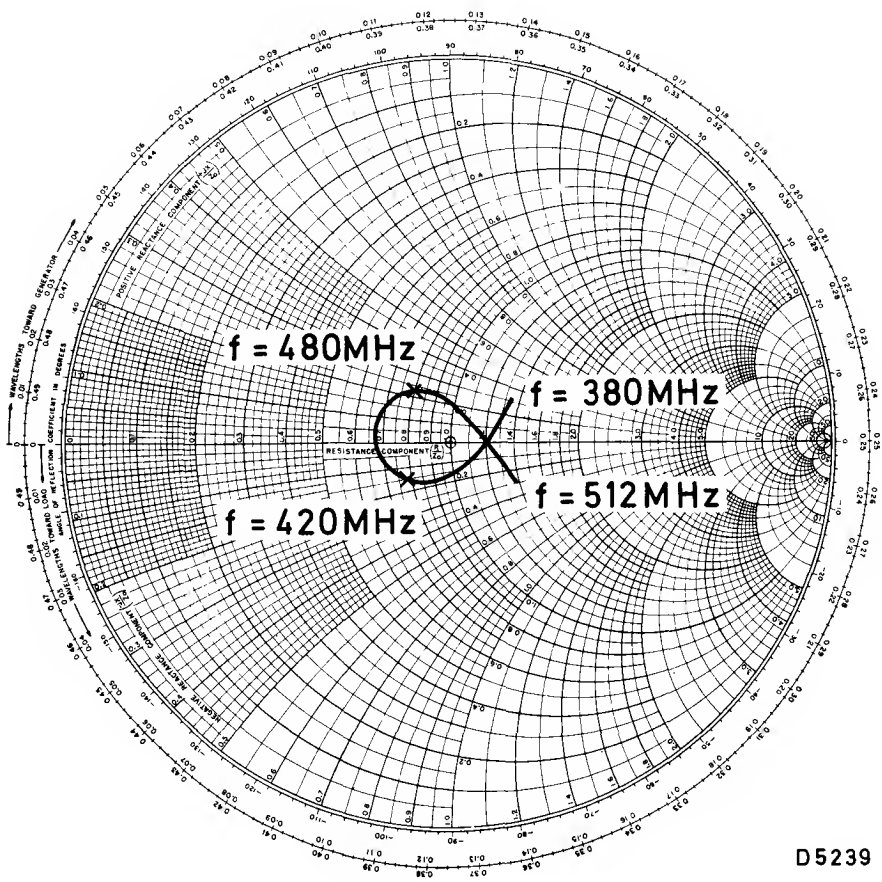
$$P_D = P_{D \text{ nom}} + 20\%, T_h = 70^{\circ}\text{C},$$

$$V_{CC} = 16.5\text{V (BGY22)}$$

$$V_{CC} = 15.0\text{V (BGY22A)}$$

$$\text{V.S.W.R.} = 50:1 \text{ at any phase}$$

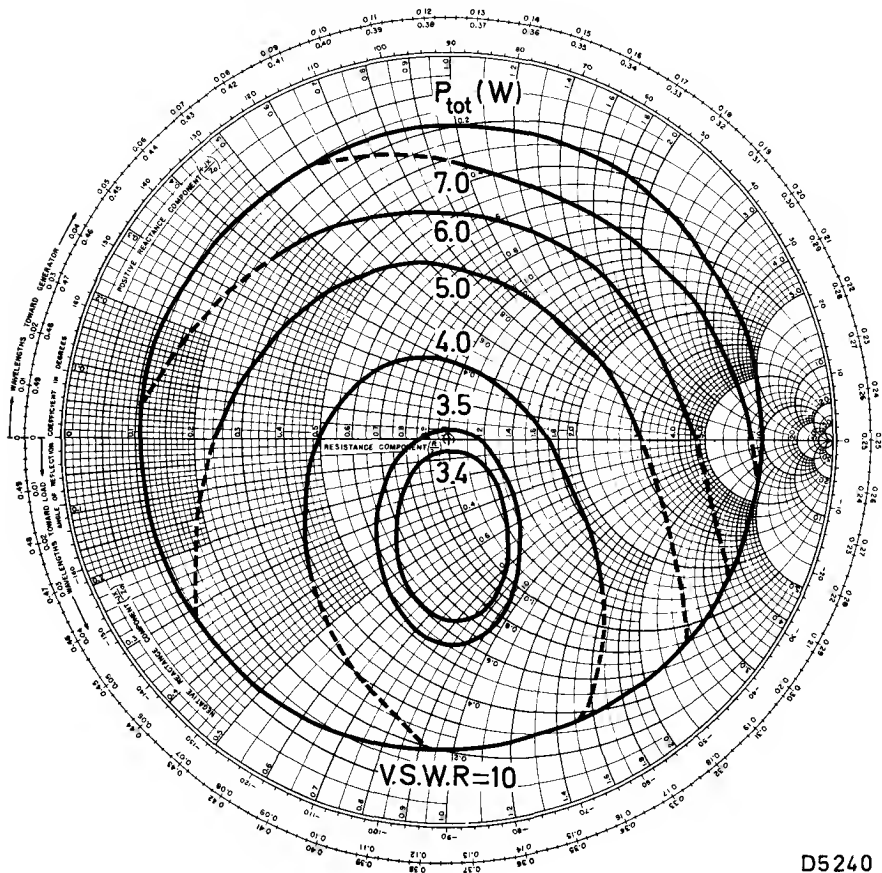
where $P_{D \text{ nom}} = P_D$ for 2.5W module output under nominal conditions.



D5239

TYPICAL VARIATION OF INPUT IMPEDANCE WITH FREQUENCY

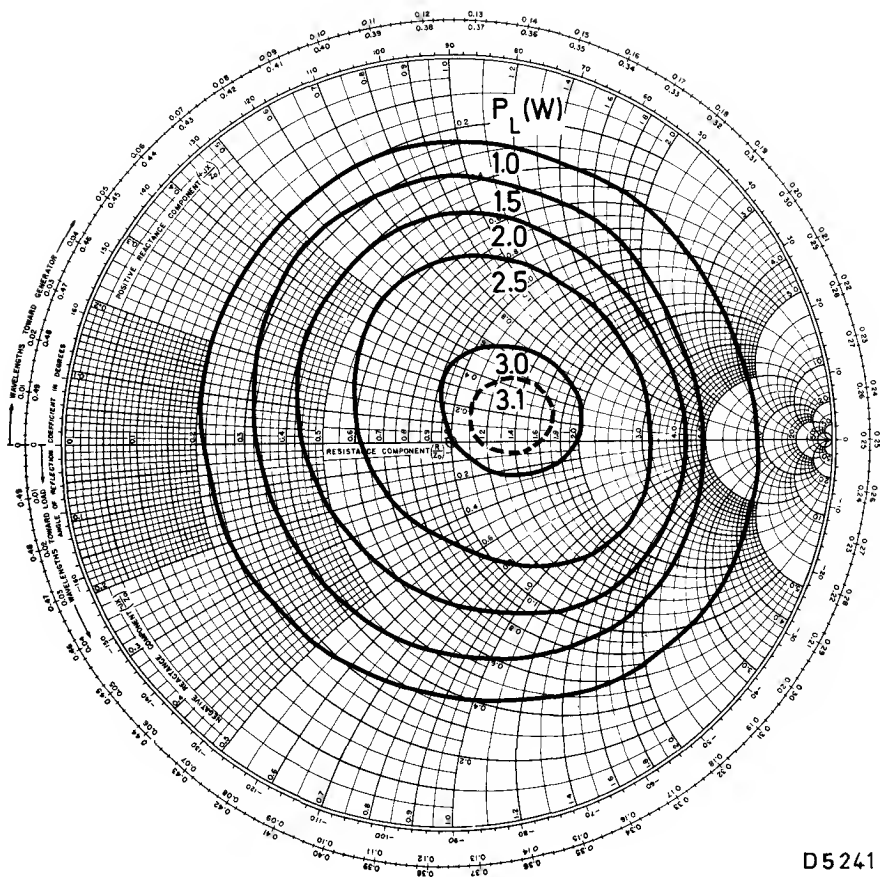
APPLICATION INFORMATION (Cont'd)



TYPICAL VARIATION OF POWER DISSIPATION WITH LOAD IMPEDANCE

$$f = 470\text{MHz}$$

$$V_{CC} = 13.5\text{V}$$



D5241

TYPICAL VARIATION OF LOAD POWER WITH LOAD IMPEDANCE

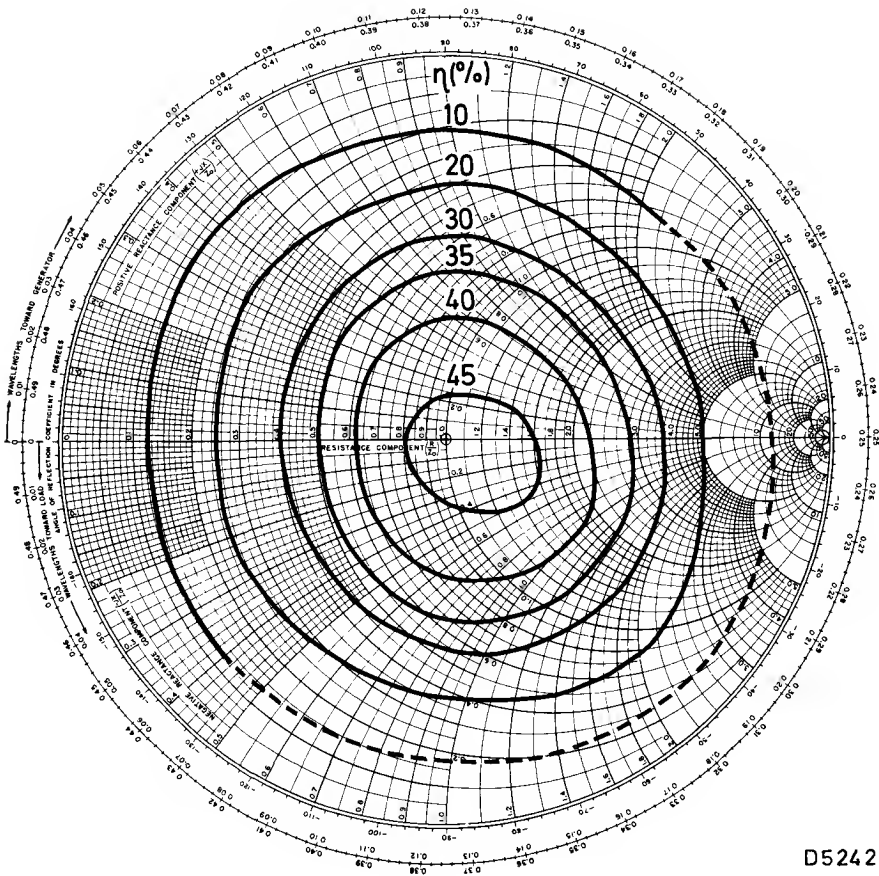
$$P_D = 50\text{mW}$$

$$f = 470\text{MHz}$$

$$V_{CC} = 13.5\text{V}$$

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APPLICATION INFORMATION (Cont'd)



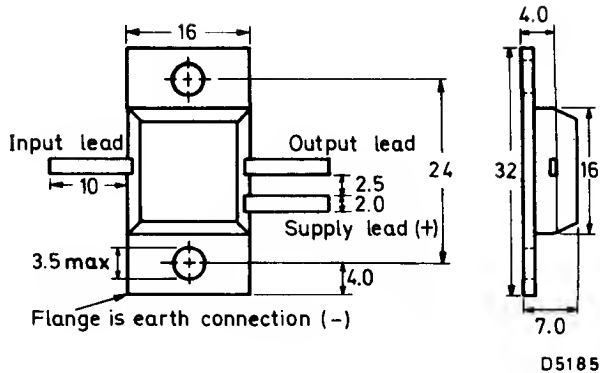
TYPICAL VARIATION OF EFFICIENCY WITH LOAD IMPEDANCE

$P_D = 50\text{mW}$

$f = 470\text{MHz}$

$V_{CC} = 13.5\text{V}$

OUTLINE AND DIMENSIONS



All dimensions in millimetres

MOUNTING

To ensure good thermal contact between mounting base and heatsink, burrs or thickening at the edges of the heatsink holes should be removed and the package bolted down onto a flat surface.

Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for 10 seconds at least 1mm from the plastic.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

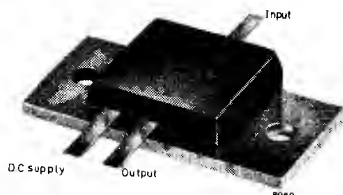
THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR

Mullard

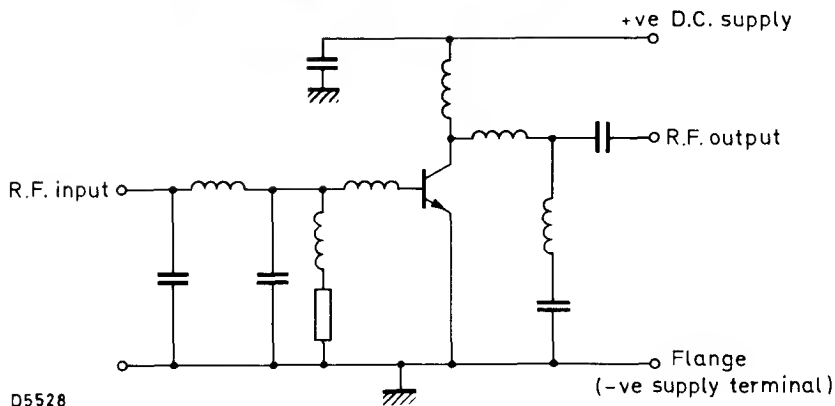
TENTATIVE DATA

Broadband u.h.f. amplifier modules primarily designed for mobile applications operating directly from 12V vehicle systems. The modules are suitable for driving directly from the BGY22 and BGY22A respectively, and when so driven will produce 7W output into a 50Ω load over the band 380-480MHz (BGY23), and 7W over the band 420-480MHz (BGY23A).

QUICK REFERENCE DATA							
Type	Mode	Freq. range (MHz)	V _{CC} (V)	P _D (W)	P _L (W)	η (%)	Matched input and output Z (Ω)
BGY23	f. m.	380-480	13.5	2.5	7.0 min.	60 min.	50
BGY23	f. m.	380-480	13.5	2.5	8.3 typ.	71 typ.	50
BGY23	f. m.	480-512	13.5	2.5	7.5 typ.	69 typ.	50
BGY23A	f. m.	420-480	12.5	2.5	7.0 min.	60 min.	50



Mechanical details
on page 10

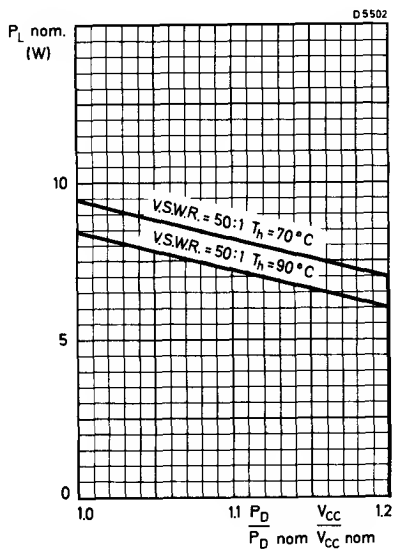
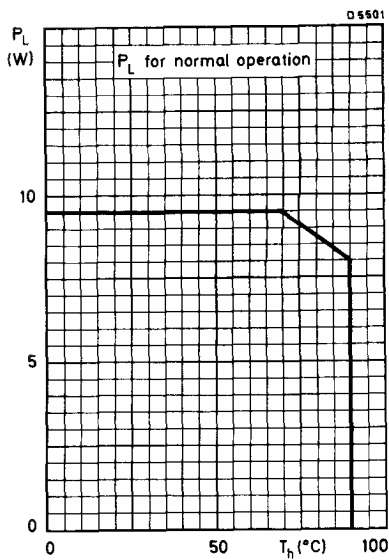


RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CC} max.	D.C. voltage - supply terminal to flange	18	V
$*V_{in}$ max.	D.C. voltage - input terminal to flange	± 0.5	V
V_{out} max.	D.C. voltage - output terminal to flange	± 25	V
I_{in} max.	D.C. supply terminal current	1.7	A
P_D max.	$V_{CC} = 13.5V, Z_L = 50\Omega$	3.5	W



Where $P_L \text{ nom.} = P_L$ at $V_{CC} = 13.5V, Z_L = 50\Omega$ (BGY23)

and $P_L \text{ nom.} = P_L$ at $V_{CC} = 12.5V, Z_L = 50\Omega$ (BGY23A)

*No external D.C. connection should be made to this terminal.

U.H.F. POWER AMPLIFIER MODULES

BGY23 BGY23A

OPERATING CHARACTERISTICS (At $T_h = 25^\circ$ unless otherwise stated.)

Reference planes at RF input and output terminals are 1mm from the plastic encapsulation.

Frequency range 380 - 512 MHz, $V_{CC} = 13.5V$ (BGY23)

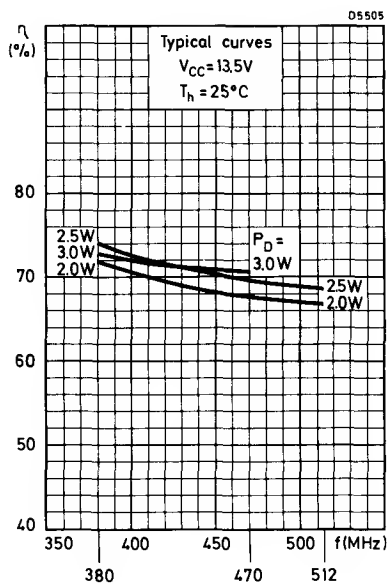
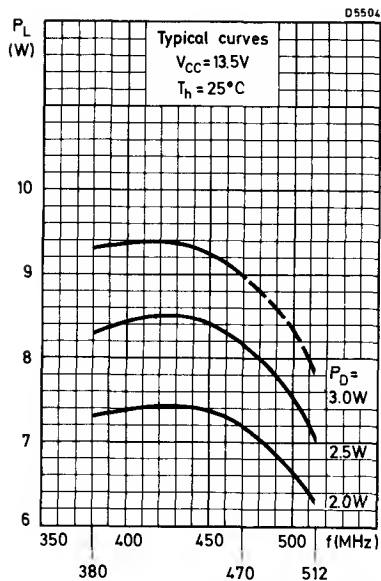
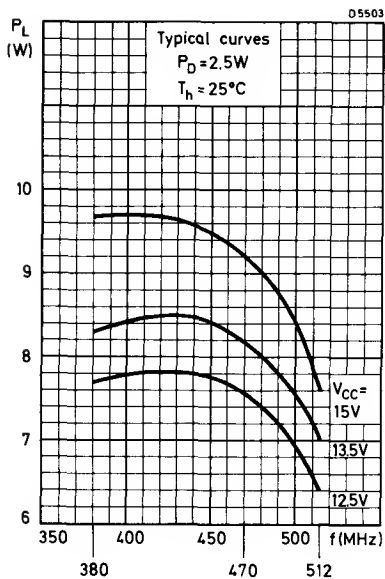
Frequency range 420 - 480 MHz, $V_{CC} = 12.5V$ (BGY23A)

			Min.	Typ.	Max.	
I_Q	Quiescent Current $P_D = 0$		-	-	5.0	mA
P_L	Load Power $P_D = 2.5W$, $f = 380-480MHz$	BGY 23	7.0	-	9.5	W
	$P_D = 2.5W$, $f = 480-512MHz$	BGY 23	-	7.5	-	W
	$P_D = 2.5W$, $f = 420-480MHz$	BGY 23A	7.0	-	9.5	W
η	Efficiency $P_D = 2.5W$		60	-	-	%
I_{in}	Module Current $P_D = 2.5W$		-	900	-	mA
	Harmonic Content $P_D = 2.5W$					Any harmonic is at least 20dB down relative to carrier.
	Input V.S.W.R. with respect to 50Ω $P_D = 2.5W$		-	-	2: 1	
	Temperature coefficient of P_L $P_D = 2.5W$, $T_h = 25^\circ C$ to $70^\circ C$		-	-20	-	mW/ $^\circ C$
Stability						
	$V_{CC} = 10.5$ to $15V$, $P_D = 1.0$ to $3.5W$					
	$T_h = -40$ to $+90^\circ C$					
	Output load V.S.W.R. $\leq 3: 1$, all phases					No instabilities
	Output load V.S.W.R. $\leq 10: 1$, all phases					No appreciable instabilities

THERMAL CHARACTERISTICS

T_{stg} range	-40 to +100	$^\circ C$
T_h range	-40 to +90	$^\circ C$

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APPLICATION INFORMATION

R. F. performance in c. w. operation, $T_h = 25^{\circ}\text{C}$

Drive Source and Load Impedance = 50Ω

Type	freq. range (MHz)	V_{CC} (V)	P_D (W)	P_L (W)	η (%)
BGY23	380-512	15.0	2.5	9.0 typ.	65 typ.
BGY23	380-480	13.5	2.5	7.0 min.	60 min.
BGY23	380-480	13.5	2.5	8.3 typ.	71 typ.
BGY23	480-512	13.5	2.5	7.5 typ.	69 typ.
BGY23	380-512	12.5	2.5	7.4 typ.	70 typ.
BGY23A	420-480	12.5	2.5	7.0 min.	60 min.

Connection to the BGY22/BGY22A respectively can be either by 50Ω transmission line or directly with a total lead length not greater than 2mm.

The module is designed to withstand full load mis-match under the following conditions:

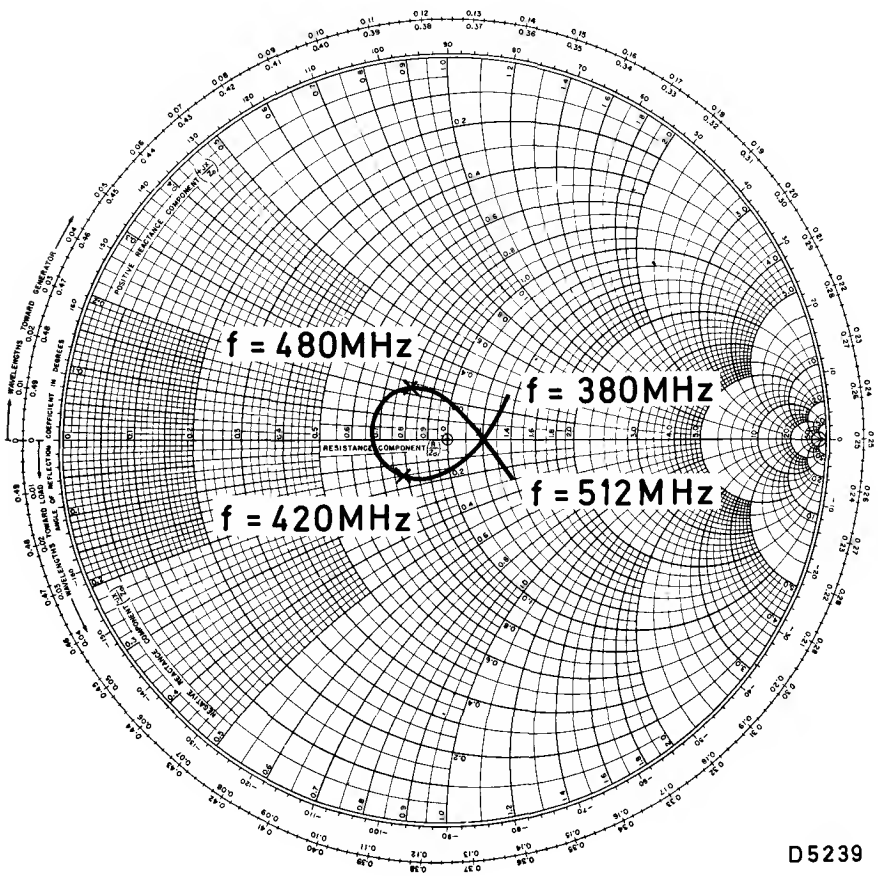
$$P_D = P_{D \text{ nom}} + 20\%, T_h = 70^{\circ}\text{C}$$

$$V_{CC} = 16.5\text{V (BGY23)}$$

$$V_{CC} = 15.0\text{V (BGY23A)}$$

$$V.S.W.R. = 50:1 \text{ at any phase.}$$

where $P_{D \text{ nom}} = P_D$ for 7.0W module output under nominal conditions.



TYPICAL VARIATION OF INPUT IMPEDANCE WITH FREQUENCY

BGY23
BGY23A

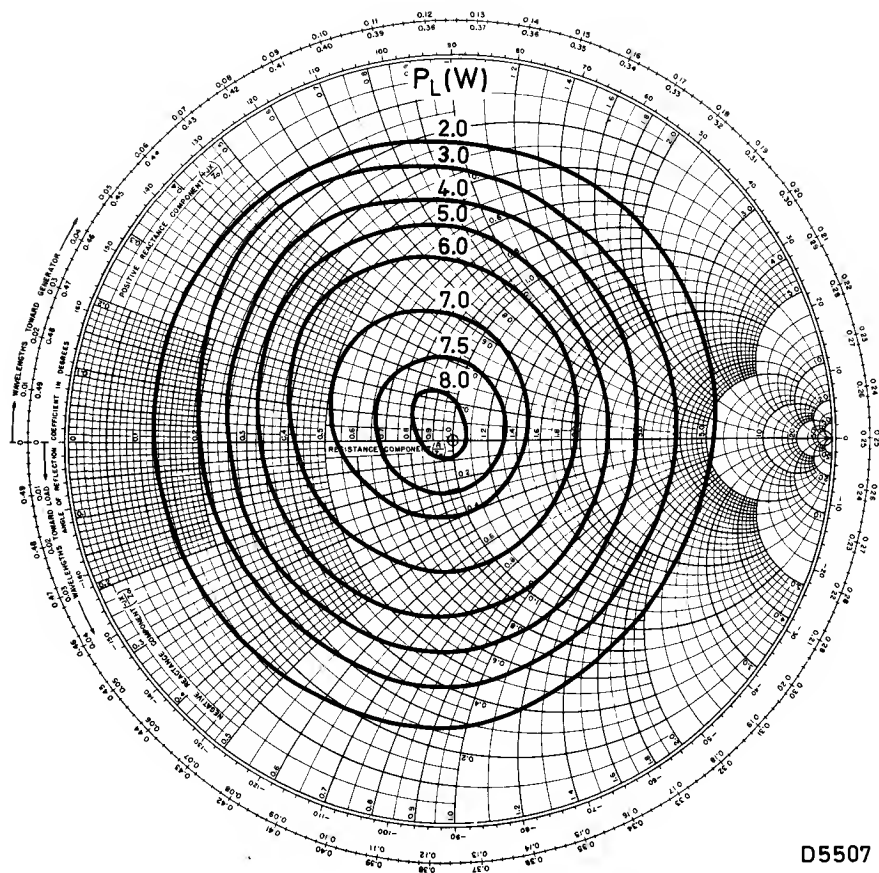
The chart is a Smith Chart with the following features:

- Outer Scale:** SWR (Standing Wave Ratio) from 1.0 to infinity.
- Inner Scale:** Reflection Coefficient (V) from 0.0 to 1.0.
- Radial Line:** A line from the center (1.0) through the point 1.0 on the outer scale to the point 10 on the inner scale.
- Constant SWR Circle:** A circle labeled 10, centered at the center of the chart.
- Other Scales:** Scales for SWR, reflection coefficient, and transmission loss are also present.

TYPICAL VARIATION OF OVERALL POWER DISSIPATION WITH LOAD IMPEDANCE

$$V_{CC} = 13.5V$$

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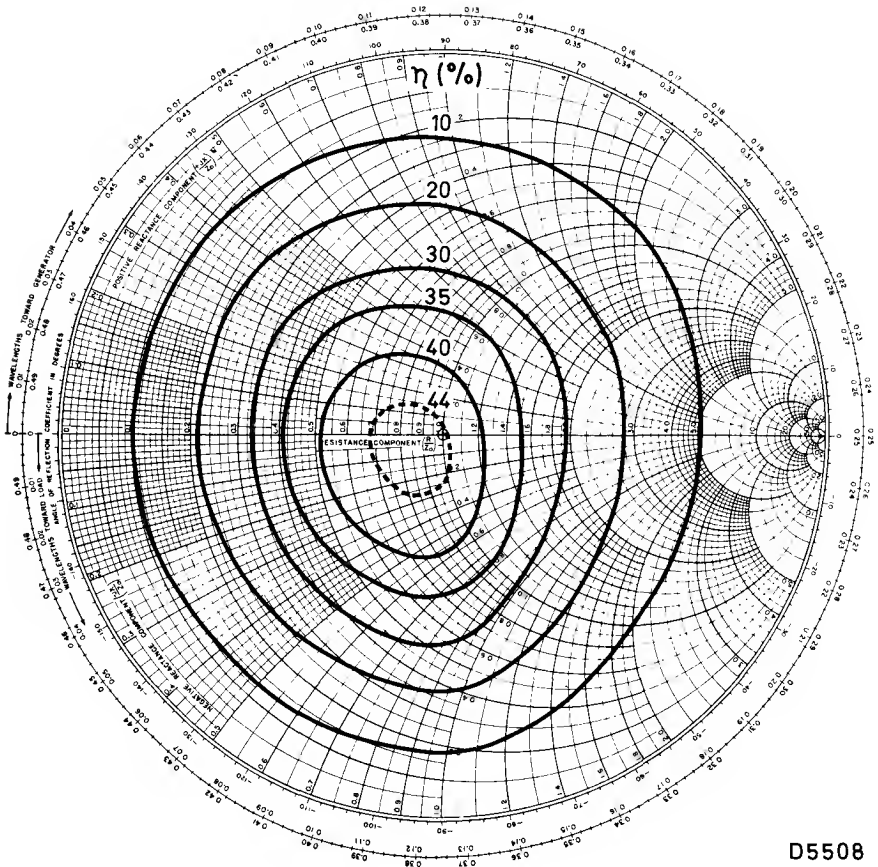


BGY22/23 or BGY22A/23A CASCADED AMPLIFIER AT 470 MHz
TYPICAL VARIATION OF LOAD POWER WITH LOAD IMPEDANCE

$$V_{CC} = 13.5V$$

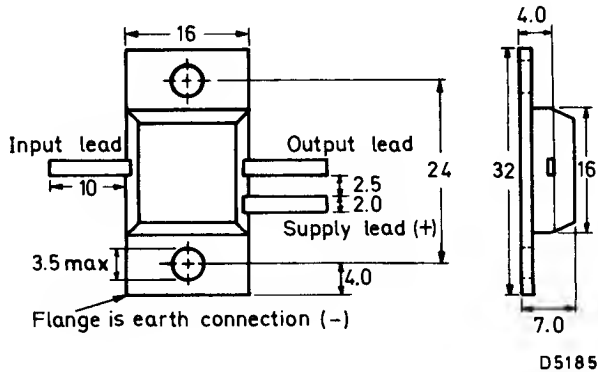
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APPLICATION INFORMATION (Cont'd)



BGY22/23 or BGY22A/23A CASCADED AMPLIFIER AT 470 MHz
TYPICAL VARIATION OF OVERALL EFFICIENCY WITH LOAD IMPEDANCE
 $V_{CC} = 13.5V$

OUTLINE AND DIMENSIONS



All dimensions in millimetres

MOUNTING

To ensure good thermal contact between mounting base and heatsink, burrs or thickening at the edges of the heatsink holes should be removed and the package bolted down onto a flat surface.

Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for 10 seconds at least 1mm from the plastic.

CAUTION

This device incorporated Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR

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**N-P-N SILICON PLANAR
EPITAXIAL V.H.F. TRANSISTOR**

BLX13

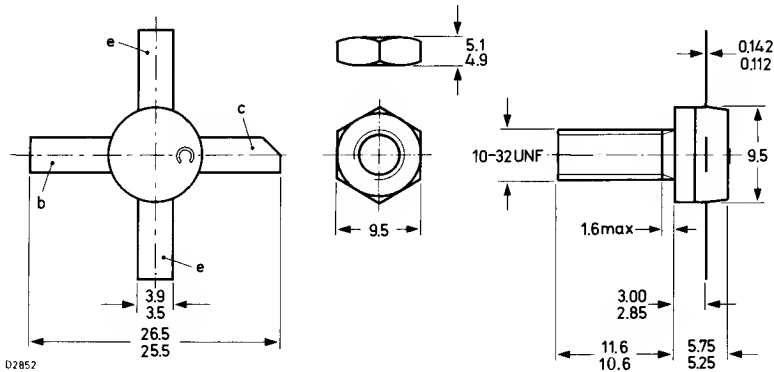
N-P-N silicon planar epitaxial transistor intended for s.s.b. in class A and AB and f.m. transmitting applications in class B with a supply voltage up to 28V. The transistor is designed to withstand severe load mismatch conditions. It has a capstan envelope with a moulded cap and all leads isolated from the stud.

QUICK REFERENCE DATA

Operation	Class	V _{CC} (V)	f ₁ (MHz)	f ₂ (MHz)	P _L (W)	G _p (dB)	d ₃ (dB)	I _C (A)	dt (%)
s. s. b.	A	26	28.000	28.001	0.8 (P. E. P.)	> 18	< -40	1.2	-
s. s. b.	AB	28	28.000	28.001	25 (P. E. P.)	> 18	typ. -35	typ. 1.28	typ. 35

Operation	Class	V _{CC} (V)	f (MHz)	P _S (W)	P _L (W)	G _p (dB)	I _C (A)	η (%)	\bar{z}_i (Ω)	\bar{V}_L (mA/V)
c. w.	B	28	70	typ. 0.5	25	typ. 17	typ. 1.49	typ. 60	0.53-j1.4	42.5-j54

OUTLINE AND DIMENSIONS



All dimensions in mm

Torque on nut: min. 15kg cm (1.5N m)
max. 17kg cm (1.7N m)

Diameter of clearance hole in heatsink: max. 5mm

Note: - Do not chamfer the edges of the mounting holes when removing burrs.

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RATINGS

Limiting values of operation according to the absolute maximum system

Electrical

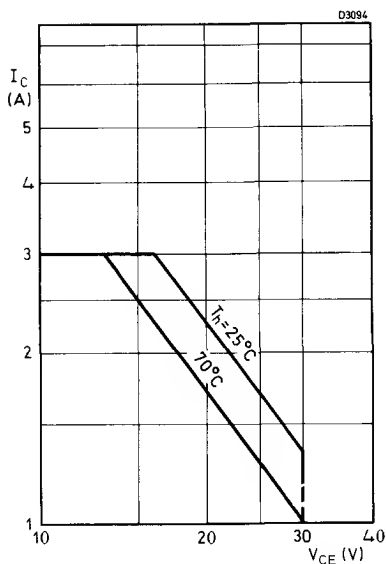
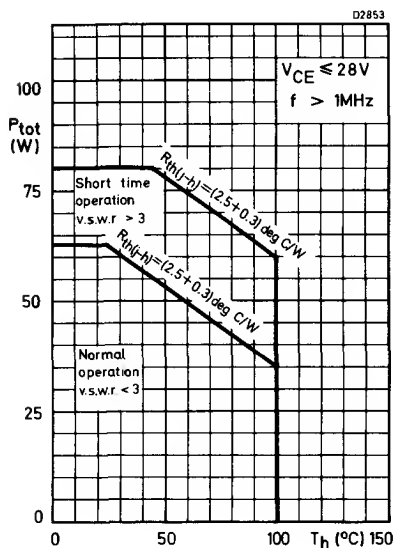
V_{CBOM} max.	65	V
V_{CEO} max.	36	V
V_{EBO} max.	4.0	V
$I_C(AV)$ max.	3.0	A
I_{CM} max. ($f > 1\text{MHz}$)	6.0	A
P_{tot} max. ($T_h = 25^\circ\text{C}$, $f > 1\text{MHz}$)	62.5	W

Temperature

T_{stg}	-30 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	2.5	degC/W
$R_{th(mb-h)}$	0.3	degC/W



SAFE OPERATING AREAS

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

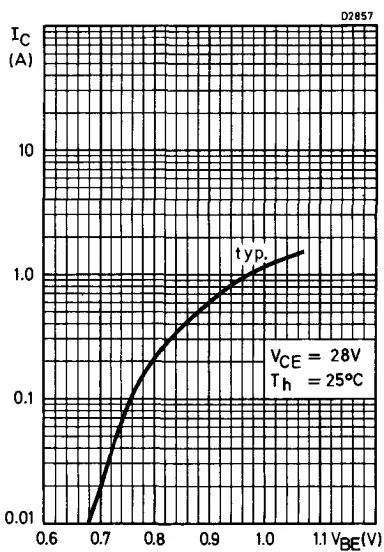
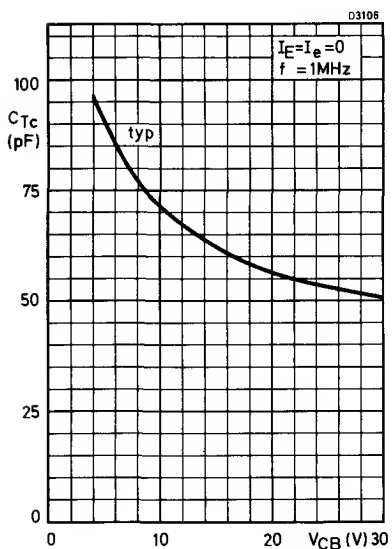
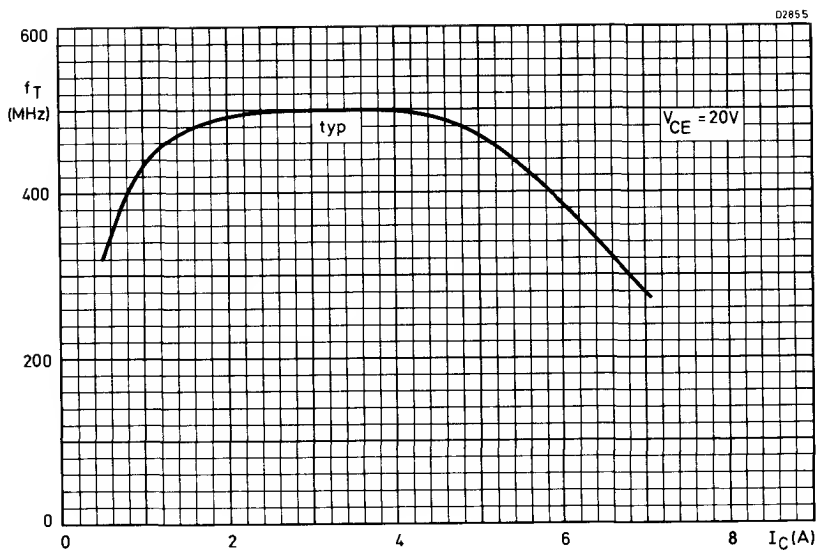
BLX13

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 50\text{mA}$, open emitter	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 50\text{mA}$, open base	36	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 10\text{mA}$, open collector	4.0	-	-	V
E	Transient energy $L = 25\text{mH}$, $f = 50\text{Hz}$ open base $-V_{BE} = 1.5\text{V}$, $R_{BE} = 33\Omega$	8.0 8.0	- -	- -	mWs mWs
h_{FE}	Static forward current transfer ratio $I_C = 1.0\text{A}$, $V_{CE} = 5\text{V}$	10	50	100	
f_T	Transition frequency $I_C = 3.0\text{A}$, $V_{CE} = 20\text{V}$	-	500	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 30\text{V}$, $f = 1\text{MHz}$	-	50	65	pF
$-C_{re}$	Feedback capacitance $I_C = 100\text{mA}$, $V_{CE} = 28\text{V}$	-	31	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

The issue of the information contained in this publication does not imply any authority or licence for the utilisation of any patented feature

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLX13

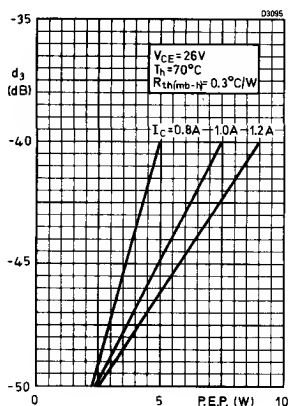
APPLICATION INFORMATION

R.F. performance in S.S.B. operation (linear power amplifier)

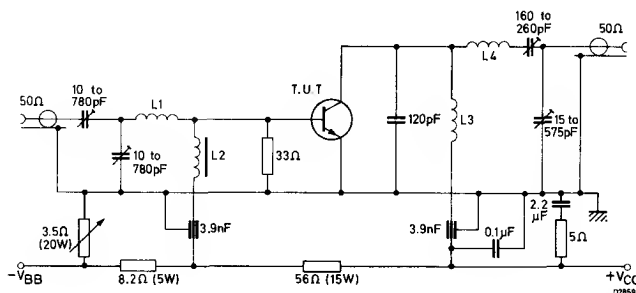
$$f_1 = 28.000\text{MHz}, f_2 = 28.001\text{MHz}$$

V_{CC} (V)	P_L (W)	G_p (dB)	d_3 (dB)	I_C (A)	T_h (°C)	Class
26	0-8 (P. E. P.)	> 18	< -40	1.2	≤ 25	A

*The figure given is the maximum encountered at any driving level between the specified values of P. E. P. and is referred to the according level of either of the equal amplified tones. Relative to the according peak envelope power this figure should be increased by 6dB.



Test circuit: Class A



L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total).

L2 = 7 turns of enamelled copper wire (0.7mm); 60μH.

L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.

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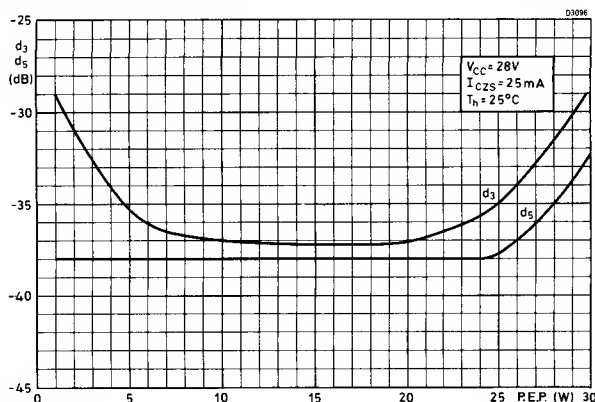
APPLICATION INFORMATION (contd.)

R.F. performance in S.S.B. operation (linear power amplifier)

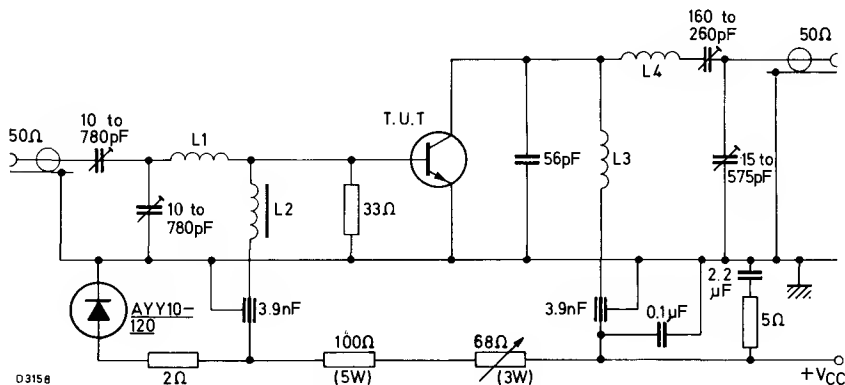
$$f_1 = 28.000\text{MHz}, f_2 = 28.001\text{MHz}, T_h \leq 25^\circ\text{C}$$

V_{CC} (V)	P_L (W)	G_p (dB)	$*d_3$ (dB)	dt (%)	I_{CZS} (mA)	I_C (A)	Class
28	25(P. E. P.)	>18	typ. -35	typ. 35	25	typ. 1.28	AB

*Intermodulation distortion figure quoted is related to the according level of either of the equal amplified tones. Relative to the according peak envelope power, this figure should be increased by 6dB.



Test circuit:- Class AB



L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total)

L2 = 7 turns of enamelled copper wire (0.7mm); 60μH.

L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.

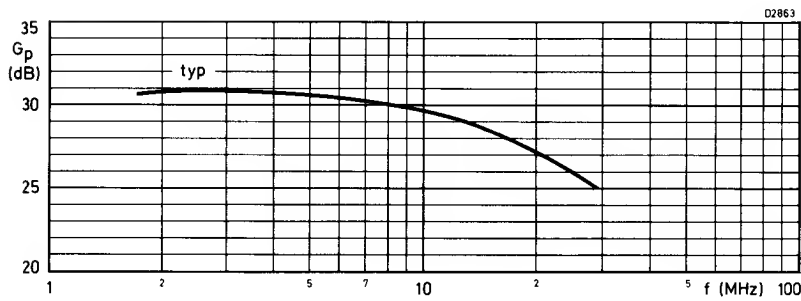
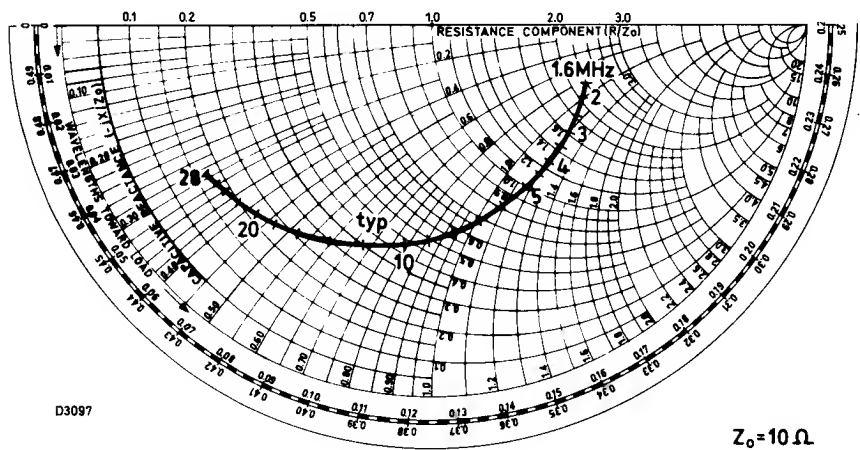
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N-P-N SILICON PLANAR
EPITAXIAL V.H.F. TRANSISTOR

BLX13

APPLICATION INFORMATION (contd.)

Typical large signal input impedance and transistor power gain in a class AB amplifier
at $V_{CC} = 28V$, $P_L = 25W(P.E.P.)$, $Z_L = 12.5\Omega$, $I_{CZS} = 25mA$, $T_h = 25^{\circ}C$.

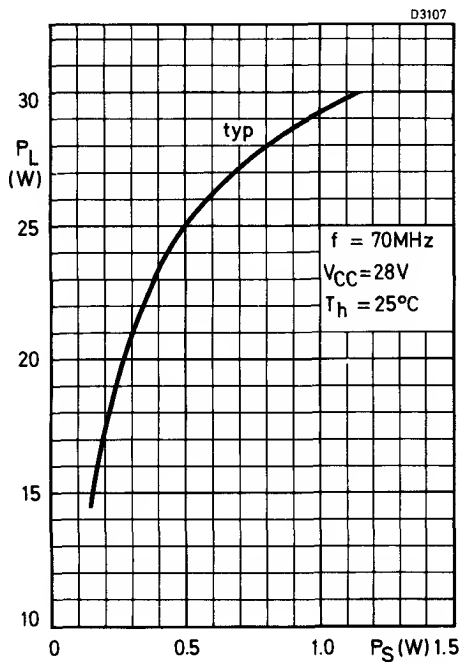


APPLICATION INFORMATION (contd.)

R. F. performance in C. W. operation (Class B)

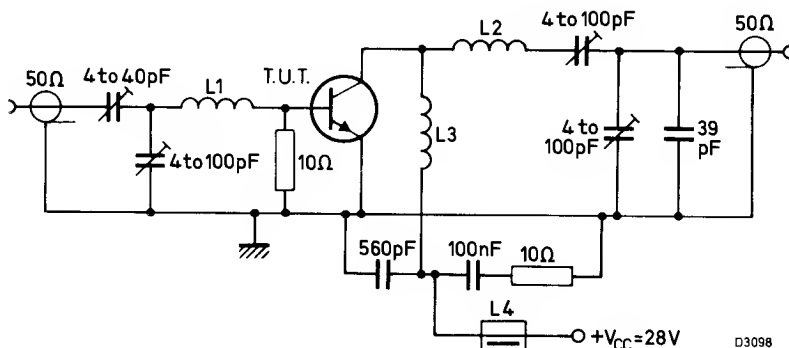
$$V_{CC} = 28V, T_h \leq 25^\circ C$$

f (MHz)	P _S (W)	P _L (W)	I _C (A)	G _p (dB)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mmho)
70	typ. 0.5	25	typ. 1.49	17	60	0.53-j1.4	42.5-j54



APPLICATION INFORMATION (contd.)

Test circuit:- 70MHz (class B)



L1 = 3 turns of enamelled copper wire (1.5mm) 93nH; int. dia. 10mm, length 8mm, leads 2×5 mm.

L2 = 5 turns of enamelled copper wire (1.5mm) 147nH; int. dia. 9mm, length 14mm, leads 2×5 mm.

L3 = 4 turns of enamelled copper wire (1.5mm) 118nH; int. dia. 9mm, length 10.5mm, leads 2×5 mm.

L4 = Ferroxcube choke

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

The Service Department
Mullard Limited
2 New Road
Mitcham Junction
Surrey. CR4 4XY.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

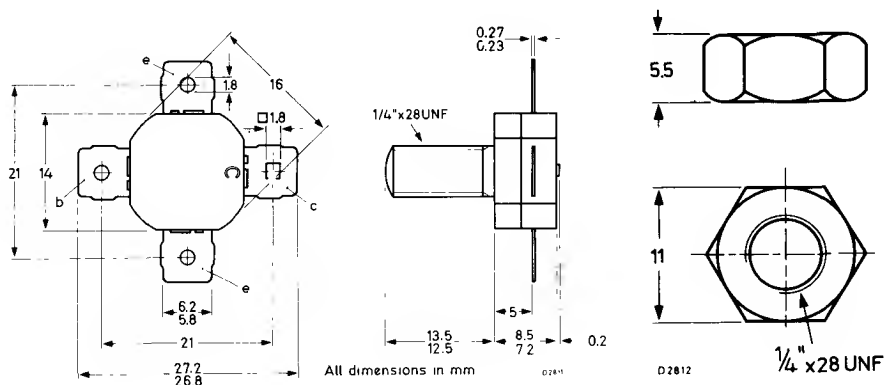
BLX14

Silicon n-p-n planar epitaxial transmitting transistor in a plastic stripline package, for use in s.s.b. and c.w. equipment with a 28V supply, operating in the v.h.f. band. The BLX14 is rated at 50W P. E. P. in the frequency range 1.6 to 28MHz (intermodulation better than 30dB down, full load mismatch permissible at stud temperatures up to 70°C) and at 50W for frequencies up to 70MHz in the c.w. operation.

QUICK REFERENCE DATA

Operation	Class	V _{CC} (V)	f (MHz)	P _L (W)	G _p (dB)	d ₃ (dB)	I _{CZS} (A)
s.s.b.	A	28	1.6 to 28	15(P. E. P.)	> 13	typ. -40	2.0
s.s.b.	AB	28	1.6 to 28	7.5 to 50 (P. E. P.)	> 13	< -30	0.1
c.w.	B	28	70	50	> 7.5		
c.w.	B	28	30	50	typ. 16		

OUTLINE AND DIMENSIONS



Torque on nut: 23kg cm (2.3N m) min.
27kg cm (2.7N m) max.

Diameter of clearance hole in heatsink: 6.5mm max.

Note: Do not chamfer the edges of the mounting holes when removing burrs.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

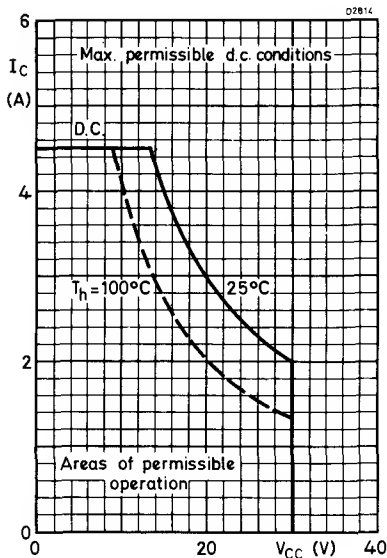
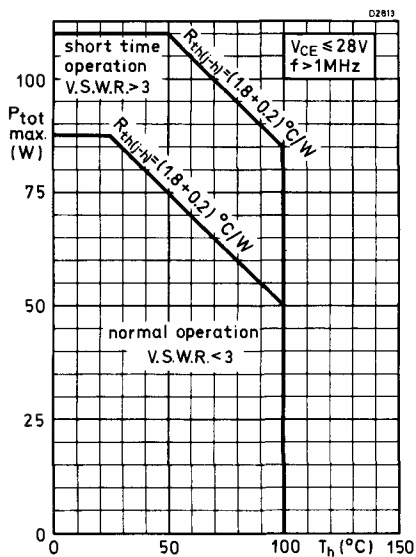
V_{CBOM} max.	85	V
V_{CERM} max. ($R_{BE} = 10\Omega$)	85	V
V_{CEO} max.	36	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	4.0	A
I_{CM} max. ($f > 1\text{MHz}$)	12	A
P_{tot} max. ($T_h < 25^\circ\text{C}$, $f > 1\text{MHz}$)	88	W

Temperature

T_{stg}	-65 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$	1.8	degC/W
$R_{th(mb-h)}$	0.2	degC/W

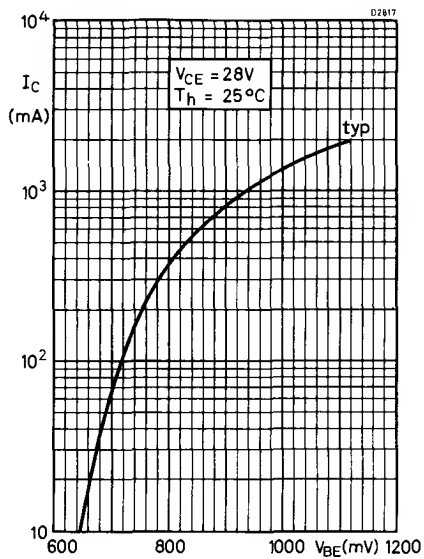
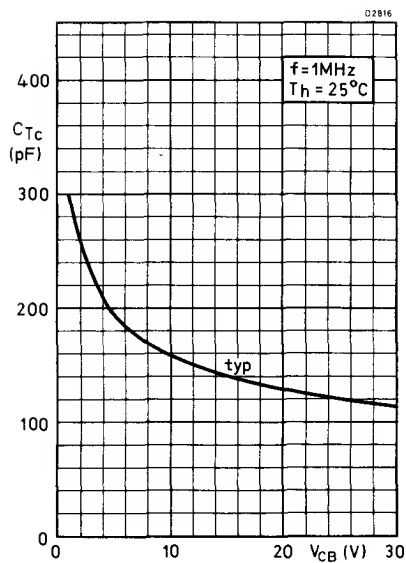
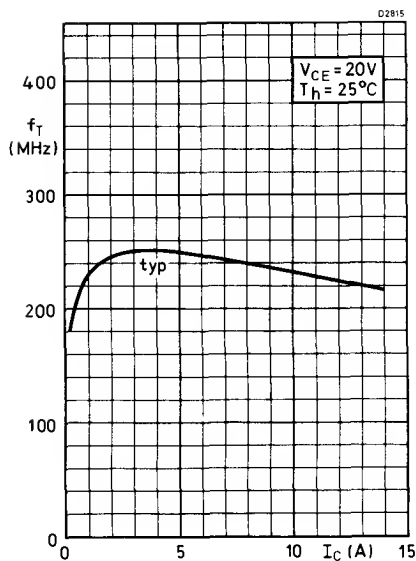


N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLX14

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter, $I_C = 25\text{mA}$	85	-	-	V
$V_{(BR)CER}$	Collector-emitter breakdown voltage $R_{BE} = 10\Omega$, $I_C = 25\text{mA}$	85	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage open base, $I_C = 50\text{mA}$	36	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector, $I_E = 10\text{mA}$	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 0.7\text{A}$, $I_B = 0.14\text{A}$	-	-	1.0	V
E	Transient energy				
	$L = 25\text{mH}$, $f = 50\text{Hz}$ open base	8.0	-	-	mWs
	$-V_{BE} = 1.5\text{V}$, $R_{BE} = 33\Omega$	8.0	-	-	mWs
h_{FE}	Static forward current transfer ratio $I_C = 1.4\text{A}$, $V_{CE} = 6\text{V}$	15	-	100	
f_T	Transition frequency $I_C = 3.0\text{A}$, $V_{CE} = 10\text{V}$	-	250	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 30\text{V}$, $f = 1\text{MHz}$	-	115	125	pF
$-C_{re}$	Feedback capacitance $I_C = 100\text{mA}$, $V_{CE} = 28\text{V}$, $f = 1\text{MHz}$	-	90	-	pF
C_{cs}	Collector-stud capacitance	-	3.5	-	pF



APPLICATION INFORMATION

R.F. performance in S.S.B. operation (linear power amplifier)

$$V_{CC} = 28V; T_h \text{ up to } 25^{\circ}C$$

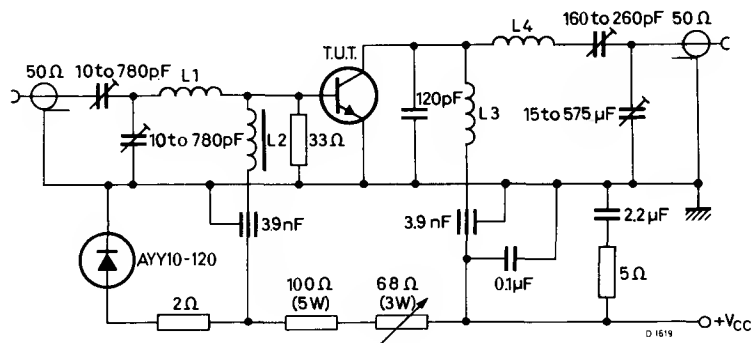
$$f_1 = 28.000MHz; f_2 = 28.001MHz$$

Output power (W)	G_p (dB)	η_{dt} (%)	d_3^{\dagger} (dB)	d_5^{\dagger} (dB)	I_{CZS} (A)	I_C (A)	Class
7.5 to 50 (P.E.P.)	> 13	> 35	< -30	< -30	0.1	< 2.55	AB

At temperatures up to $90^{\circ}C$ the output power relative to that at $25^{\circ}C$ is diminished by a factor of $-40mW/degC$.

The transistor is designed to withstand a full load mismatch operating under 50W P.E.P. at $V_{CC} = 28V$ and $T_h = 70^{\circ}C$.

Test circuit: - Class A-B



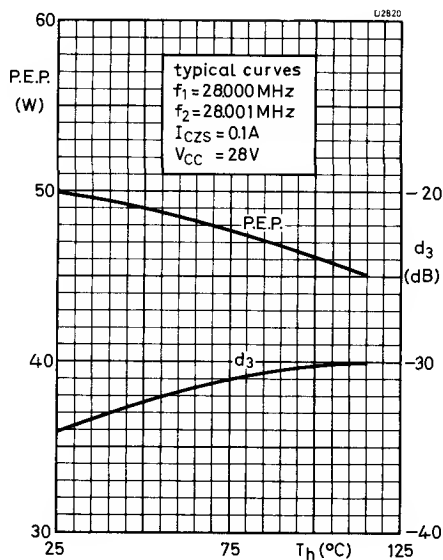
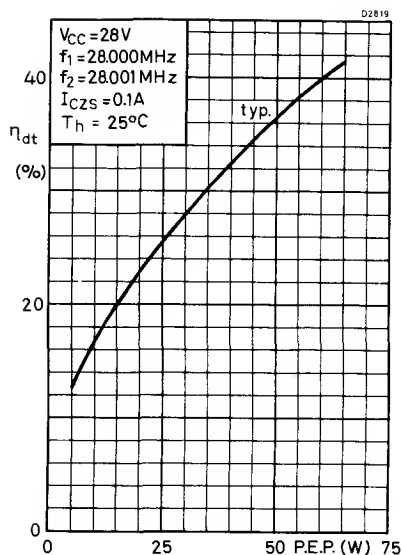
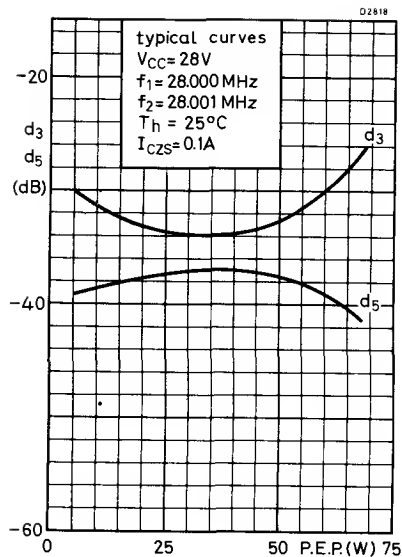
L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total).

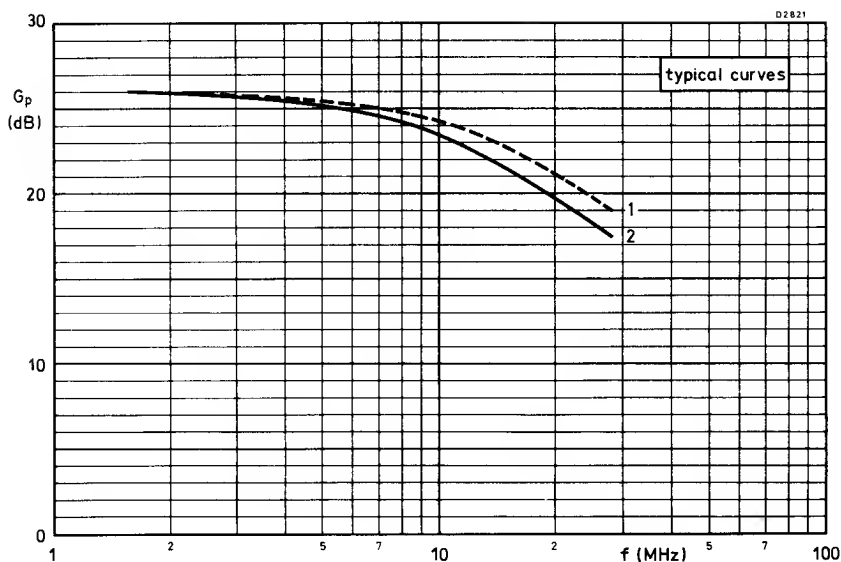
L2 = 7 turns of enamelled copper wire (0.7mm); $60\mu H$.

L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.

\dagger Maximum values encountered at any level of drive refer to the amplitude of either of the two equal tones at that level.





S.S.B. class AB operation

$$P_L = 50W \text{ P. E. P.}$$

$$V_{CC} = 28V$$

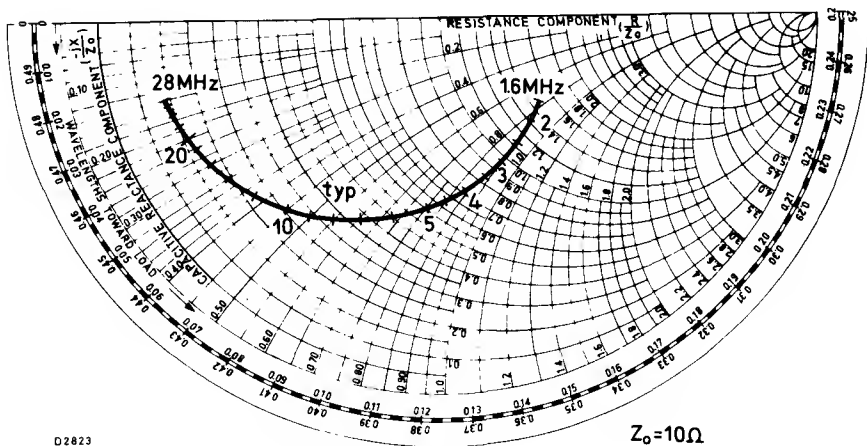
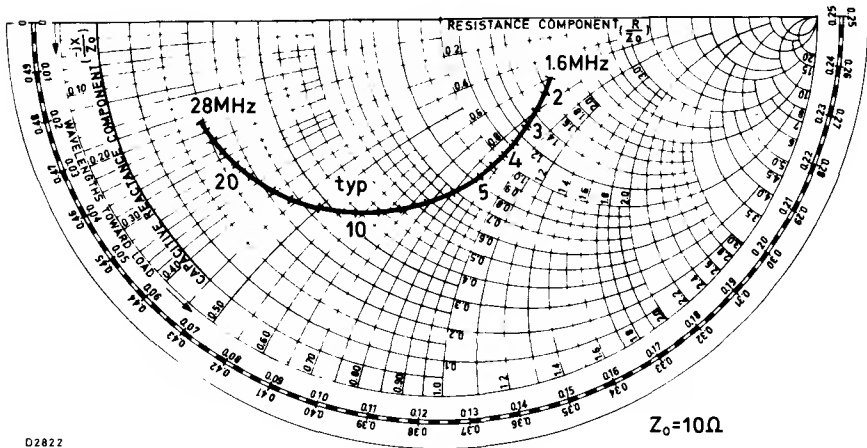
$$I_C = 100mA$$

$$Z_L = 6.25\Omega$$

$$T_h = 25^\circ C$$

Curves

1. This curve applies to a push-pull amplifier with cross neutralisation.
Collector-base neutralising capacitor = 82pF.
2. This curve applies to an un-neutralised amplifier.



S.S.B. class AB operation

$$P_L = 50W \text{ P. E. P.}$$

$$V_{CC} = 28V$$

$$I_C = 100mA$$

$$Z_L = 6.25\Omega$$

$$T_h = 25^\circ C$$

The upper curve applies to a push-pull amplifier with cross neutralisation.
Collector-base neutralising capacitor = 82pF

The lower curve applies to an un-neutralised amplifier.

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLX14

APPLICATION INFORMATION (contd.)

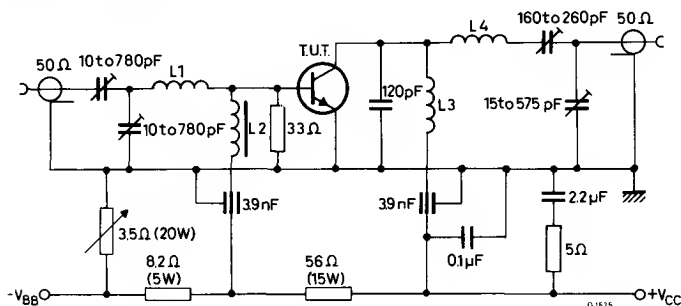
R.F. performance in S.S.B. operation (linear power amplifier)

$$V_{CC} = 28V, T_h \text{ up to } 25^{\circ}C, f_1 = 28.000MHz, f_2 = 28.001MHz$$

Output power (W)	G_p (dB)	η_{dt} (%)	d_3^{\dagger} (dB)	d_5^{\dagger} (dB)	I_C (A)	Class
15 P.E.P.	> 13	-	typ. -40	typ. -45	2.0	A

\dagger See note on page 5.

Test circuit: - Class A

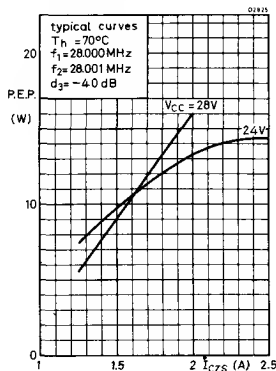
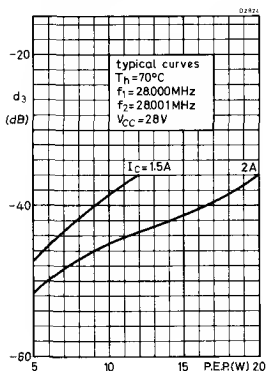


L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total).

L2 = 7 turns of enamelled copper wire (0.7mm); 60μH.

L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.



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APPLICATION INFORMATION (contd.)

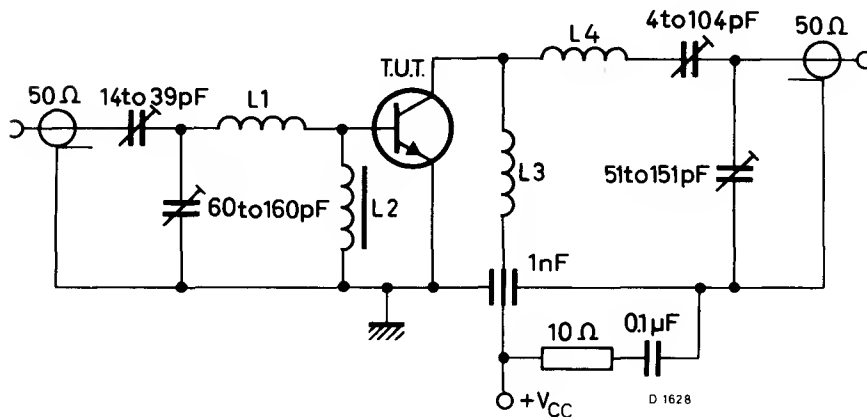
R. F. performance in c. w. operation (class B)

$V_{CC} = 28V$, T_h up to $25^{\circ}C$

f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mA/V)
70	< 8.9	50	< 3.25	> 7.5	> 55	$1.0 + j0.2$	$115 - j77$
50	typ. 4	50	typ. 3.25	typ. 11	typ. 55	$0.9 - j0.5$	$104 - j85$
30	typ. 1.2	50	typ. 3.25	typ. 16	typ. 55	$0.75 - j1.6$	$89 - j101$

At temperatures up to $90^{\circ}C$ the output power relative to that at $25^{\circ}C$ is diminished by a factor of $\sim 40mW/degC$.

Test circuit: - $f = 70MHz$



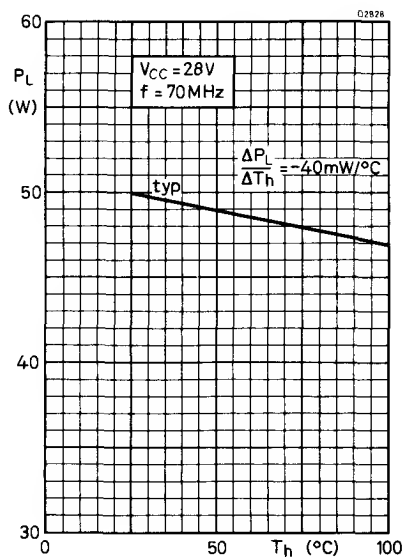
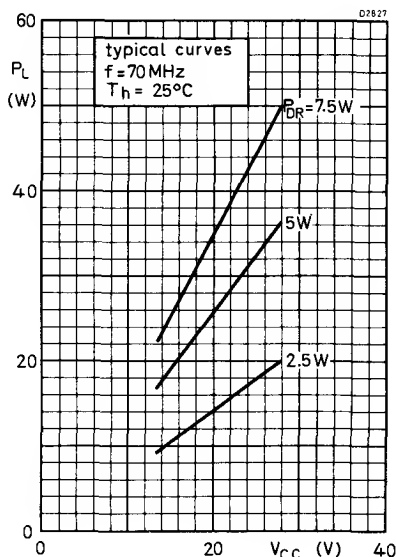
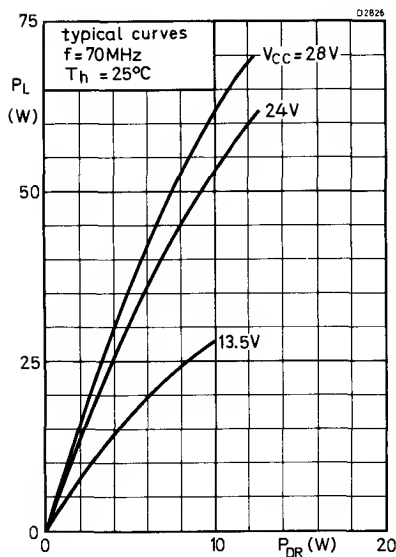
L1 = 60mm of straight enamelled copper wire (1.5mm); 9mm above chassis

L2 = FXC choke coil

L3 = 2 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int. dia. 10mm, leads 55mm (total)

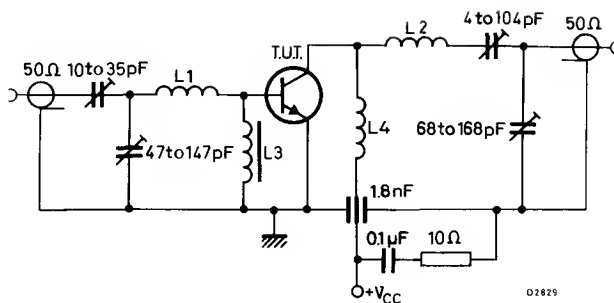
L4 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm, leads 50mm (total)

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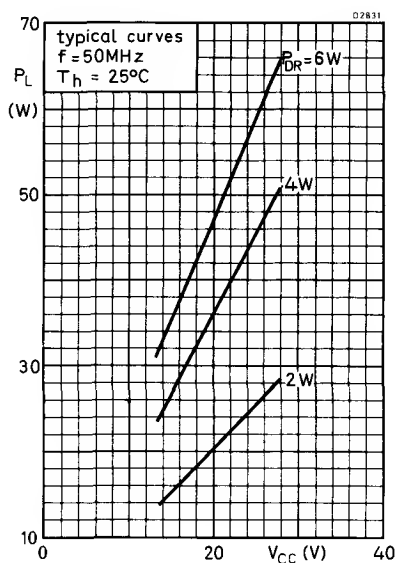
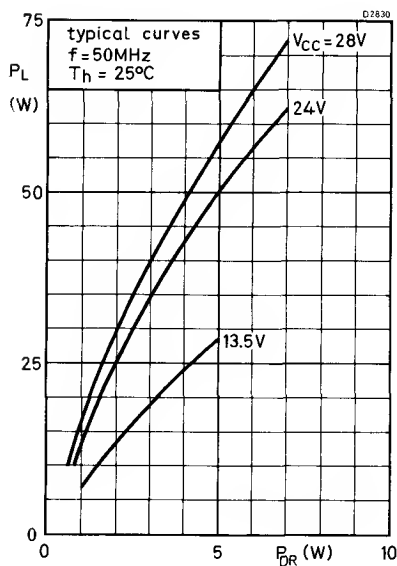


APPLICATION INFORMATION (contd.)

Test circuit:- $f = 50\text{MHz}$



- L1 = 1 turn of enamelled copper wire (1.5mm); int.dia. 10mm; leads 40mm (total)
- L2 = 4 turns of enamelled copper wire (1.5mm); int.dia. 12mm; leads 40mm (total)
- L3 = FXC choke coil
- L4 = 3 turns of enamelled copper wire (1.5mm); int.dia. 10mm; leads 40mm (total), winding pitch 2mm

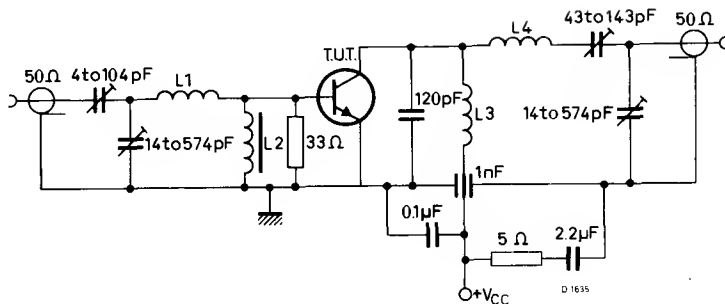


N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLX14

APPLICATION INFORMATION (contd.)

Test circuit: - $f = 30\text{MHz}$

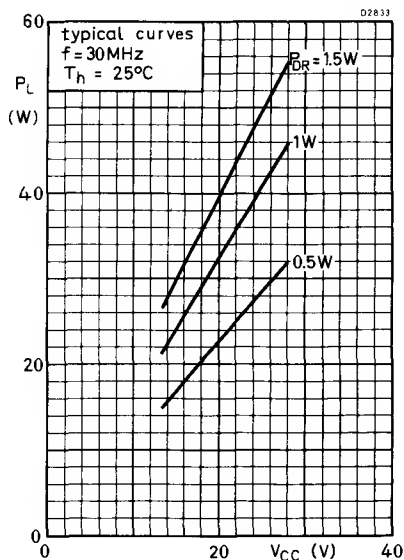
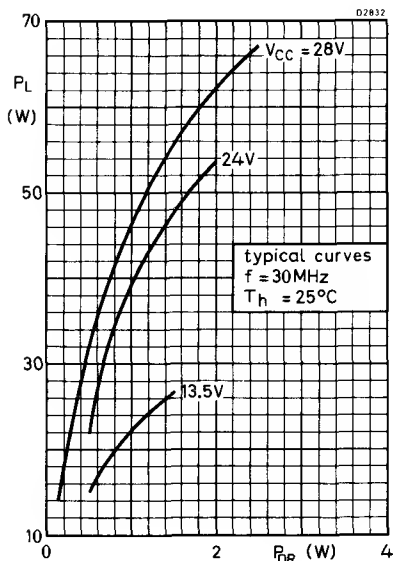


L1 = 2 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia. 10mm; leads 60mm (total)

L2 = 7 turns of enamelled copper wire (0.7mm); 60μH

L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia. 10mm; leads 50mm (total)

L4 = 6 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia. 12mm; leads 50mm (total)



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CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

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THE SERVICE DEPARTMENT
MULLARD LIMITED
2 NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4 XY.

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX65

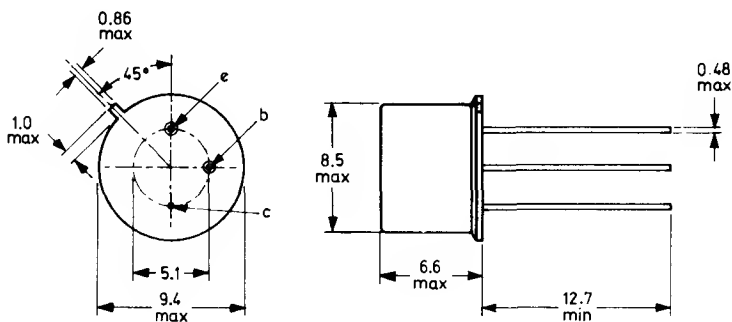
Silicon n-p-n transistor, mounted in a TO-39 envelope, for v.h.f./u.h.f. mobile applications. With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLX65 will produce typically 2.0W output into a 50 Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50 Ω (W)	η (%)	T_c (°C)	Circuit
12.5	470	0.5	2.0 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	0.4	2.0 typ.	66 typ.	25	
12.5	175	0.12	2.0 typ.	75 typ.	25	

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-3/SB3-3B
J. E. D. E. C. TO-39



All dimensions in mm

D1574

Collector connected to case

The maximum lead diameter is guaranteed only for 12.7mm

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CESM} max. ($R_{BE} = 0$)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. ($f \geq 10\text{MHz}$)	2.0	A
P_{tot} max. ($f \geq 10\text{MHz}$, $T_c \leq 90^\circ\text{C}$)	3.0	W

See also graph on page 3

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
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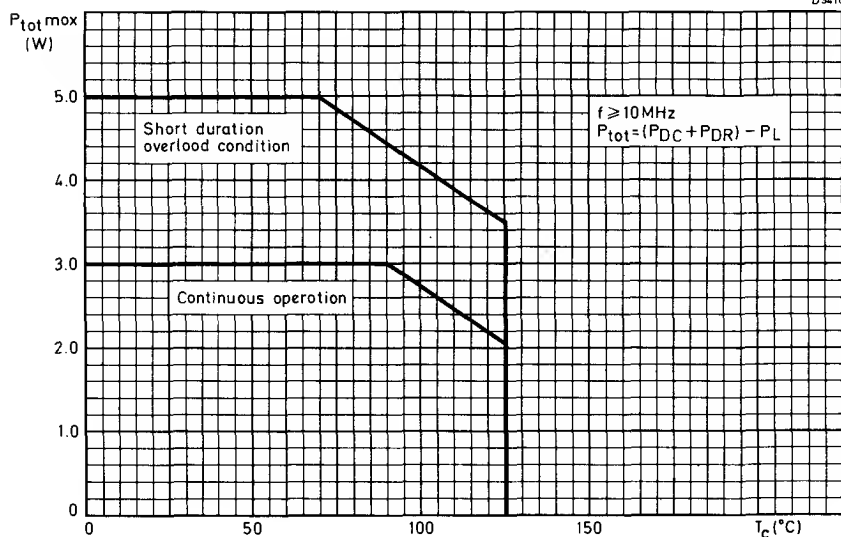
ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 25\text{mA}$	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
$V_{CE(sat)}$	Collector emitter saturation voltage $I_C = 100\text{mA}$, $I_B = 20\text{mA}$	-	0.1	-	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	10	40	-	
f_T	Transition frequency $I_C = 200\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1400	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	6.5	9.0	pF

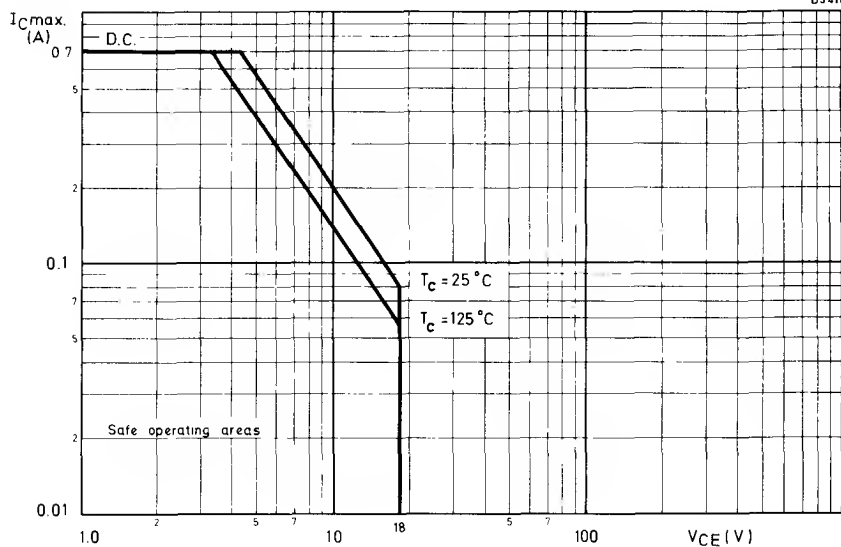
N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX65

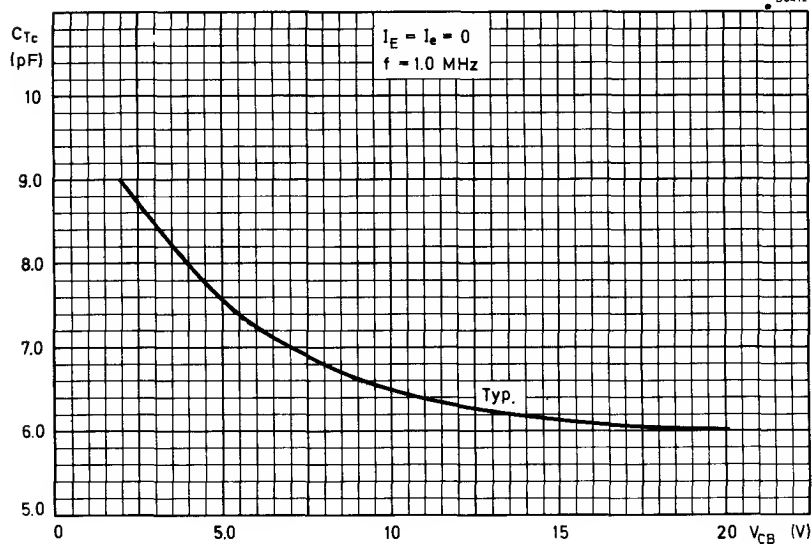
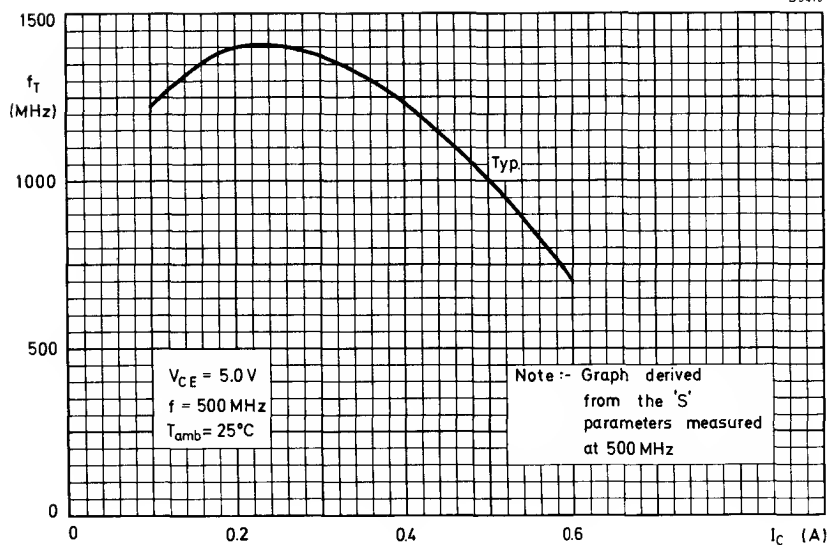
D3410



D3411



Mullard



N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX65

APPLICATION INFORMATION

R. F. Performance in c. w. operation ($T_c = 25^{\circ}\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
12.5	470	0.5	2.0 min.	65 min.	-	-
13.8	470	0.4	2.0 typ.	66 typ.	$5 + j10$	$16 - j50$
12.5	175	0.12	2.0 typ.	75 typ.	-	-

At $P_L = 2.0\text{W}$ and $V_{CC} = 12.5\text{V}$, the output power at case temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $5\text{mW}/^{\circ}\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$$V_{CC} = 16.5\text{V} \quad f = 470\text{MHz} \quad T_c = 70^{\circ}\text{C}$$

$$V.S.W.R. = 50:1 \quad \text{at any phase}$$

$$P_{DR} = P_{DR \text{ nom.}} + 20\%.$$

$$\text{Where } P_{DR \text{ nom.}} = P_{DR} \text{ for } 1.4\text{W transistor output into } 50\Omega$$

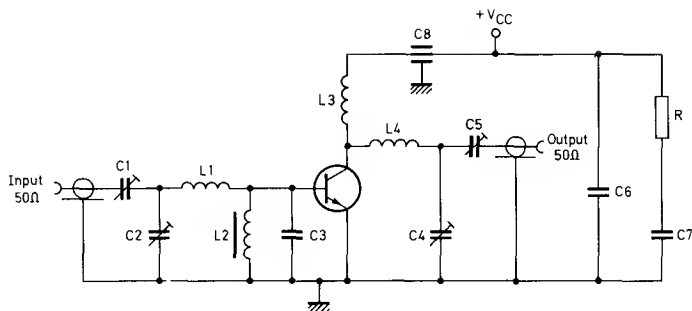
$$\text{load at } V_{CC} = 13.8\text{V}.$$

The issue of the information contained in this publication does not imply any authority or licence for the utilisation of any patented feature.

Mullard

APPLICATION INFORMATION (contd.)

470MHz Amplifier circuit



02580

Component values for 470MHz amplifier circuit

C1 = C2 = C4 = C5 = 1.8 to 18pF film dielectric trimmer capacitors

C3 = 22pF disc ceramic capacitor

C6 = 10nF ceramic capacitor

C7 = 0.1μF disc ceramic capacitor

C8 = 4nF feed-through capacitor

L1 = 1 turn of 1mm copper wire, int. dia. 5mm, lead length <1mm

L2 = 0.22μH choke

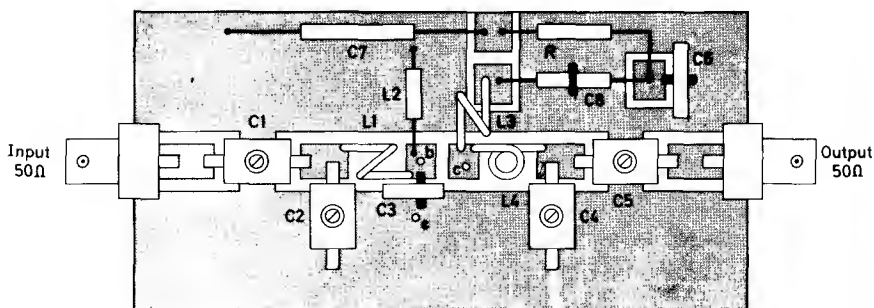
L3 = 1 turn of 1mm copper wire, int. dia. 7mm, lead length 2mm

L4 = 1 turn of 1mm copper wire, int. dia. 5mm, lead length 2mm

R = 10Ω - carbon

Component layout on 1.5mm single copper clad fibre-glass board

Dimensions of the board: - 80 × 40mm



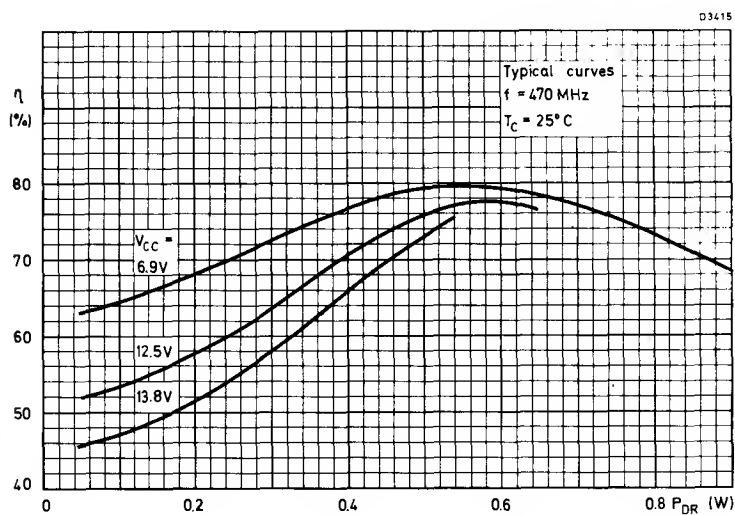
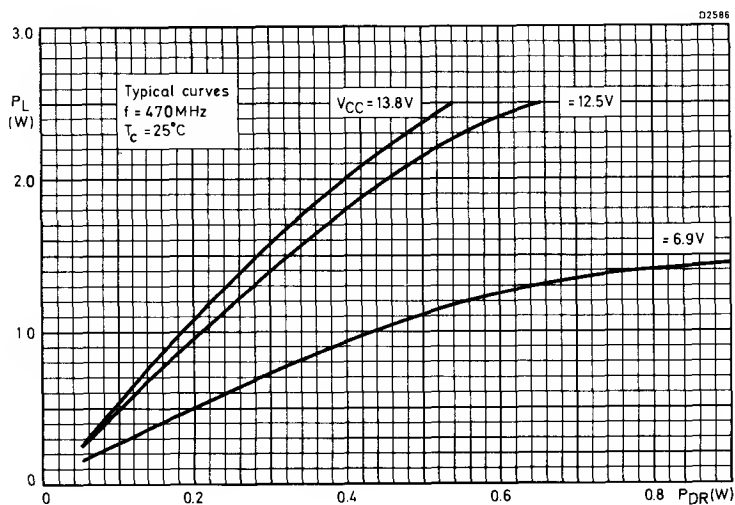
03414

Shaded area copper

To obtain the specified gain performance, the emitter lead length should not exceed 1.6mm.

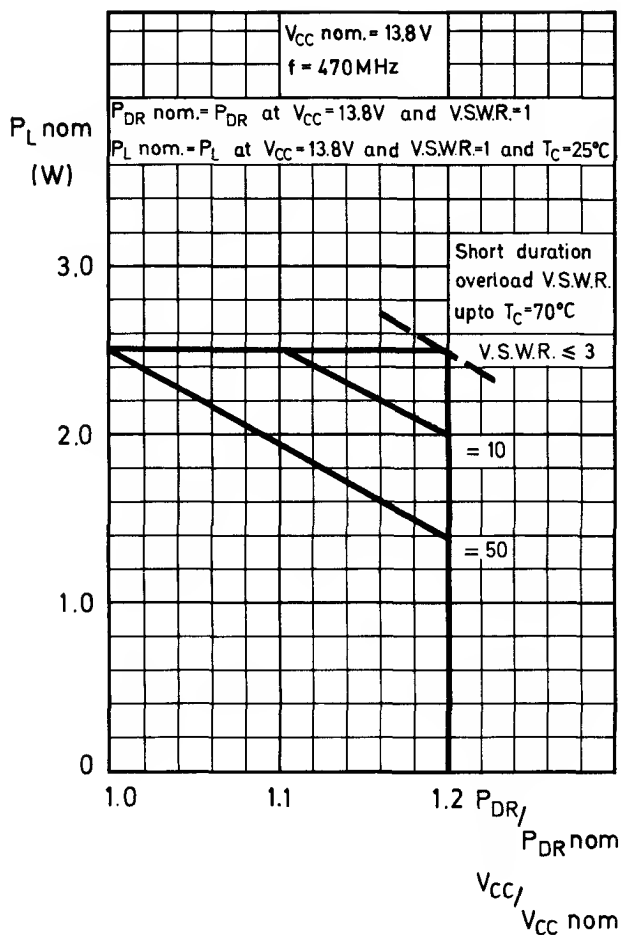
Mullard

APPLICATION INFORMATION (contd.)



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

D3416



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

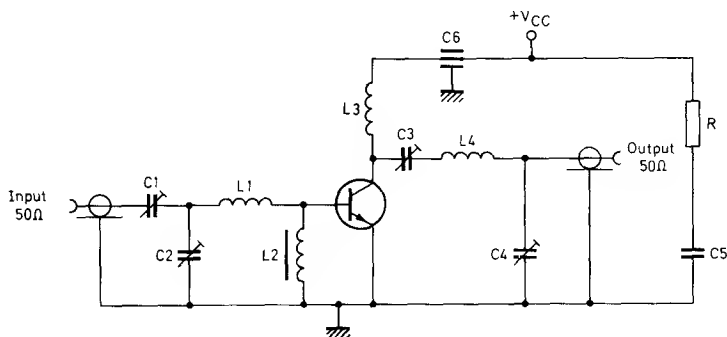
The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 2.5 watts load power in the circuit on page 6, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50:1 at a heatsink temperature of 70°C . This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX65

APPLICATION INFORMATION

175MHz Amplifier circuit



D2582

Component values for 175MHz amplifier circuit

C1 = C4 = 0 to 60pF

C2 = C3 = 0 to 30pF

concentric trimmer capacitors

C5 = 0, 25μF disc ceramic capacitor

C6 = 4nF feed-through capacitor

L1 = 25mm straight 1.2mm copper wire. Height above board = 3mm

L2 = 3 turns of 0.5mm copper wire on Ferrite FX1115

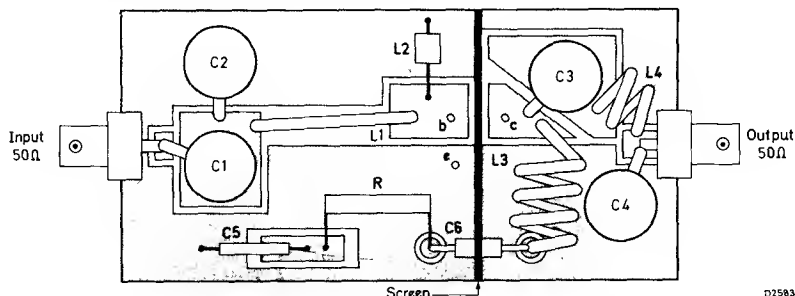
L3 = 5 turns of 1.2mm copper wire, int. dia. 10mm, close wound, lead length 5mm

L4 = 3 turns of 1.2mm copper wire, int. dia. 10mm, close wound, lead length 5mm

R = 10Ω - carbon

Component layout on 1.5mm single copper clad fibre-glass board

Dimensions of the board 80 × 40mm

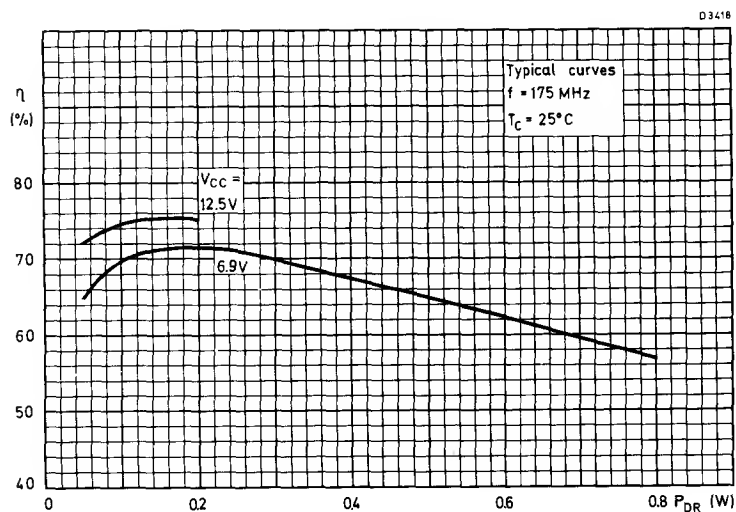
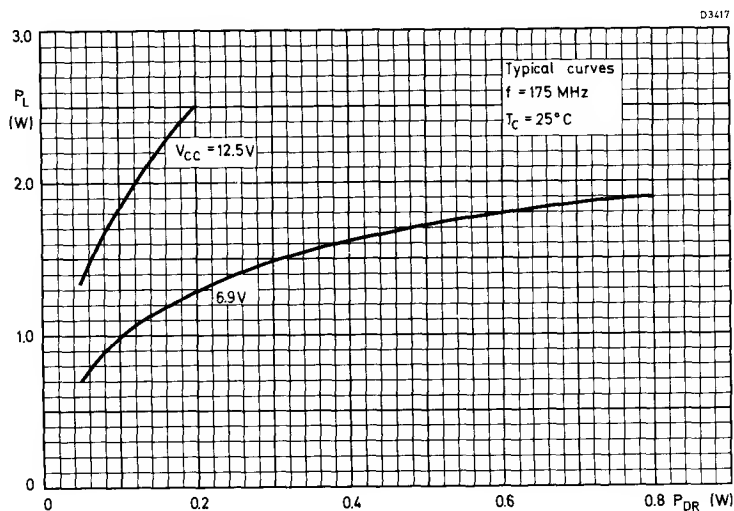


D2583

Shaded area copper

To obtain the specified gain performance, the emitter lead length should not exceed 1.6mm.

Mullard



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH
DRIVE POWER

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

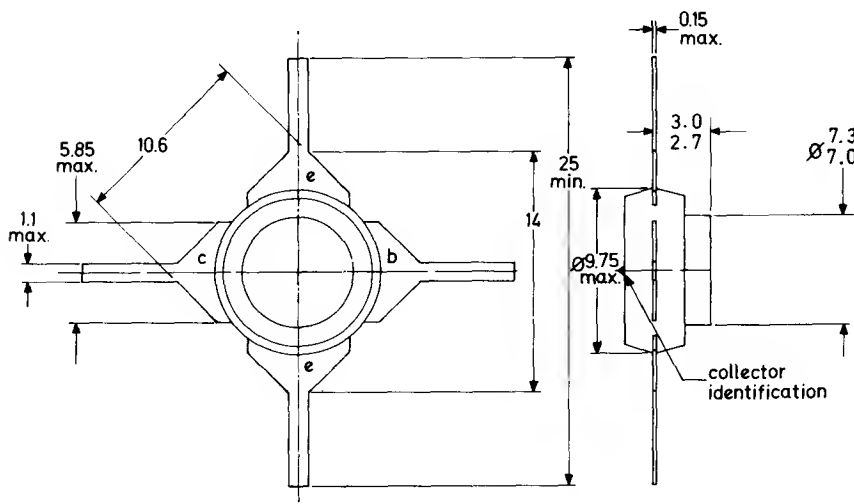
BLX66

Silicon n-p-n transistor for v. h. f. /u. h. f. mobile applications. The device is mounted in a plastic, studless, capstan strip-line encapsulation. With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLX66 will produce typically 2.5W output into a 50 Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50 Ω (W)	η (%)	T_{mb} (°C)	Circuit
12.5	470	0.35	2.5 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	0.28	2.5 typ.	75 typ.	25	
13.8	470	0.15	1.5 typ.	65 typ.	25	
12.5	175	0.03	3.0 typ.	84 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3419

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CESM} max. ($R_{BE} = 0$)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. ($f \geq 10\text{MHz}$)	2.0	A
P_{tot} max. ($f \geq 10\text{MHz}$, $T_{mb} \leq 90^\circ\text{C}$)	4.0	W

See also graph on page 3

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
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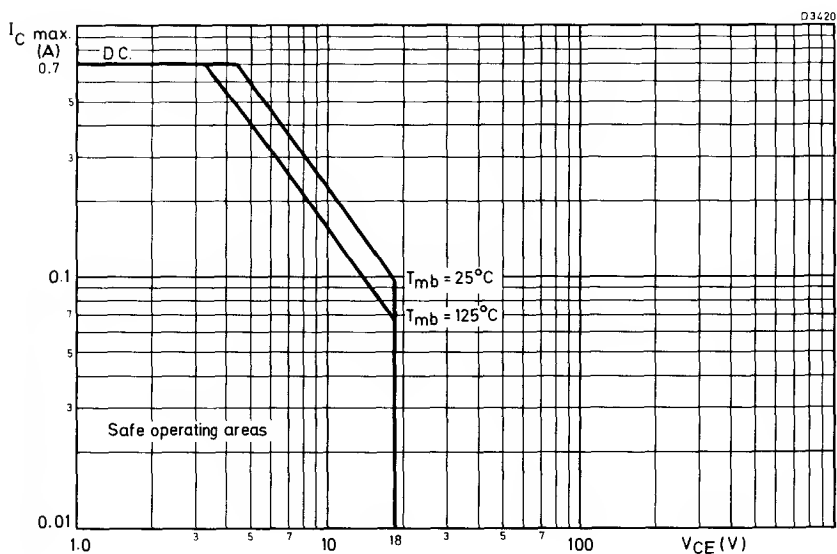
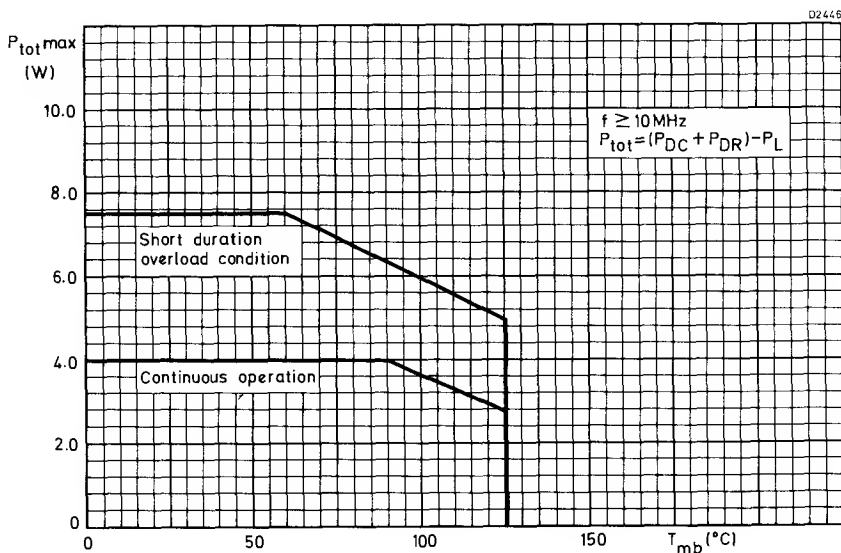
ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 25\text{mA}$	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100\text{mA}$, $I_B = 20\text{mA}$	-	0.1	-	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	10	40	-	
f_T	Transition frequency $I_C = 200\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1400	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	6.5	9.0	pF

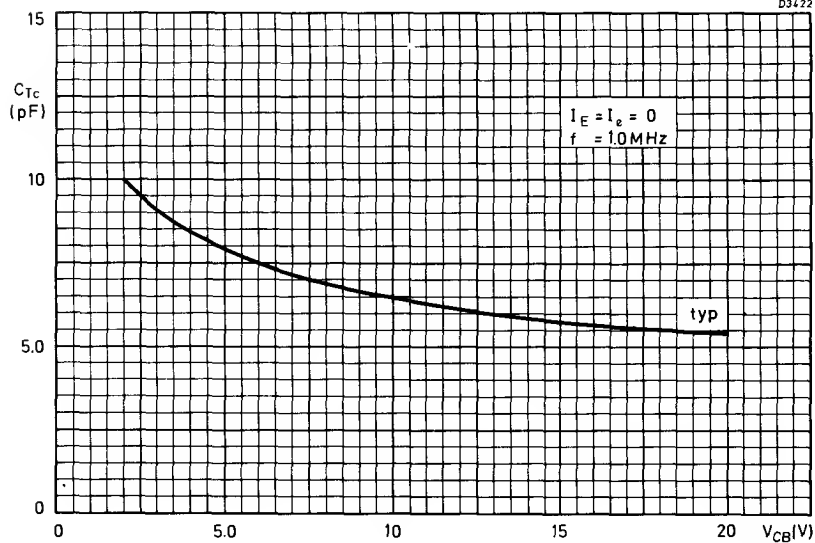
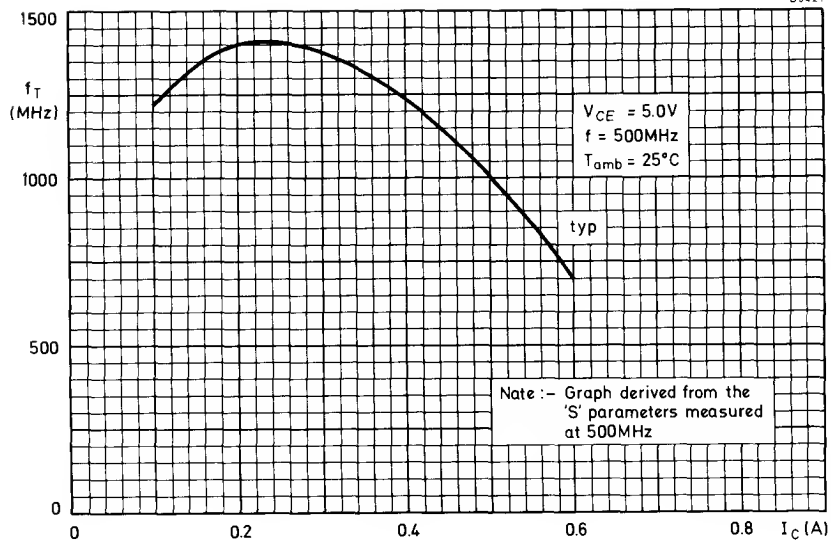
*Derived from the 'S' parameters measured at $f = 500\text{MHz}$, $T_{amb} = 25^\circ\text{C}$

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX66



Mullard



N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX66

APPLICATION INFORMATION

R. F. performance in c. w. operation ($T_{mb} = 25^{\circ}\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
12.5	470	0.35	2.5 min.	65 min.	-	-
13.8	470	0.28	2.5 typ.	75 typ.	$2.5 + j4.5$	$23 - j35$
13.8	470	0.15	1.5 typ.	65 typ.	-	-
12.5	175	0.03	3.0 typ.	84 typ.	$2.4 - j3.8$	$35 - j40$

At $P_L = 2.5\text{W}$ and $V_{CC} = 12.5\text{V}$, the output power at mounting-base temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $5\text{mW}/^{\circ}\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$$V_{CC} = 16.5\text{V}, \quad f = 470\text{MHz}, \quad T_{mb} = 70^{\circ}\text{C}$$

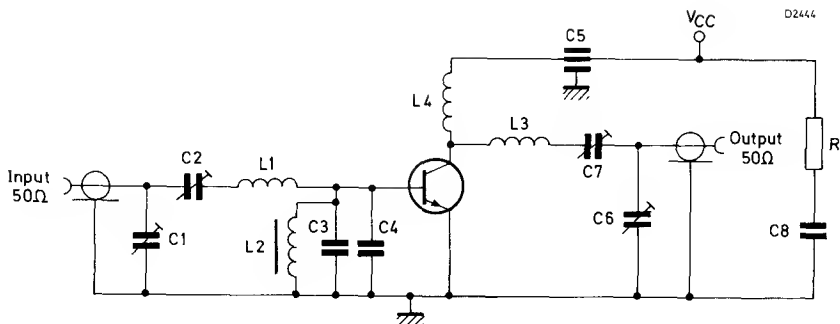
$$V.S.W.R. = 50:1 \quad \text{at any phase}$$

$$P_{DR} = P_{DR \text{ nom.}} + 20\%$$

Where $P_{DR \text{ nom.}} = P_{DR}$ for 2.5W transistor output into a 50Ω load at $V_{CC} = 13.8\text{V}$.

APPLICATION INFORMATION (contd.)

470MHz Amplifier circuit



Component values for 470MHz amplifier circuit

C1 = C2 = C6 = C7 = 1.8 to 18pF film dielectric trimmers

C3 = C4 = 18pF disc ceramic capacitors

C5 = 4nF feed-through capacitor

C8 = 0.1μF disc ceramic capacitor

L1 = 1 turn of 1.2mm copper wire, int. dia. 6mm, lead length < 1mm

L2 = 1μH choke

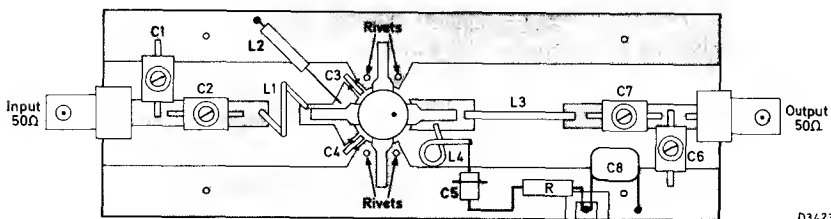
L3 = 30mm of straight 2mm copper wire. Height above board = 2mm

L4 = 2 turns of 0.5mm copper wire, int. dia. 3mm, close wound, lead length = 8mm

R = 10Ω - carbon

Component layout on 1.5mm double copper clad fibre-glass board

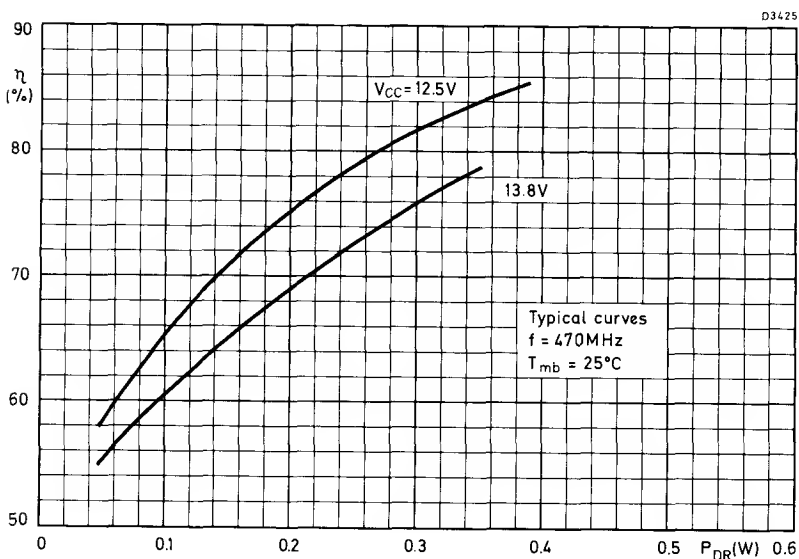
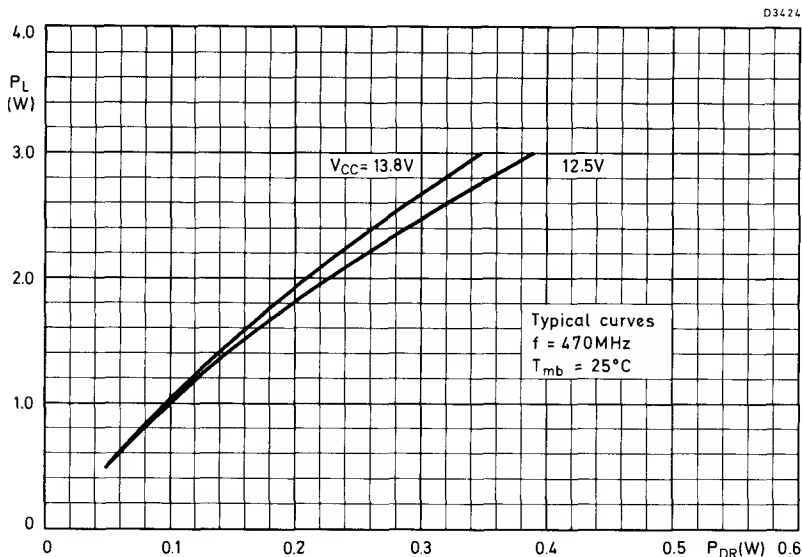
Dimensions of the board: - 110 × 50mm



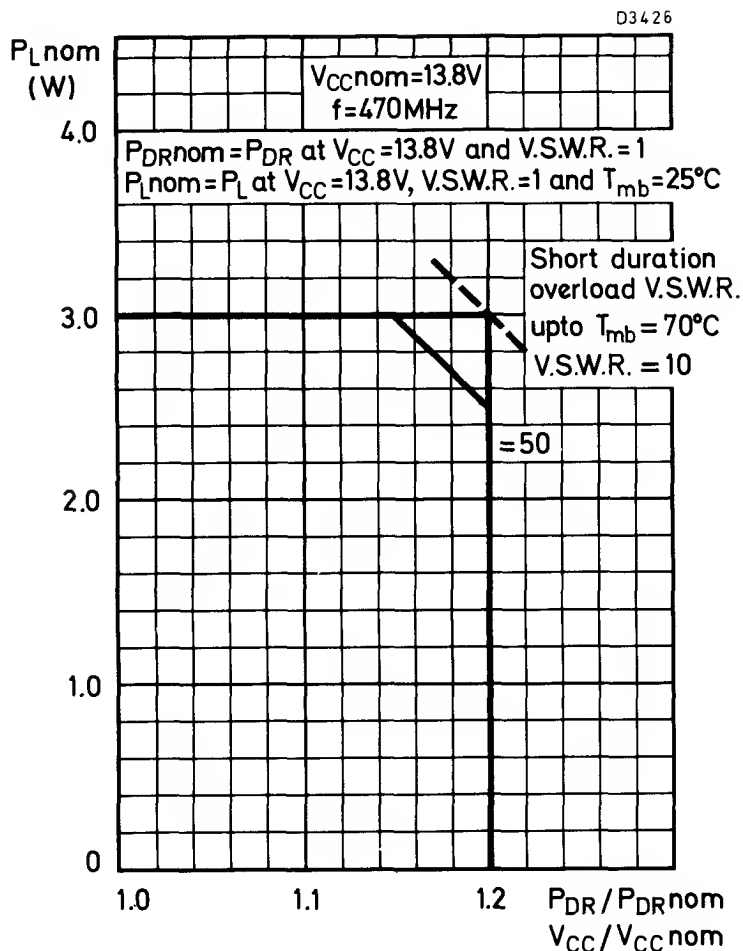
Shaded area copper

Underside area completely copper clad

Mullard



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 3 watts load power in the circuit on page 6, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50:1 at a heatsink temperature of 70°C . This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

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SURREY, CR4 4SR.

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N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

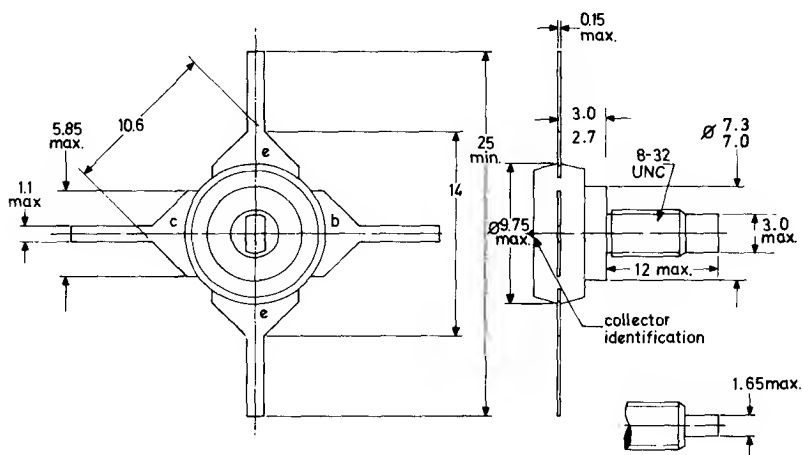
BLX67

Silicon n-p-n transistor for v. h. f. /u. h. f. mobile applications. The device is mounted in a plastic, capstan strip-line encapsulation. With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLX67 will produce typically 3W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
12.5	470	0.35	2.5 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	0.35	3.0 typ.	79 typ.	25	
13.8	470	0.15	1.5 typ.	65 typ.	25	
12.5	175	0.03	3.0 typ.	84 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CESM} max. ($R_{BE} = 0$)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. ($f \geq 10\text{MHz}$)	2.0	A
P_{tot} max. ($f \geq 10\text{MHz}$, $T_h \leq 90^\circ\text{C}$)	4.5	W

See also graph on page 3

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
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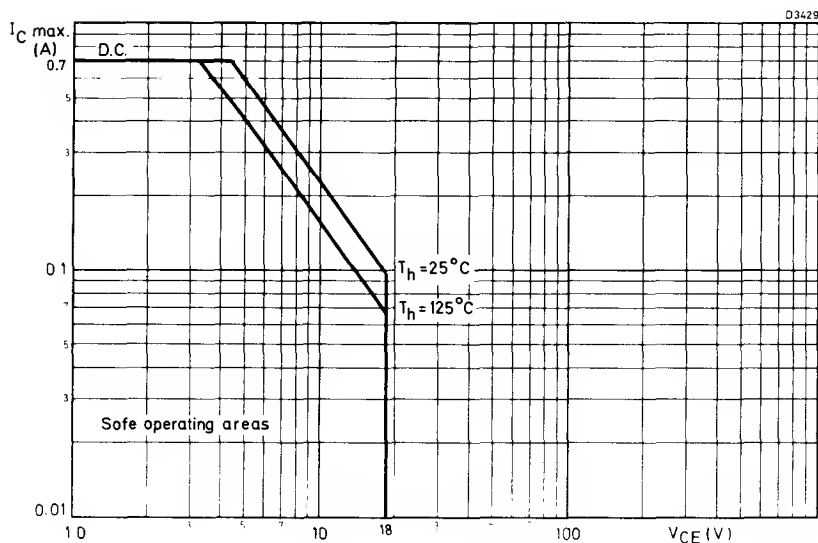
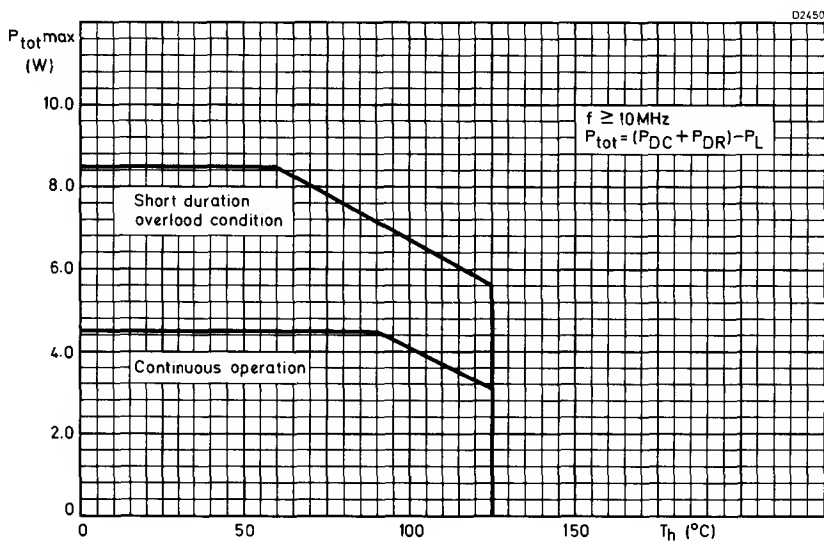
ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C \approx 25\text{mA}$	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C \approx 100\text{mA}$, $I_B = 20\text{mA}$	-	0.1	-	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	10	40	-	
$*f_T$	Transition frequency $I_C = 200\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1400	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	6.5	9.0	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

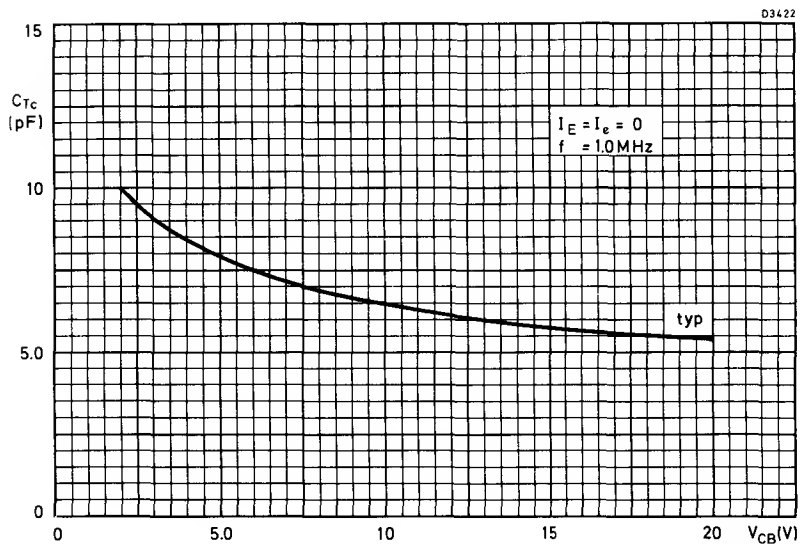
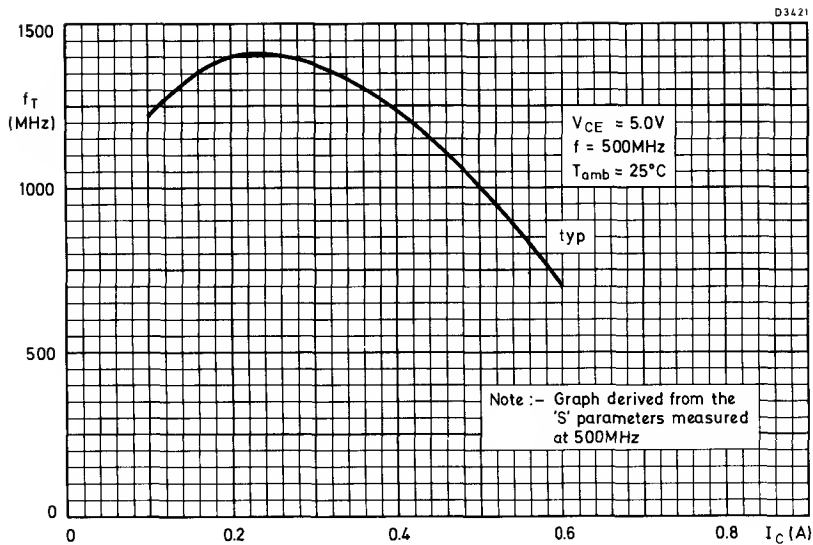
*Derived from the 'S' parameters measured at $f = 500\text{MHz}$, $T_{amb} = 25^\circ\text{C}$

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX67



Mullard



N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX67

APPLICATION INFORMATION

R.F. performance in c. w. operation ($T_h = 25^\circ\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mmho)
12.5	470	0.35	2.5 min.	65 min.	-	-
13.8	470	0.35	3.0 typ.	79 typ.	3+j5	27-j38
13.8	470	0.15	1.5 typ.	65 typ.	-	-
12.5	175	0.03	3.0 typ.	84 typ.	2.4-j3.8	35-j40

At $P_L = 2.5\text{W}$ and $V_{CC} = 12.5\text{V}$, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $5\text{mW}/^\circ\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions:

$$V_{CC} = 16.5\text{V}, \quad f = 470\text{MHz} \quad T_h = 70^\circ\text{C}$$

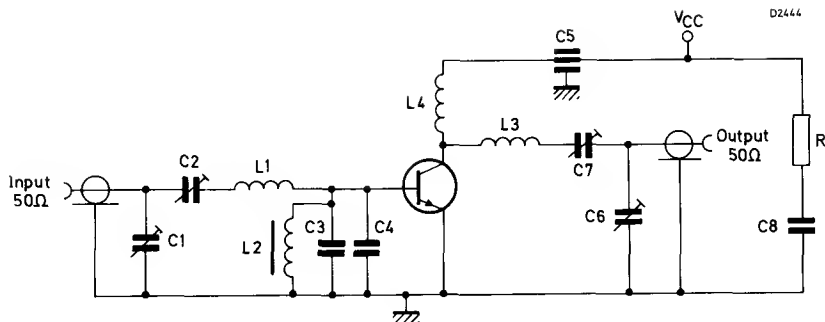
$$V.S.W.R. = 50:1 \quad \text{at any phase}$$

$$P_{DR} = P_{DR \text{ nom.}} + 20\%$$

Where $P_{DR \text{ nom.}} = P_{DR}$ for 2.5W transistor output into a 50Ω load at $V_{CC} = 13.8\text{V}$.

APPLICATION INFORMATION (contd.)

470MHz Amplifier circuit



Component values for 470MHz amplifier circuit

C1 = C2 = C6 = C7 = 1.8 to 18pF film dielectric trimmers

C3 = C4 = 18pF disc ceramic capacitors

C5 = 4nF feed-through capacitor

C8 = 0.1μF disc ceramic capacitor

L1 = 1 turn of 1.2mm copper wire, int. dia. 6mm, lead length <1mm

L2 = 1μH choke

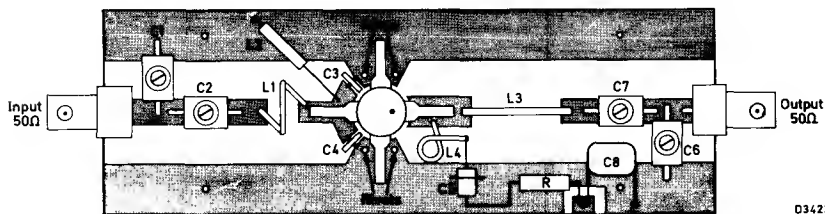
L3 = 30mm of straight 2mm copper wire. Height above board = 2mm

L4 = 2 turns of 0.5mm copper wire int. dia. 3mm, close wound, lead length = 8mm

R = 10Ω - carbon

Component layout on 1.5mm double copper clad fibre-glass board

Dimensions of the board: - 110 × 50mm

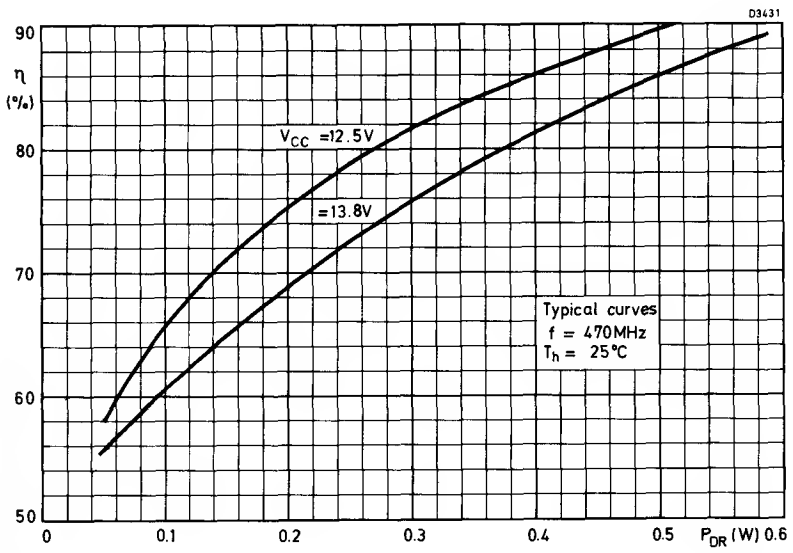
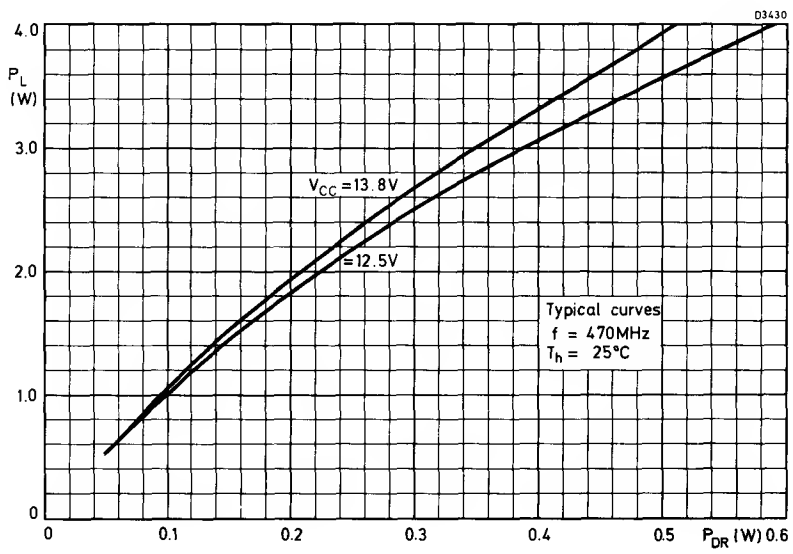


Shaded area copper

Underside area completely copper clad

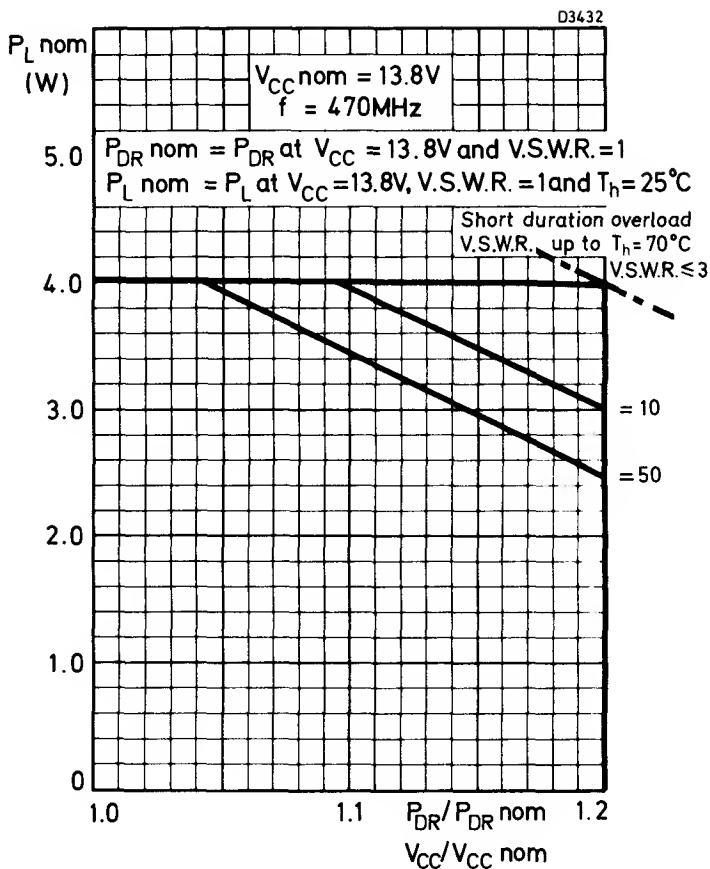
**N-P-N SILICON PLANAR
V.H.F./U.H.F. TRANSISTOR**

BLX67



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

Mullard



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 4 watts load power in the circuit on page 6, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50:1 at a heatsink temperature of 70°C . This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

CAUTION

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N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

N-P-N epitaxial planar transistor intended for use in class A, B and C operated mobile, industrial and military transmitters with a supply voltage of 13.5 V. The transistor is resistance stabilized. Every transistor is tested under severe load mismatch conditions with a supply overvoltage to 16.5 V. It has a capstan envelope with a moulded cap. All leads are isolated from the stud.

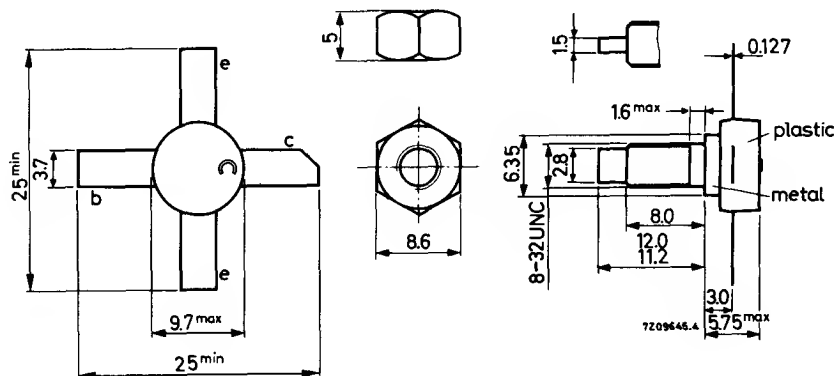
QUICK REFERENCE DATA

R.F. performance up to $T_{mb} = 25^{\circ}\text{C}$ in an unneutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{Z}_i (Ω)	\bar{Y}_L (mA/V)
c.w.	13.5	470	< 8	20	< 2.28	> 4	> 65	$1.1 + j4.9$	$190 - j45$
c.w.	12.5	470	< 6.8	17	< 2.09	> 4	> 65		

MECHANICAL DATA

Dimensions in mm



Torque on nut: min. 7.5 kg cm
(0.75 Newton metres)
max. 8.5 kg cm
(0.85 Newton metres)

Diameter of clearance hole in heatsink: max.
4.17 mm.

Mounting hole to have no burrs at either end.
De-burring must leave surface flat; do not
chamfer or countersink either end of hole.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

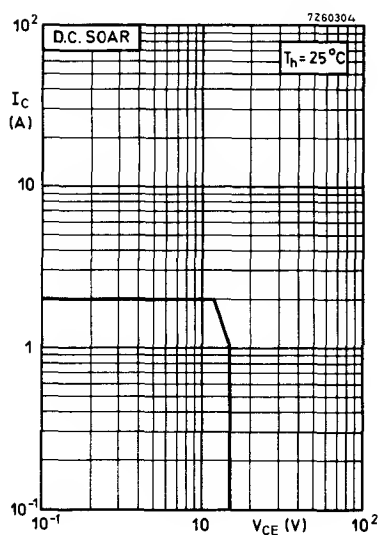
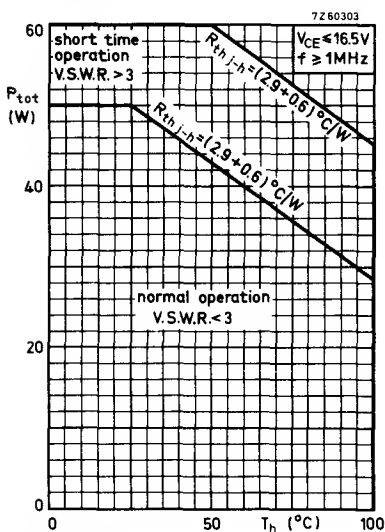
Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V

Currents

Collector current (average)	$I_{C(AV)}$	max.	3.5	A
Collector current (peak value) $f > 1$ MHz	I_{CM}	max.	10	A

Power dissipation

Total power dissipation up to $T_h = 25^\circ\text{C}$ $f > 1$ MHz	P_{tot}	max.	50	W
---	-----------	------	----	---



Temperature

Storage temperature	T_{stg}	-30 to +200	$^\circ\text{C}$
Operating junction temperature	T_j	max. 200	$^\circ\text{C}$

THERMAL RESISTANCE

From junction to mounting base	$R_{th j-mb}$	=	2.9	$^\circ\text{C/W}$
From mounting base to heatsink	$R_{th mb-h}$	=	0.6	$^\circ\text{C/W}$

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

Breakdown voltages

Collector-base voltage open emitter, $I_C = 25\text{ mA}$	$V_{(BR)CBO}$	>	36	V
Collector-emitter voltage open base, $I_C = 25\text{ mA}$	$V_{(BR)CEO}$	>	18	V
Emitter-base voltage open collector; $I_E = 10\text{ mA}$	$V_{(BR)EBO}$	>	4	V

Transient energy

$L = 25\text{ mH}$; $f = 50\text{ Hz}$

open base	E	>	3.1	mWs
$-V_{BE} = 1.5\text{ V}$; $R_{BE} = 33\ \Omega$	E	>	3.1	mWs

D.C. current gain

$I_C = 1\text{ A}$; $V_{CE} = 5\text{ V}$	h_{FE}	>	10
		typ.	30

Transition frequency

$I_C = 2\text{ A}$; $V_{CE} = 10\text{ V}$	f_T	typ.	1.0	GHz
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Collector capacitance at $f = 1\text{ MHz}$

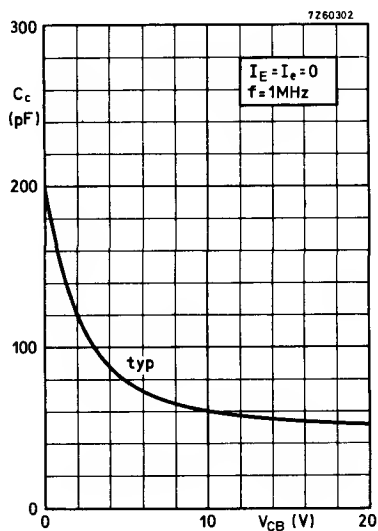
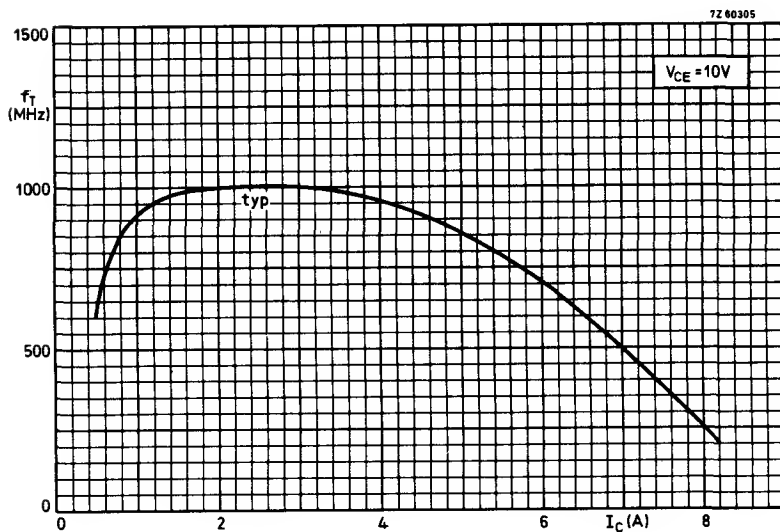
$I_E = I_e = 0$; $V_{CB} = 15\text{ V}$	C_c	typ.	55	pF
		<	70	pF

Feedback capacitance

$I_C = 100\text{ mA}$; $V_{CE} = 15\text{ V}$	$-C_{re}$	typ.	32	pF
--	-----------	------	----	----

Collector-stud capacitance

	C_{cs}	typ.	2	pF
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N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

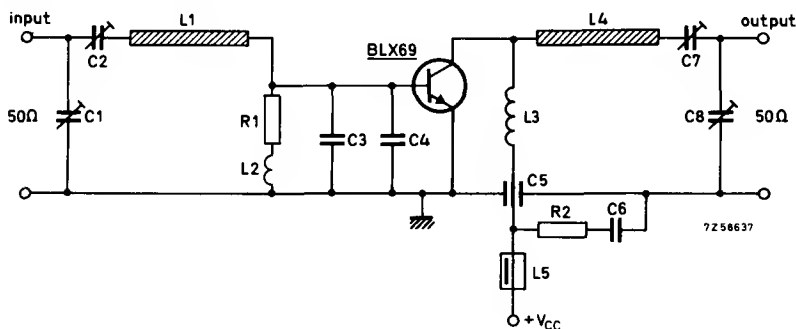
APPLICATION INFORMATION

R. F. performance in c. w. operation (unneutralised common-emitter class B circuit)

T_{mb} up to 25 °C

f (MHz)	V _{CC} (V)	P _S (W)	P _L (W)	I _C (A)	G _p (dB)	η (%)	\bar{Z}_i (Ω)	\bar{Y}_L (mA/V)
470	13.5	< 8	20	< 2.28	> 4	> 65	1.1 + j4.9	190-j45
470	12.5	< 6.8	17	< 2.09	> 4	> 65		
175	12.5	typ. 1.35	17	typ. 2.3	typ. 11	typ. 60	1.5 + j0.6	170-j57

Test circuit for 470 MHz:



List of components:

C1=C2=C7=C8=1.8 to 9.0 pF film dielectric trimmer

C3=C4= 15 pF chip capacitor

C5= 100 pF feed through capacitor

C6= 33 nF polyester capacitor

R1= 1 Ω

R2= 10 Ω

L1= strip-line (41.1 mm x 5.0 mm)

L2= 13 turns closely wound enamelled Cu wire (0.5 mm); int. diam. 4.0 mm (0.32 μ H)

L3= 2 turns Cu wire (1 mm); winding pitch 1.5 mm; int. diam. 4 mm; leads 2x5 mm

L4= strip-line (52.7 mm x 5.0 mm)

L5= ferroxcube choke coil. Z (at f = 250 MHz) = 400 Ω \pm 20 %

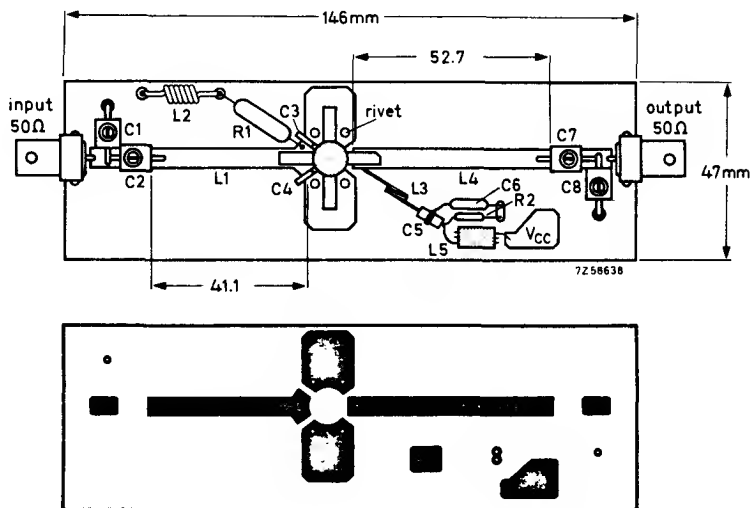
L1 and L4 are strip lines on a double Cu clad print plate with teflon fibre glass dielectric

(ϵ_r = 2.74); thickness 1.45 mm

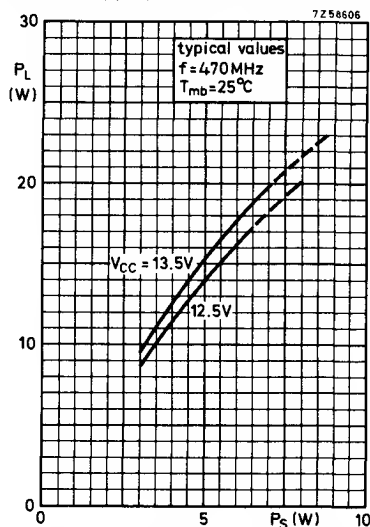
Component lay-out for 470 MHz: see page 6

APPLICATION INFORMATION (continued)

Component lay-out and printed circuit board for 470 MHz test circuit.



The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.



The issue of the information contained in this publication does not imply any authority or licence for the utilisation of any patented feature.

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they **MUST NOT** be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
2, NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.

N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX91

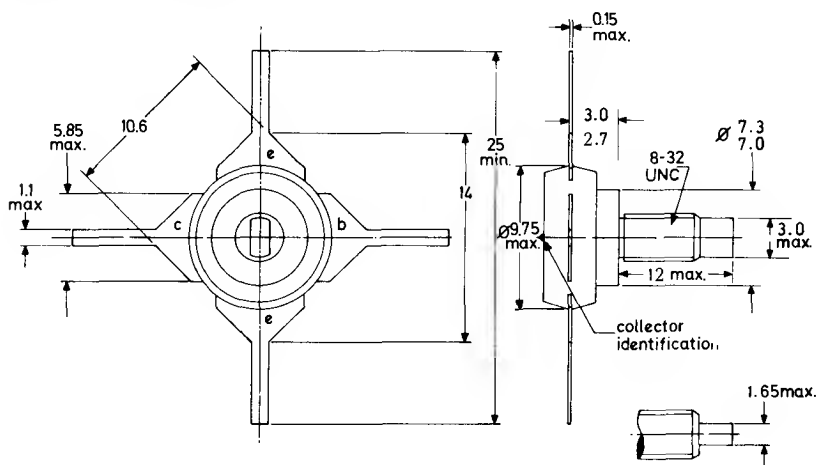
TENTATIVE DATA

Silicon n-p-n transistor designed for u.h.f. operation in class A, B or C with frequencies up to 1GHz. The device is mounted in a plastic, capstan, strip-line encapsulation.

With a supply voltage of 28V and a signal frequency of 470MHz, the BLX91 will produce 1.0W output into a 50Ω load.

QUICK REFERENCE DATA						
V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
28	470	0.08	1.0 min.	50 min.	25	Un-neutralised common-emitter class B
28	470	0.08	1.45 typ.	60 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

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RATINGS

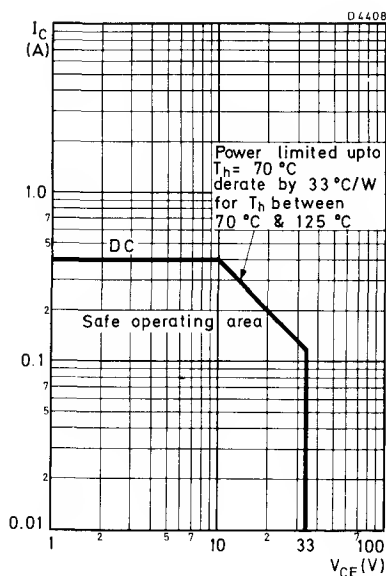
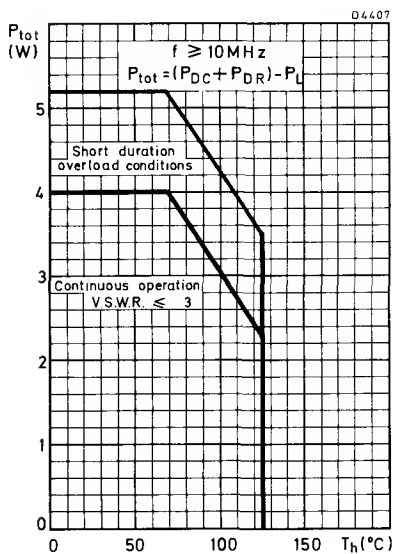
Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	65	V
V_{CESM} max. ($R_{BE} = 0$)	65	V
V_{CEO} max.	33	V
V_{EBO} max.	4.0	V
I_C max.	400	mA
I_{CM} max. ($f \geq 10\text{MHz}$)	800	mA
P_{tot} max. ($f \geq 10\text{MHz}$, $T_h \leq 70^\circ\text{C}$) see also graphs below	4.0	W

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
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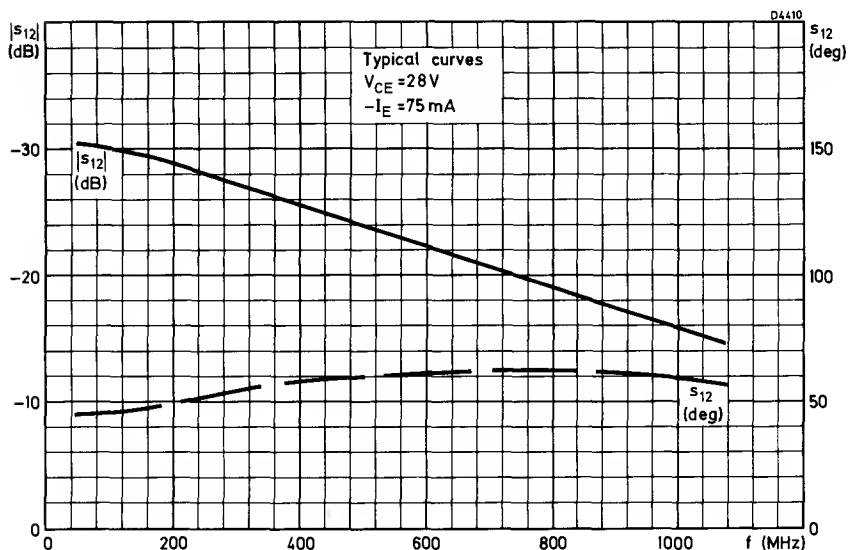
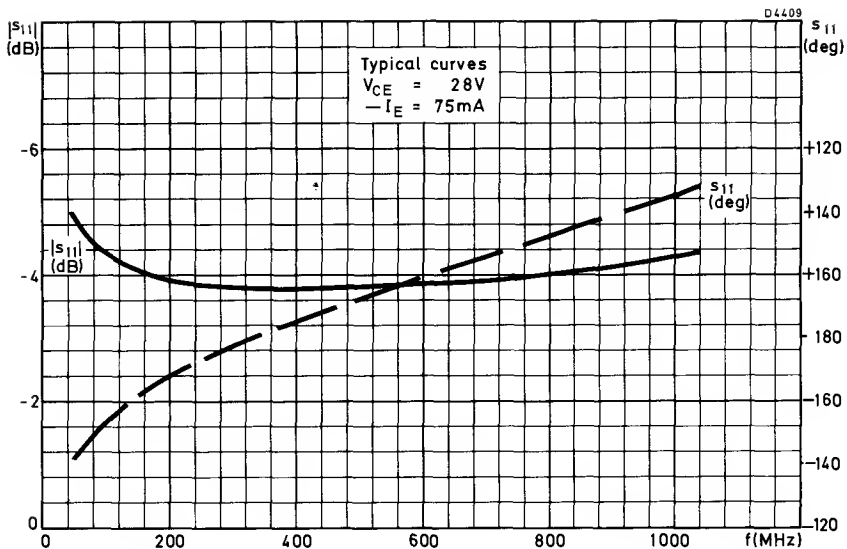
N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX91

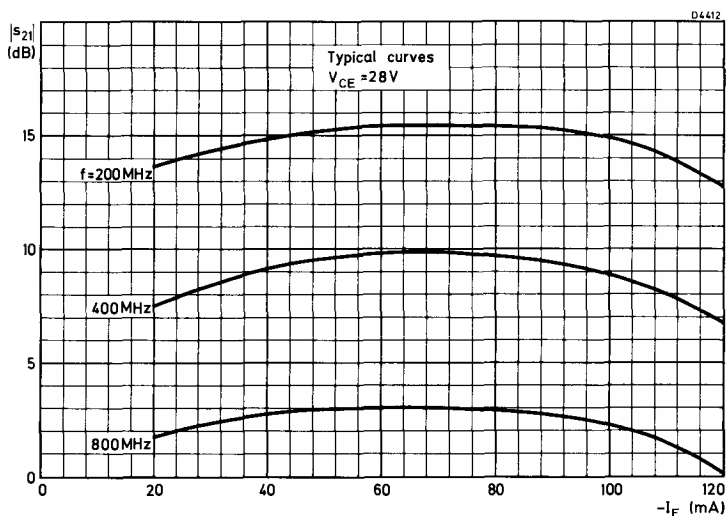
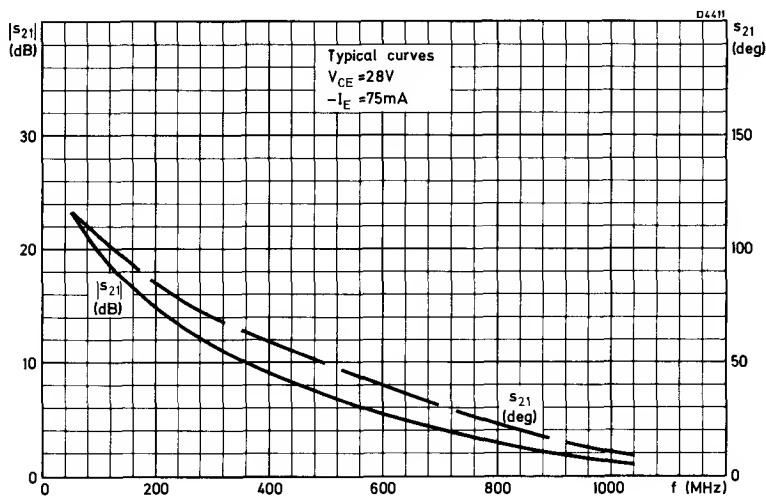
ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	65	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 25\text{mA}$	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	10	35	-	
*f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1200	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	3.5	-	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	-	11	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

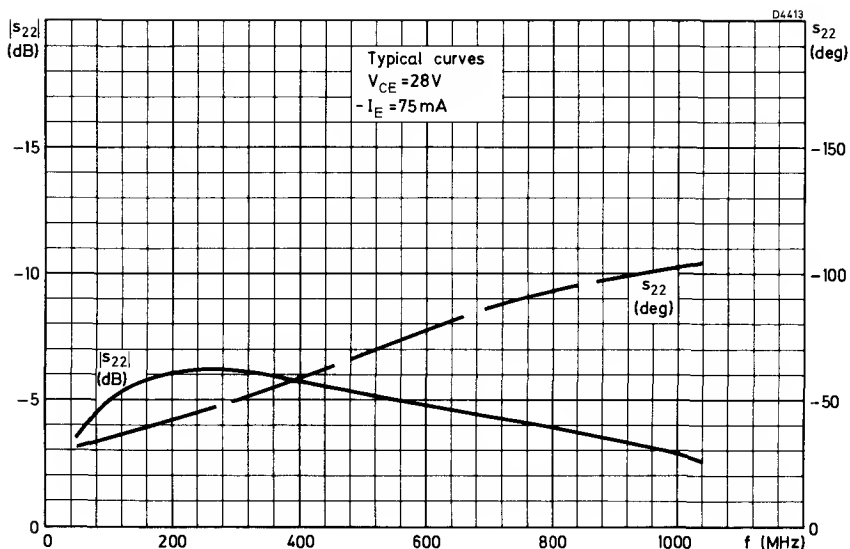
* Derived from the 's' parameters measured at $f = 500\text{MHz}$, $T_{amb} = 25^{\circ}\text{C}$



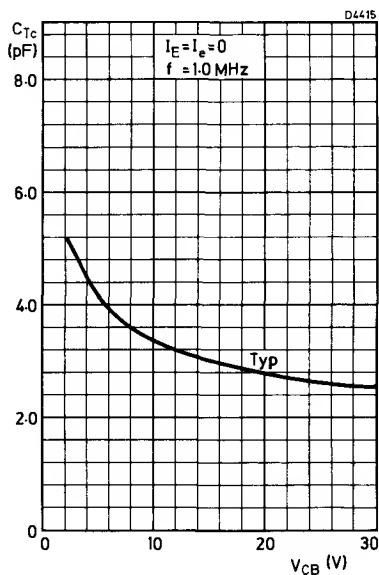
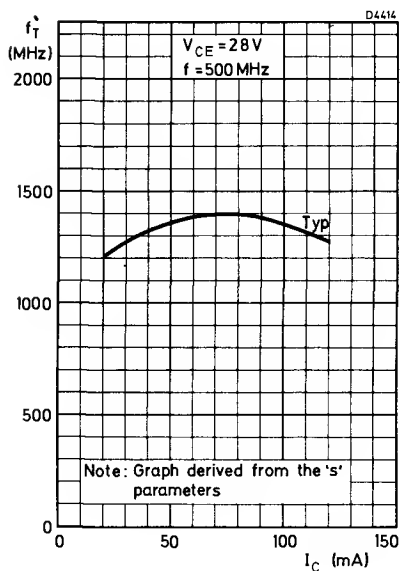
TYPICAL VARIATION OF INPUT REFLECTION COEFFICIENT
 AND FEEDBACK COEFFICIENT WITH FREQUENCY



TYPICAL VARIATION OF FORWARD TRANSFER COEFFICIENT
WITH FREQUENCY AND EMITTER CURRENT



TYPICAL VARIATION OF OUTPUT REFLECTION COEFFICIENT
WITH FREQUENCY



N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX91

APPLICATION INFORMATION

R. F. Performance in c.w. operation ($T_h = 25^{\circ}\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50 Ω (W)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mmho)
24	470	0.05	0.85 typ.	53 typ.	-	-
28	470	0.08	1.0 min.	50 min.	-	-
28	470	0.08	1.45 typ.	60 typ.	1.4 + j1.6	3.7 - j22
28	1000	0.40	1.4 typ.	50 typ.	-	-

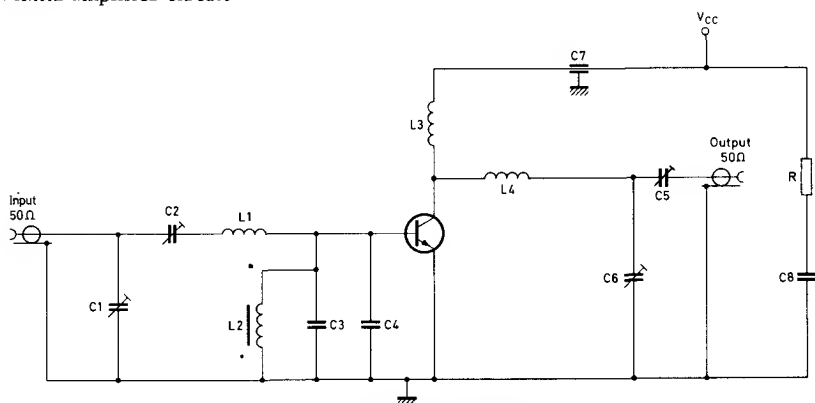
At $P_L = 1.0\text{W}$ and $V_{CC} = 28\text{V}$, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $2\text{mW}/^{\circ}\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$$V_{CC} = 28\text{V} \quad f = 470\text{MHz} \quad T_h = 90^{\circ}\text{C}$$

$$P_L = 1.2\text{W} \quad \text{V.S.W.R.} = 50:1 \text{ at any phase}$$

470MHz amplifier circuit



D4457

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APPLICATION INFORMATION (contd.)

Component values for 470MHz amplifier circuit.

C1 = C2 = C5 = 1.8 to 18pF film-dielectric trimmer capacitors.

C3 = C4 = 18pF disc ceramic capacitors.

C6 = 1.0 to 9.0pF film-dielectric trimmer capacitors.

C7 = 1000pF feed-through capacitor.

C8 = 0.1μF ceramic capacitor.

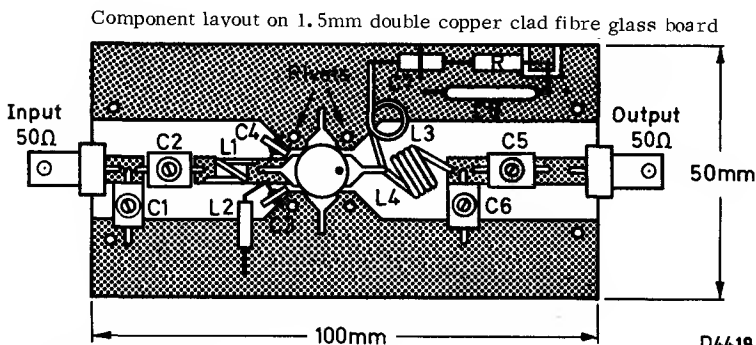
L1 = 1 turn of 1.2mm Cu wire, internal diameter 5mm, lead length = 2mm.

L2 = 0.47μH choke.

L3 = 5 turns of 0.5mm Cu wire, internal diameter 4mm, lead length = 5mm, close wound.

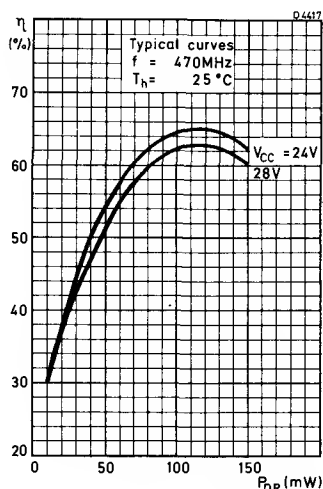
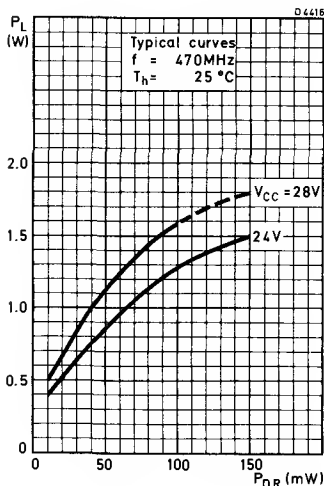
L4 = 4 turns of 1.2mm Cu wire, internal diameter 6.5mm, lead length = 4mm, close wound.

R = 10Ω carbon.



Shaded area copper

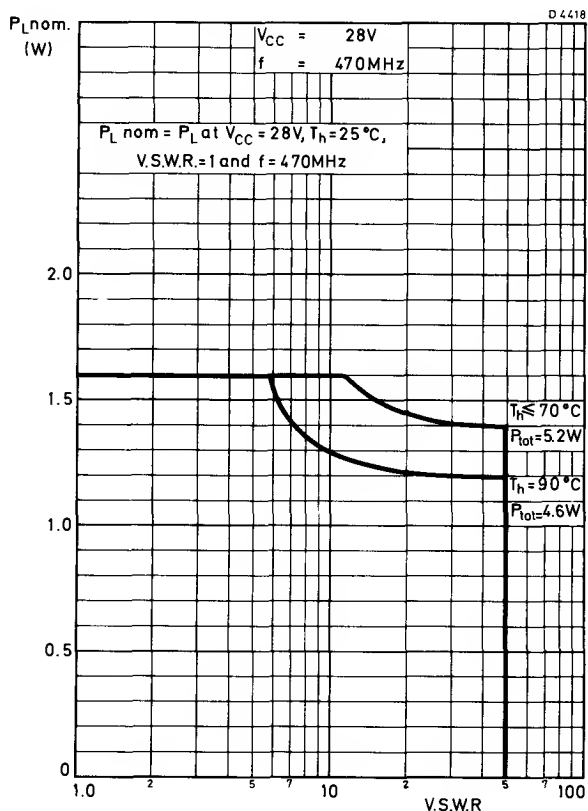
Underside area completely copper clad



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY
WITH DRIVE POWER

Mullard

APPLICATION INFORMATION (contd.)



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The above graph has been derived from an evaluation of the performance of transistors matched up to 1.6 watts load power in the test amplifier on Page 7 and subsequently subjected to various mismatch conditions at 28V with V.S.W.R. up to 50:1 and elevated heatsink temperatures. This indicates a restriction to the load power matched under nominal conditions in the recommended test configuration.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR
U.H.F. TRANSISTOR

BLX92

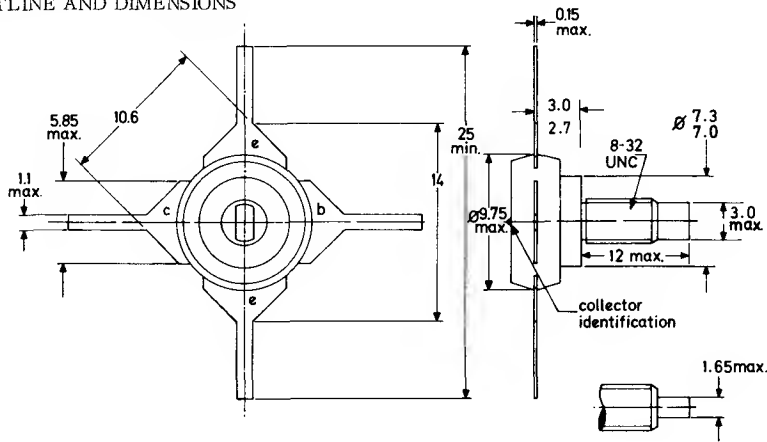
TENTATIVE DATA

Silicon n-p-n transistor designed for u.h.f. operation in class A, B or C with frequencies up to 1GHz. The device is mounted in a plastic, capstan, strip-line encapsulation.

With a supply voltage of 28V and a signal frequency of 470MHz, the BLX92 will produce 2.5W output into a 50Ω load.

QUICK REFERENCE DATA						
V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
24	470	0.2	2.4 typ.	70 typ.	25	Un-neutralised common-emitter class B
28	470	0.2	2.5 min.	60 min.	25	
28	470	0.2	3.0 typ.	66 typ.	25	
28	1000	0.7	2.5 typ.	50 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

D 3370

RATINGS

Limiting values of operation according to the absolute maximum system.

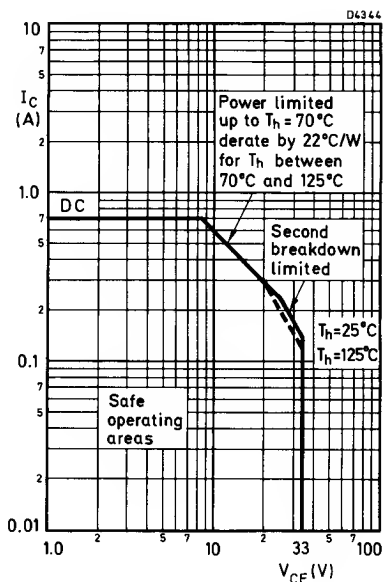
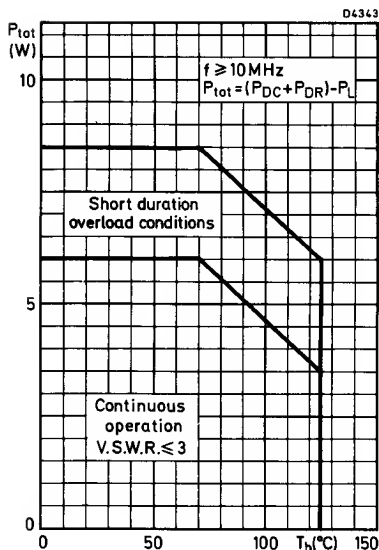
Electrical

V_{CBOM} max.	65	V
V_{CESM} max. ($R_{BE} = 0$)	65	V
V_{CEO} max.	33	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. ($f \geq 10\text{MHz}$)	2.0	A
P_{tot} max. ($f \geq 10\text{MHz}$, $T_h \leq 70^\circ\text{C}$)	6.0	W

See also graphs below

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
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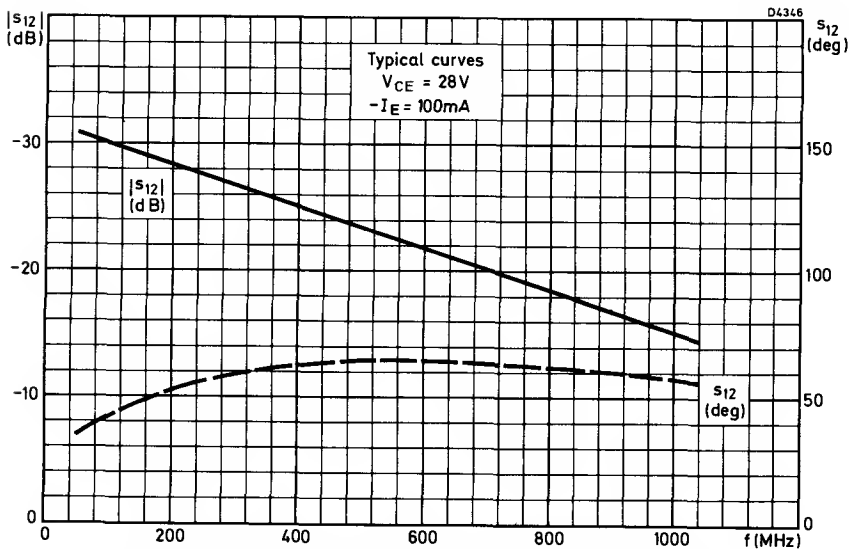
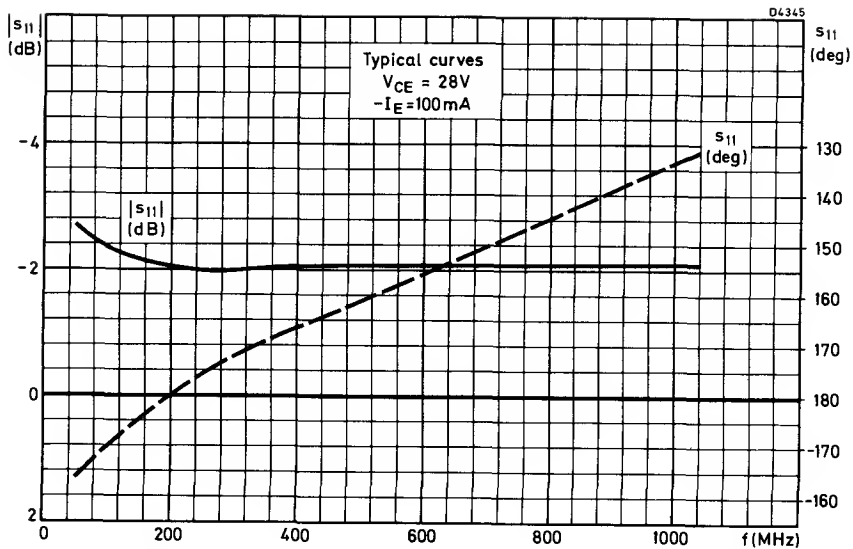
N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX92

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	65	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 25\text{mA}$	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100\text{mA}$, $I_B = 20\text{mA}$	-	0.17	-	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	10	40	-	
$*f_T$	Transition frequency $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1200	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	6.5	-	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	-	25	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

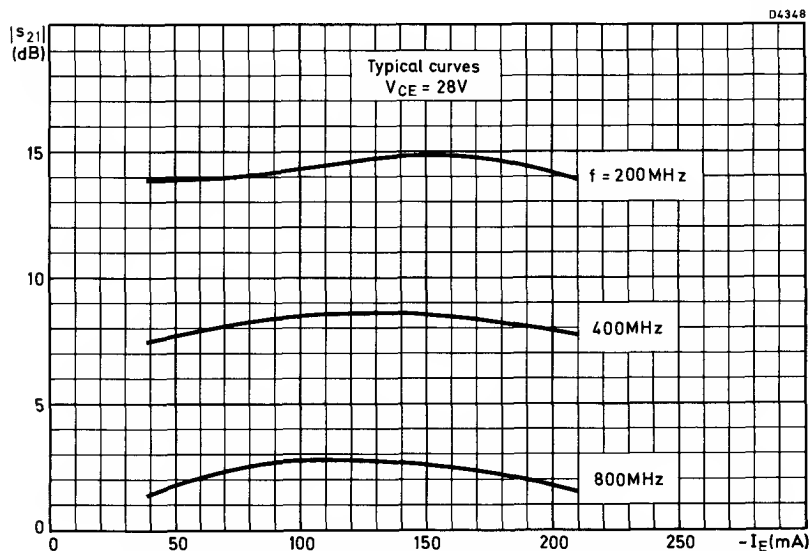
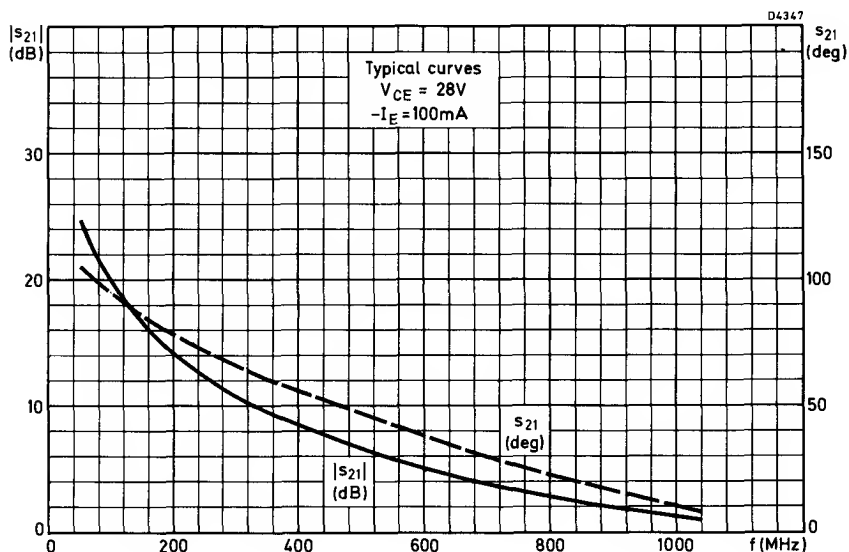
*Derived from the 's' parameters measured at $f = 500\text{MHz}$, $T_{amb} = 25^{\circ}\text{C}$



TYPICAL VARIATION OF INPUT REFLECTION COEFFICIENT AND
 FEEDBACK COEFFICIENT WITH FREQUENCY

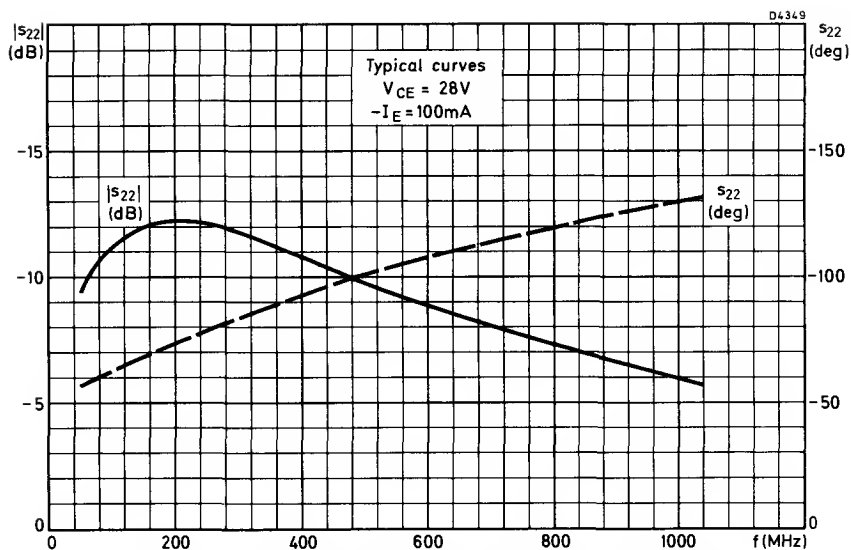
N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX92

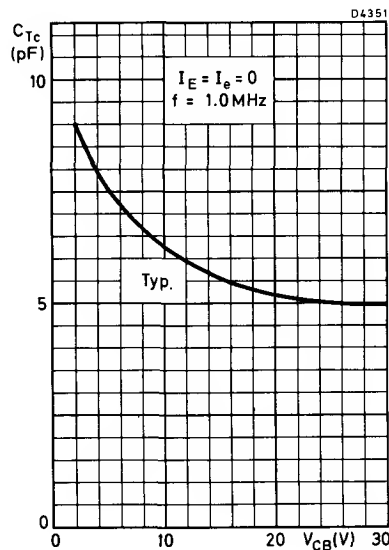
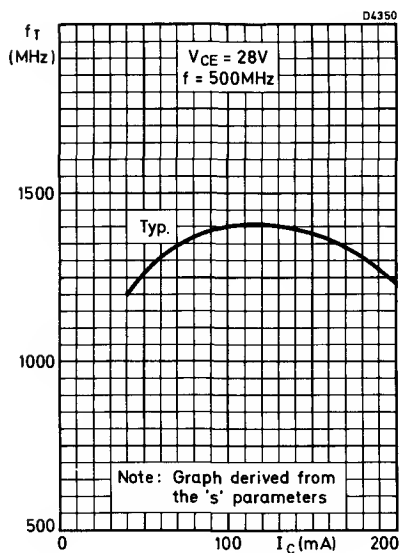


TYPICAL VARIATION OF FORWARD TRANSFER COEFFICIENT
WITH FREQUENCY AND EMITTER CURRENT

Mullard



TYPICAL VARIATION OF OUTPUT REFLECTION COEFFICIENT
 WITH FREQUENCY



N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX92

APPLICATION INFORMATION

R. F. Performance in c.w. operation ($T_h = 25^\circ\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mmho)
24	470	0.2	2.5 typ.	70 typ.	-	-
28	470	0.2	2.5 min.	60 min.	-	-
28	470	0.2	3.0 typ.	66 typ.	$1.6 + j3.4$	$7.7 - j31$
28	1000	0.7	2.5 typ.	50 typ.	-	-

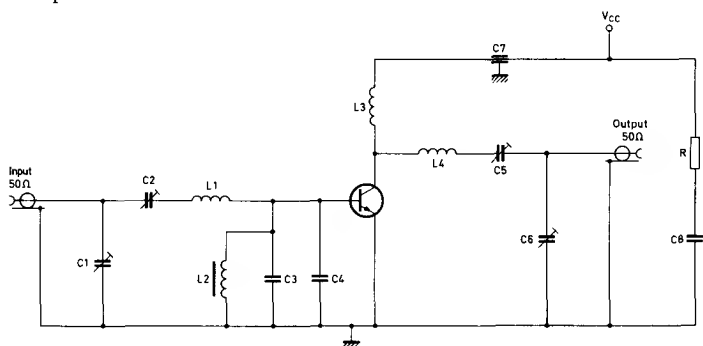
At $P_L = 2.5\text{W}$ and $V_{CC} = 28\text{V}$, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $5\text{mW}/^\circ\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$$V_{CC} = 28\text{V} \quad f = 470\text{MHz} \quad T_h = 90^\circ\text{C}$$

$$P_L = 2.5\text{W} \quad \text{V.S.W.R.} = 50:1 \text{ at any phase}$$

470MHz amplifier circuit



D4341

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APPLICATION INFORMATION (contd.)

Component values for 470MHz amplifier circuit.

C1 = C2 = 1.8 to 18pF film-dielectric trimmer capacitors.

C3 = C4 = 18pF disc ceramic capacitors.

C5 = C6 = 1.0 to 9.0pF film-dielectric trimmer capacitors.

C7 = 1000pF feed-through capacitor.

C8 = 0.1μF ceramic capacitor.

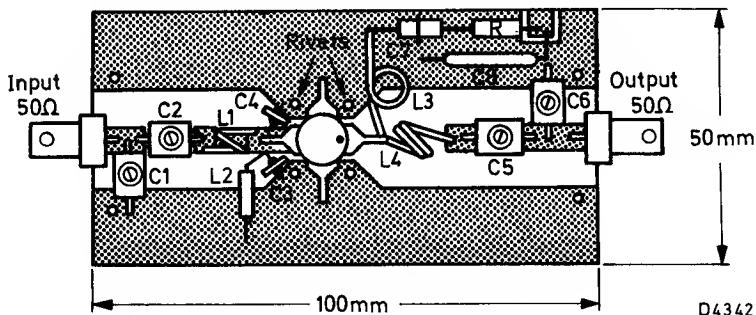
L1 = 1 turn of 1.2mm Cu wire, internal diameter 5mm, lead length = 2mm.

L2 = 0.47μH choke.

L3 = 3 turns of 0.5mm Cu wire, internal diameter 4mm, lead length = 5mm

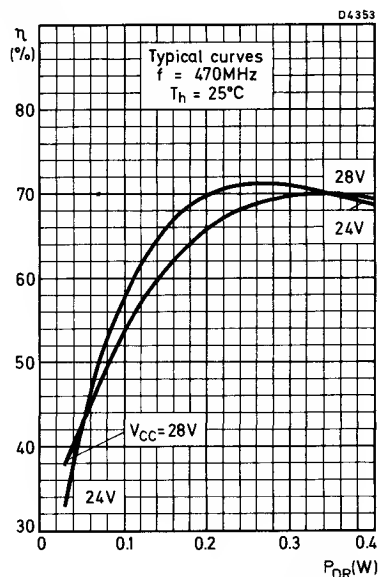
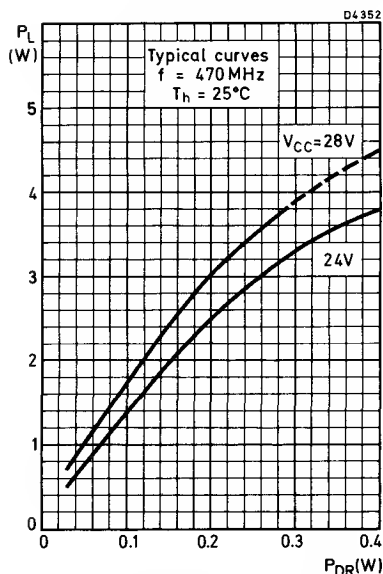
L4 = 2 turns of 1.2mm Cu wire, internal diameter 6.5mm, lead length = 4mm

Component layout on 1.5mm double copper clad fibre glass board



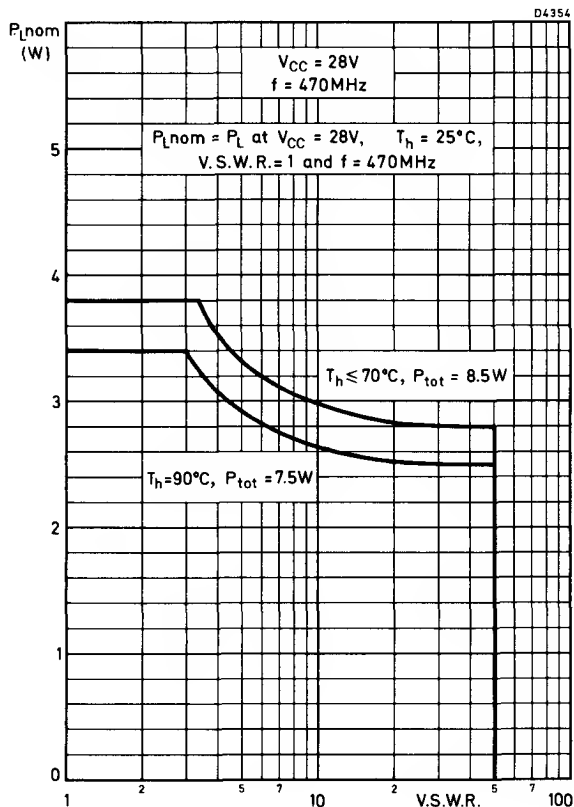
Shaded area copper

Underside area completely copper clad



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

APPLICATION INFORMATION (contd.)



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The above graph has been derived from an evaluation of the performance of transistors matched up to 3.8 watts load power in the test amplifier on Page 7 and subsequently subjected to various mismatch conditions at 28V with V.S.W.R. up to 50:1 and elevated heatsink temperatures. This indicates a restriction to the load power matched under nominal conditions in the recommended test configuration.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

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N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX93

TENTATIVE DATA

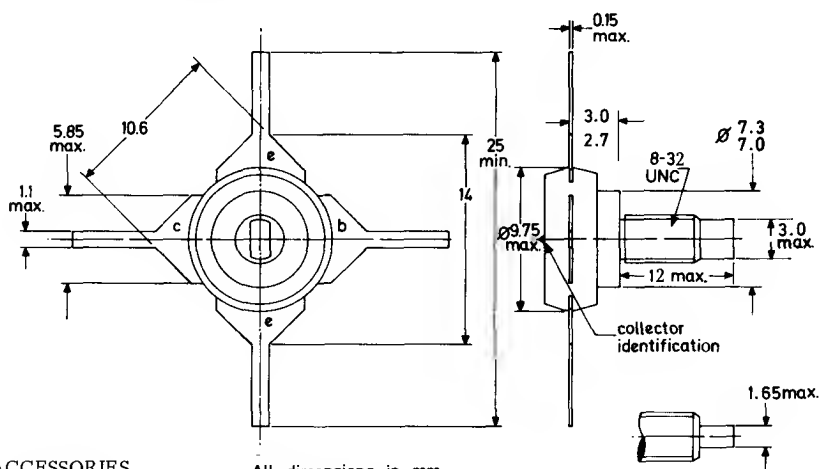
Silicon n-p-n transistor designed for u.h.f. operation in class A, B or C with frequencies up to 1GHz. The device is mounted in a plastic, capstan, strip-line encapsulation.

With a supply voltage of 28V and a signal frequency of 470MHz, the BLX93 will produce 7.0W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
24	470	1.0	7.0 typ.	70 typ.	25	Un-neutralised common-emitter class B
28	470	1.0	7.0 min.	60 min.	25	
28	470	1.0	8.0 typ.	75 typ.	25	
28	1000	1.5	5.0 typ.	45 typ.	25	

OUTLINE AND DIMENSIONS



ACCESSORIES

All dimensions in mm

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

D3370

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RATINGS

Limiting values of operation according to the absolute maximum system.

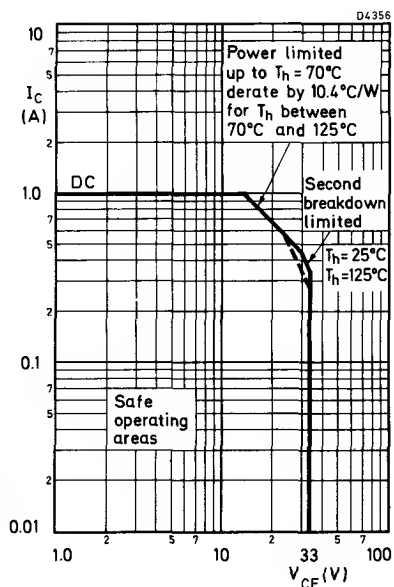
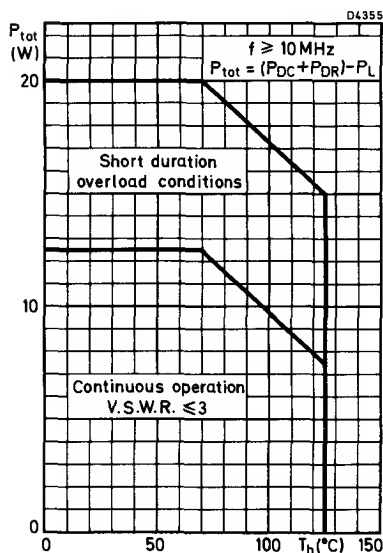
Electrical

V_{CBOM} max.	65	V
V_{CESM} max. ($R_{BE} = 0$)	65	V
V_{CEO} max.	33	V
V_{EBO} max.	4.0	V
I_C max.	1.0	A
I_{CM} max. ($f \geq 10\text{MHz}$)	3.0	A
P_{tot} max. ($f \geq 10\text{MHz}$, $T_h \leq 70^\circ\text{C}$)	12.5	W

See also graphs below

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
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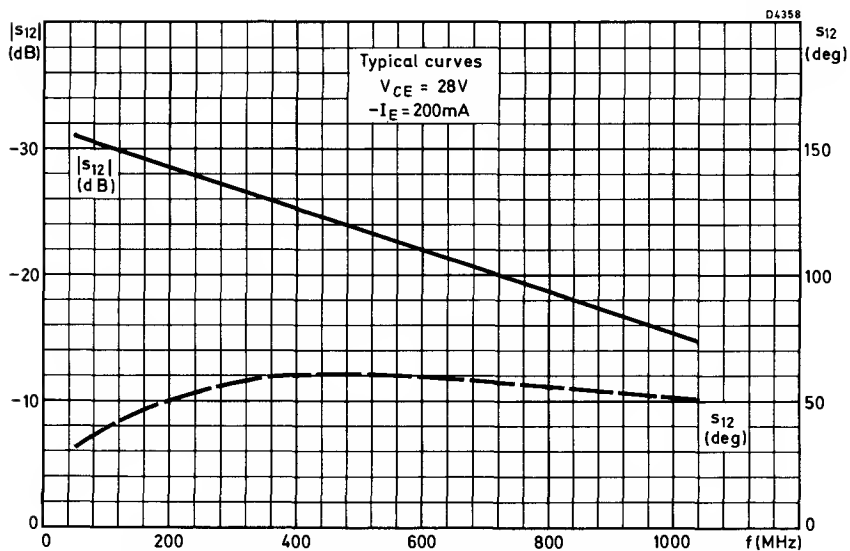
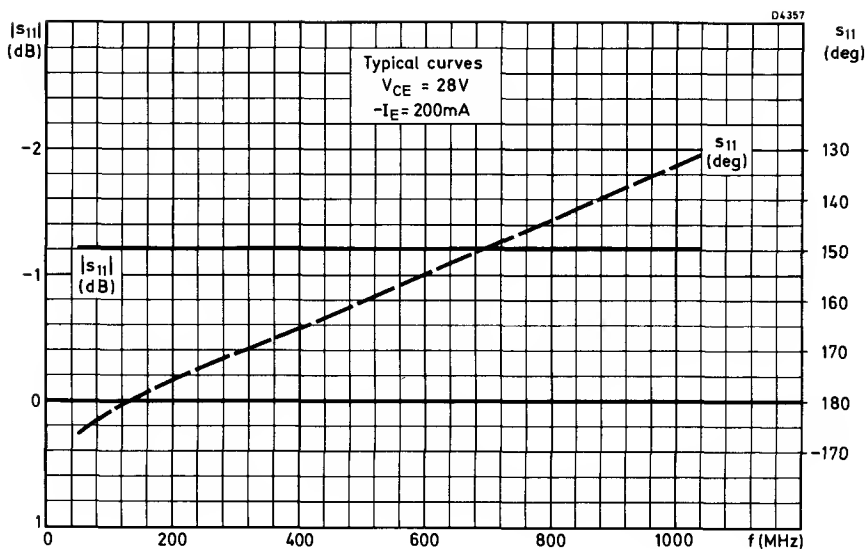
N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX93

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	65	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 25\text{mA}$	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	10	35	-	
*f_T	Transition frequency $I_C = 200\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1200	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	14	-	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	-	60	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

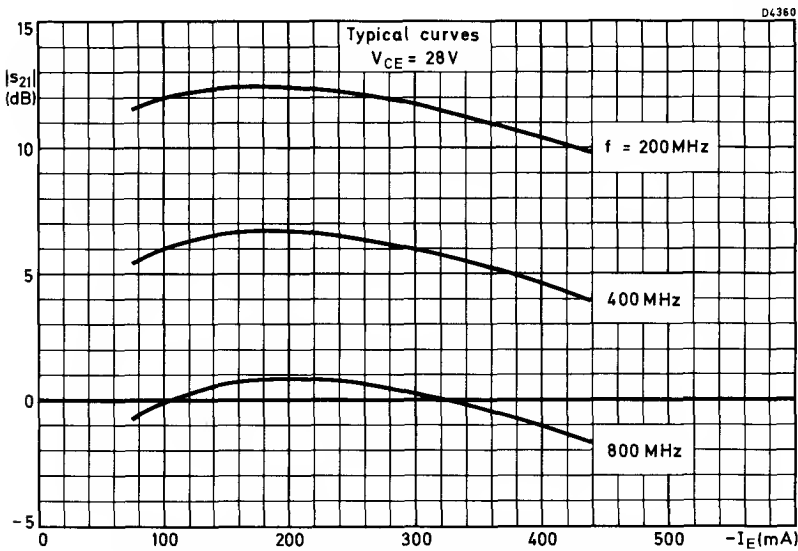
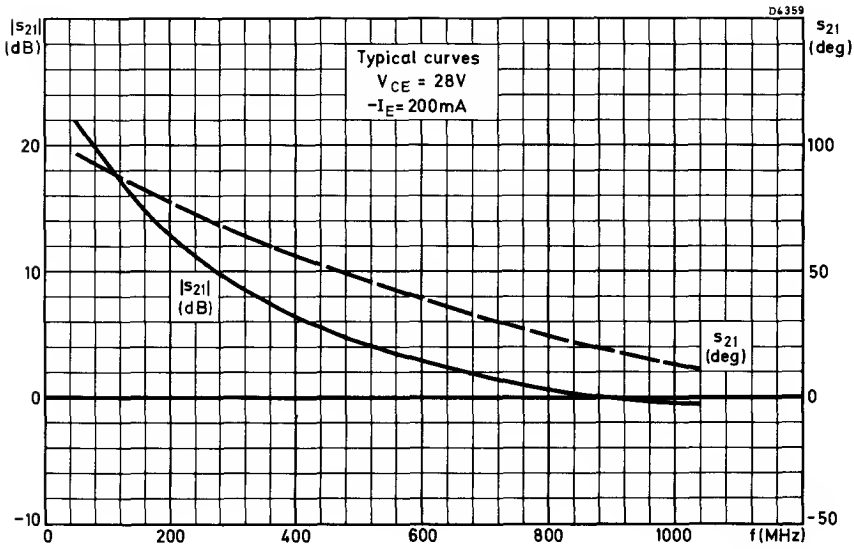
*Derived from the 's' parameters measured at $f = 500\text{MHz}$, $T_{amb} = 25^{\circ}\text{C}$



TYPICAL VARIATION OF INPUT REFLECTION COEFFICIENT AND
 FEEDBACK COEFFICIENT WITH FREQUENCY

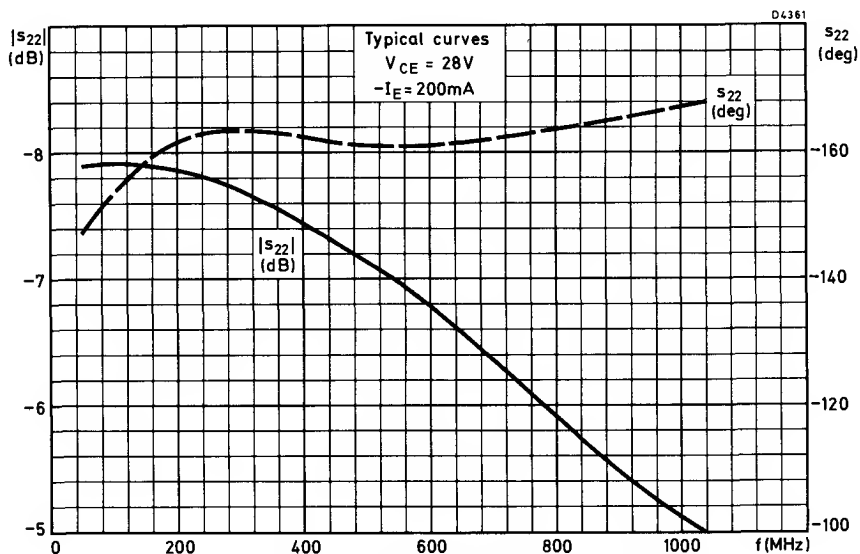
N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX93

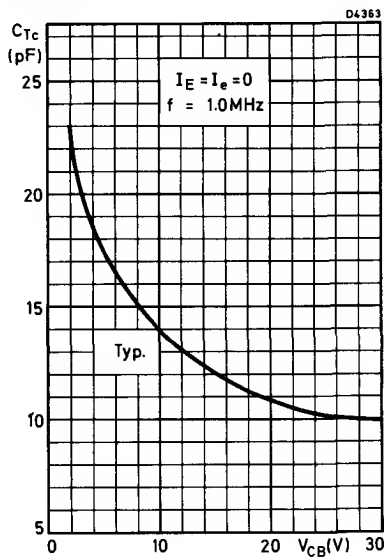
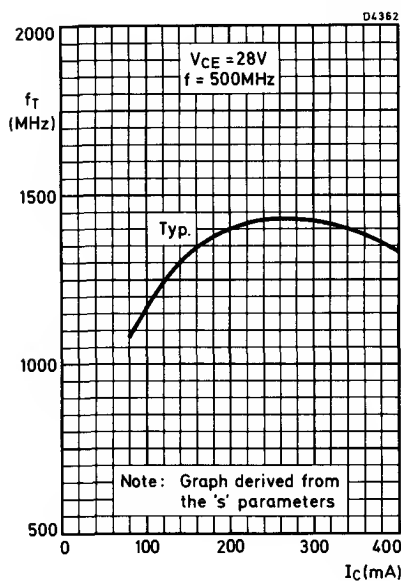


TYPICAL VARIATION OF FORWARD TRANSFER COEFFICIENT
WITH FREQUENCY AND EMITTER CURRENT

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TYPICAL VARIATION OF OUTPUT REFLECTION COEFFICIENT
WITH FREQUENCY



N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX93

APPLICATION INFORMATION

R. F. Performance in c. w. operation ($T_h = 25^{\circ}\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	\bar{z}_1 (Ω)	\bar{Y}_L (mmho)
24	470	1.0	7.0 typ.	70 typ.	-	-
28	470	1.0	7.0 min.	60 min.	-	-
28	470	1.0	8.0 typ.	75 typ.	$1.6 + j5.5$	$20 - j40$
28	1000	1.5	5.0 typ.	45 typ.	-	-

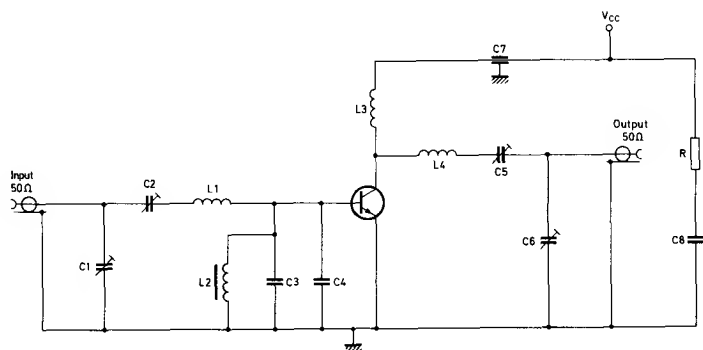
At $P_L = 7.0\text{W}$ and $V_{CC} = 28\text{V}$, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $10\text{mW}/^{\circ}\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$$V_{CC} = 28\text{V} \quad f = 470\text{MHz} \quad T_h = 90^{\circ}\text{C}$$

$$P_L = 7.0\text{W} \quad \text{V.S.W.R.} = 50:1 \text{ at any phase}$$

470MHz amplifier circuit



04341

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APPLICATION INFORMATION (contd.)

Component values for 470MHz amplifier circuit.

C1 = C2 = 1.8 to 18pF film-dielectric trimmer capacitors.

C3 = C4 = 18pF disc ceramic capacitors.

C5 = C6 = 1.0 to 9.0pF film-dielectric trimmer capacitors.

C7 = 1000pF feed-through capacitor.

C8 = 0.1μF ceramic capacitor.

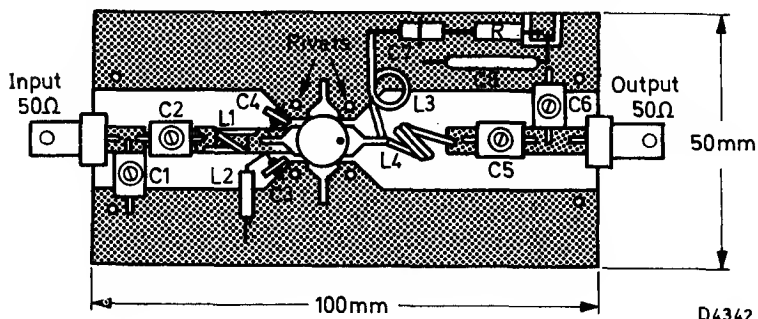
L1 = 1 turn of 1.2mm Cu wire, internal diameter 5mm, lead length = 2mm.

L2 = 0.47μH choke.

L3 = 3 turns of 0.5mm Cu wire, internal diameter 4mm, lead length = 5mm

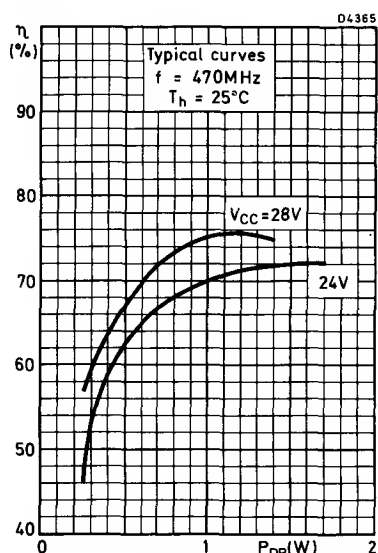
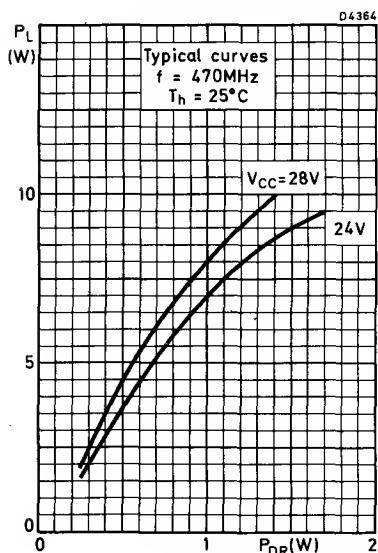
L4 = 2 turns of 1.2mm Cu wire, internal diameter 6.5mm, lead length = 4mm

Component layout on 1.5mm double copper clad fibre glass board



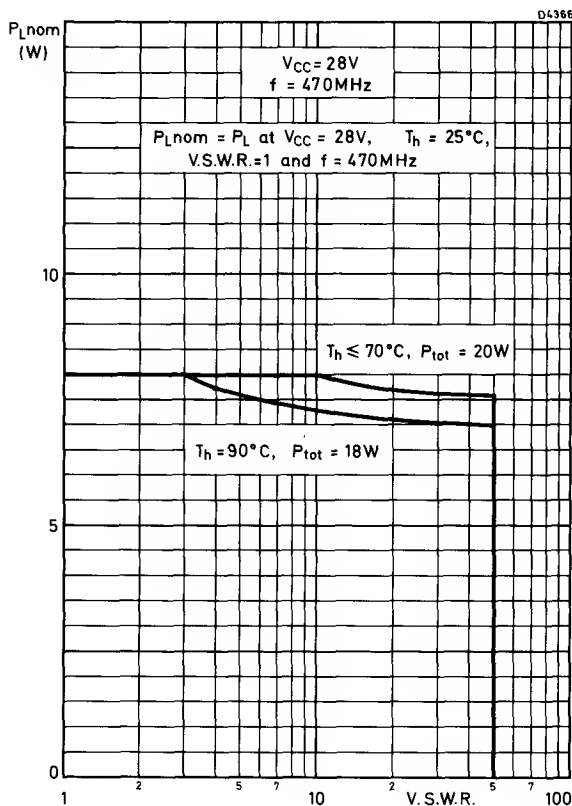
Shaded area copper

Underside area completely copper clad



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

APPLICATION INFORMATION (contd.)



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The above graph has been derived from an evaluation of the performance of transistors matched up to 8 watts load power in the test amplifier on Page 7 and subsequently subjected to various mismatch conditions at 28V with V.S.W.R. up to 50:1 and elevated heatsink temperatures. This indicates a restriction to the load power matched under nominal conditions in the recommended test configuration.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

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N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX94

N-P-N silicon planar epitaxial transistor intended for transmitting applications in class A, B or C with a supply voltage up to 28V.

The transistor is resistance stabilised and is tested under severe load mismatch conditions.

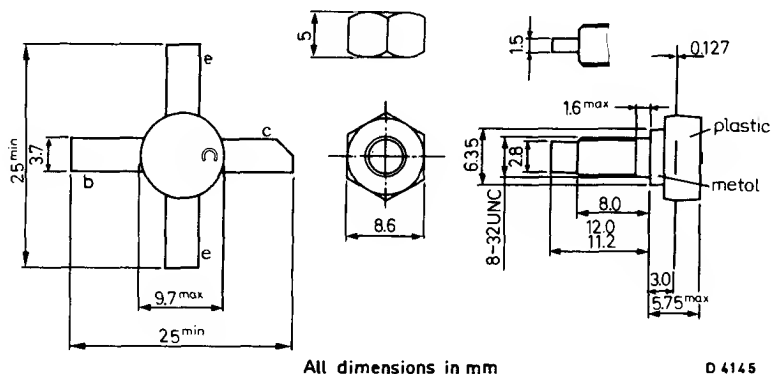
It has a 1/4" capstan envelope with a moulded cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R. F. performance at $T_{mb} \leq 25^{\circ}\text{C}$ in an un-neutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{z}_i (Ω)	\bar{y}_L (mA/V)
C. W.	28	470	<5	20	<1.3	>6	>55	$0.65 + j3.9$	62-j97

OUTLINE AND DIMENSIONS



Torque on nut: 7.5kg cm (0.75Nm) min.
8.5kg cm (0.85Nm) max.

Diameter of clearance hole in heatsink: 4.17mm max.

Note: Do not chamfer the edges of the mounting holes when removing burrs. When locking is required, an adhesive instead of a lock washer is preferred.

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

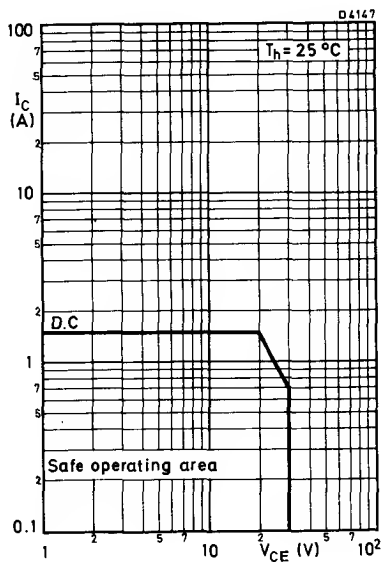
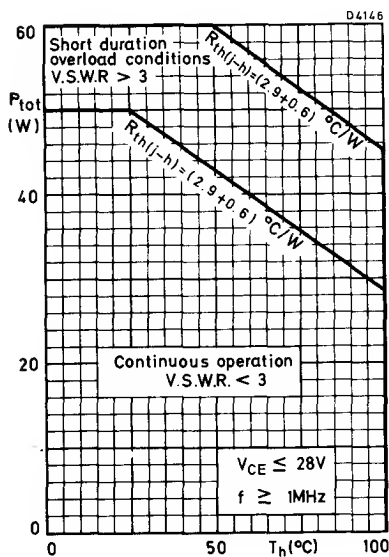
V_{CBOM} max.	65	V
V_{CEO} max.	33	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	2.0	A
I_{CM} max. ($f > 1.0\text{MHz}$)	6.0	A
P_{tot} max. ($T_h \leq 25^\circ\text{C}$, $f > 1.0\text{MHz}$)	50	W

Temperature

T_{stg}	-30 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$	2.9	$^\circ\text{C/W}$
$R_{th(mb-h)}$	0.6	$^\circ\text{C/W}$

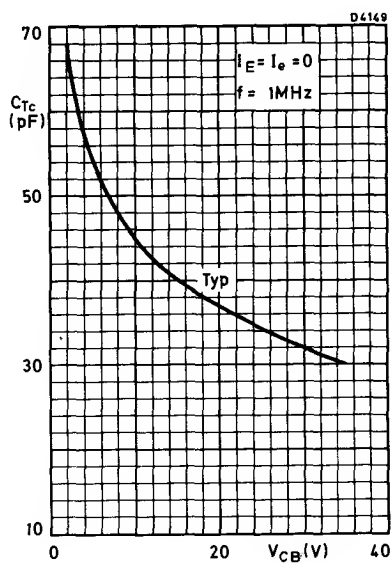
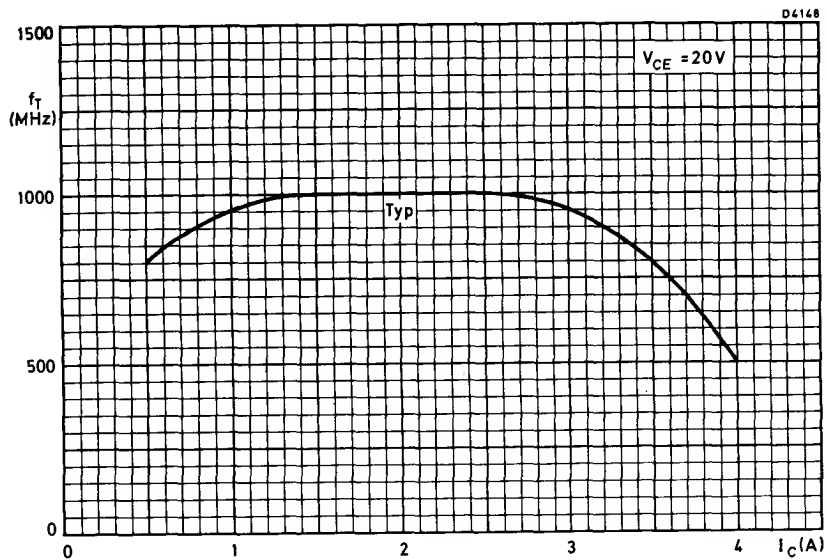


N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX94

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CEO}	Collector cut-off current $I_B = 0, V_{\text{CE}} = 28\text{V}$	-	-	10	mA
$V_{(\text{BR})\text{CBO}}$	Collector-base breakdown voltage open emitter $I_C = 25\text{mA}$	65	-	-	V
$V_{(\text{BR})\text{CEO}}$	Collector-emitter breakdown voltage, open base $I_C = 25\text{mA}$	33	-	-	V
$V_{(\text{BR})\text{EBO}}$	Emitter-base breakdown voltage open collector $I_E = 10\text{mA}$	4.0	-	-	V
E	Transient energy $L = 25\text{mH}, f = 50\text{Hz}$				
	open base	3.0	-	-	mWs
	$-V_{\text{BE}} = 1.5\text{V}, R_{\text{BE}} = 33\Omega$	3.0	-	-	mWs
h_{FE}	Static forward current transfer ratio $I_C = 1.0\text{A}, V_{\text{CE}} = 5.0\text{V}$	15	50	-	
f_{T}	Transition frequency $I_C = 2.0\text{A}, V_{\text{CE}} = 20\text{V}$	-	1.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_e = 0, V_{\text{CB}} = 30\text{V}, f = 1.0\text{MHz}$	-	32	50	pF
$-C_{\text{re}}$	Feedback capacitance $I_C = 100\text{mA}, V_{\text{CE}} = 30\text{V}, f = 1.0\text{MHz}$	-	18	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF



N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX94

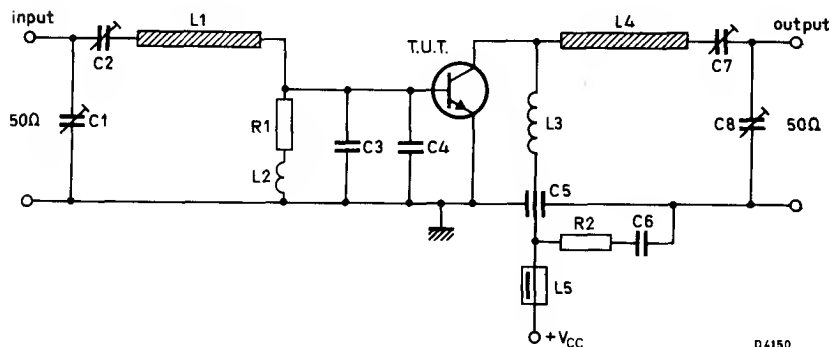
APPLICATION INFORMATION

R.F. performance in c.w. operation (un-neutralised common-emitter class B circuit)

$f = 470\text{MHz}$, $T_{mb} = 25^\circ\text{C}$

V_{CC} (V)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\overline{z}_i (Ω)	Y_L (mA/V)
28	<5	20	<1.3	>6	>55	$0.65 + j3.9$	$62 - j97$

Test circuit



Component values

$C1 = C2 = C8 = 2$ to 9pF film dielectric trimmer

$C3 = C4 = 15\text{pF}$ chip capacitor

$C5 = 100\text{pF}$ feed-through capacitor

$C6 = 33\text{nF}$ polyester capacitor

$C7 = 2$ to 18pF film dielectric trimmer

$R1 = 1\Omega$ carbon resistor

$R2 = 10\Omega$ carbon resistor

$L1 =$ strip line ($40.8 \times 5.0\text{mm}$)

$L2 = 13$ turns of closely wound enamelled copper wire (0.5mm), int. dia. 4.0mm

$L3 = 2$ turns of copper wire (1mm), winding pitch 1.5mm , int. dia. 4.0mm , leads $2 \times 5\text{mm}$

$L4 =$ strip line ($52.4 \times 5.0\text{mm}$)

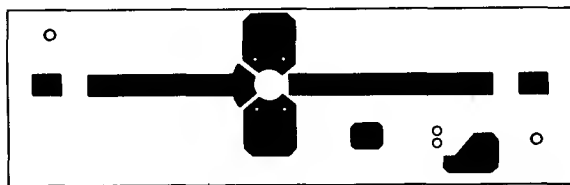
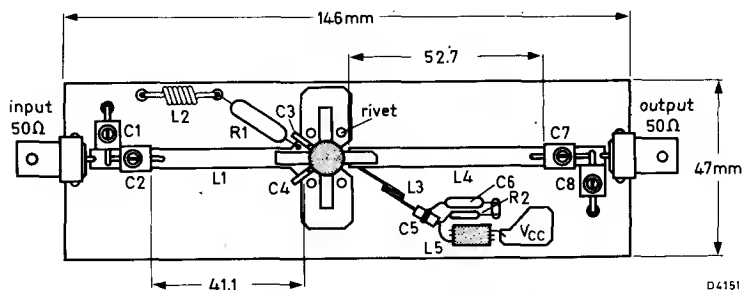
$L5 =$ ferroxcube choke coil, Z (at $f = 50\text{MHz}$) $= 750\Omega \pm 20\%$

$L1$ and $L4$ are strip lines on a double copper clad print plate with teflon fibre-glass dielectric ($\epsilon_r = 2.74$), thickness 1.45mm .

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APPLICATION INFORMATION (contd.)

Component layout and printed circuit board for 470MHz test circuit.

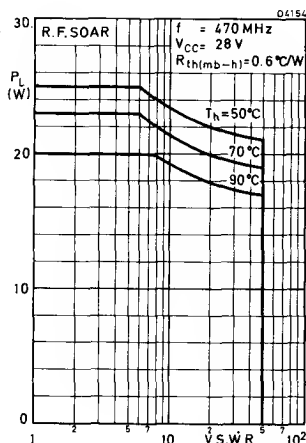
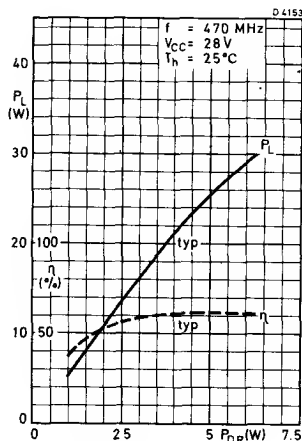


The circuit and the components are situated on one side of the teflon fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.

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N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX94



For high voltage operation, a stabilised power supply is generally used.

The graph shows the allowable output power under nominal conditions as a function of the V.S.W.R., with heat-sink temperature as parameter.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

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N-P-N SILICON V.H.F. POWER TRANSISTORS

BLY33 BLY34

TENTATIVE DATA

Silicon n-p-n high frequency medium power transistors primarily intended for class B operation in v.h.f. amplifiers. The collector is electrically connected to case.

QUICK REFERENCE DATA

	BLY33	BLY34	
V_{CES} max. (peak r.f. ≥ 1.0 MHz)	66	40	V
V_{CEO} max.	33	20	V
I_{CM} max. (peak r.f. ≥ 1.0 MHz)	1.5	1.5	A
P_{tot} max. ($T_{case} \leq 100^\circ\text{C}$)	2.0	2.0	W
T_j max.	150	150	$^\circ\text{C}$
f_T min. ($I_C = 0.2\text{A}$, $V_{CE} = 5.0\text{V}$, $f = 100\text{MHz}$)	250	250	MHz

Performance in a 175MHz common emitter amplifier:-

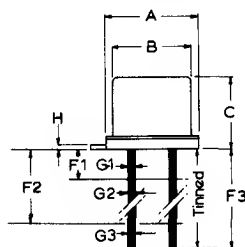
		Operation: a.m.	f.m.	
V_{CC}	Supply voltage	13.8	13.8	V
P_o	Output power	2.0	3.0	W
G_p	Typ. power gain	8.0	8.0	dB
η	Typ. efficiency	80	80	%

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B

J. E. D. E. C. TO-39



Millimetres

	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CES} max. (peak r.f. ≥ 1.0 MHz)	BLY33	66	V
	BLY34	40	V
V_{CEO} max.	BLY33	33	V
	BLY34	20	V
V_{EBO} max.		4.0	V
I_C max.		0.5	A
I_{CM} max. ($f \geq 1.0$ MHz)		1.5	A
I_{CM} max. ($f < 1.0$ MHz)		0.5	A
P_{tot} max. $T_{case} = 25^\circ\text{C}$, $f \geq 1.0$ MHz		5.0	W
		$T_{case} = 25^\circ\text{C}$, $f < 1.0$ MHz	4.0 W

See also curves on pages 5 and 6

Temperature

T_j max.	Continuous operation	150	$^\circ\text{C}$
	Intermittent operation, total duration 200 hours	200	$^\circ\text{C}$
T_{stg} min.		-65	$^\circ\text{C}$
T_{stg} max.		150	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-case)}$	25 degC/W
------------------	-----------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CES}	Collector-emitter cut-off current				
	$V_{CE} = V_{CES} \text{ max.}, V_{BE} = 0$	-	0.10	5.0	mA
	$V_{CE} = V_{CEO} \text{ max.}, V_{BE} = 0$	-	0.02	0.5	mA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 4.0\text{V}, I_C = 0$	-	0.2 μ	0.5m	A
h_{FE}	Static forward current transfer ratio				
	$I_C = 0.2\text{A}, V_{CE} = 5.0\text{V}$	10	60	-	

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 0.2A$, $V_{CE} = 5.0V$, $f = 100MHz$, $T_{amb} = 25^\circ C$	250	450	-	MHz
C_{tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 0.5MHz$	-	11	15	pF
C_{te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 0.5MHz$	45	65	90	pF

RECOMMENDED OPERATING CONDITIONS

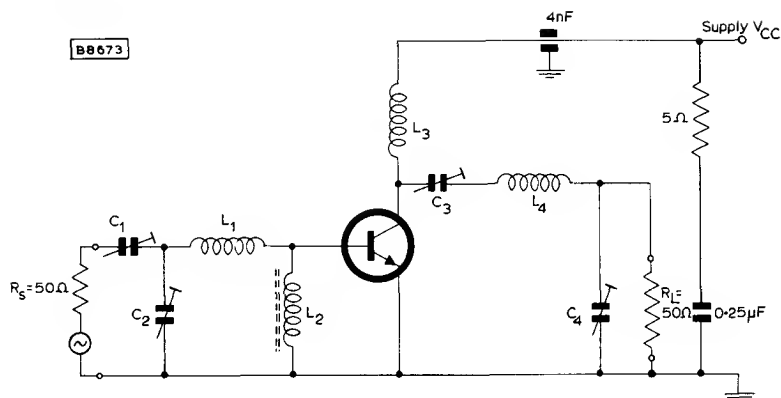
As a medium power amplifier for the output stage of a small transmitter, or as a driver for larger output stages.

$f = 175MHz$		BLY33		BLY34	
	Operation	a.m.	f.m.	f.m.	
V_{CC}	Supply voltage	nom.	13.8	28	13.8 V
		max.	16.5	32	16.5 V
V_B	Base bias voltage	0	0	0	V
P_o	Output power	2.0	3.0	3.0	W
P_i	Input power	typ.	0.32	0.28	0.5 W
		max.	0.40	0.40	0.6 W
I_{CC}	Supply current	typ.	180	160	270 mA
η	Efficiency	typ.	80	65	80 %

NOTES

1. For a.m. telephony, collector modulation of the output and driver stages is recommended.
2. A heatsink of thermal resistance $20degC/W$ is recommended for operation in ambient temperatures up to $65^\circ C$. At temperatures $> 65^\circ C$, derating is necessary.
3. Under the recommended a.m. operating condition and without modulation, the transistor can withstand any load mismatch. With modulation applied, operation into an extreme mismatch may adversely affect the life of the transistor and care should be exercised to keep the device within its ratings.

BASIC V.H.F. AMPLIFIER CIRCUIT

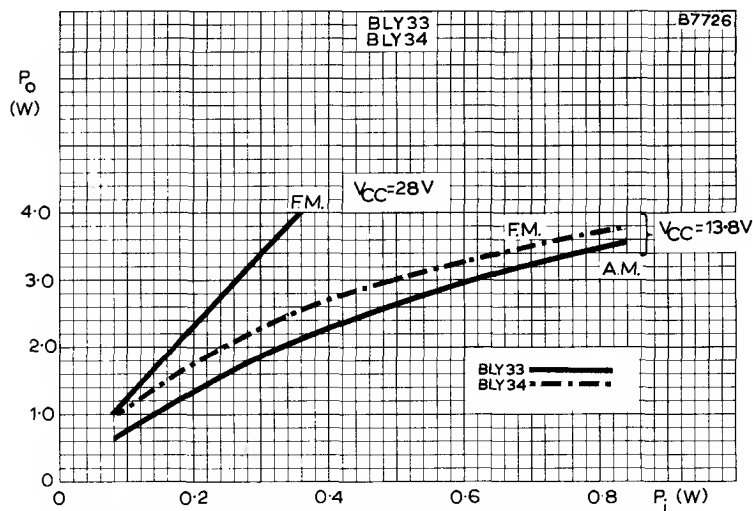


Component values for 175MHz amplifier circuit

C_1	30	pF
C_2	30	pF
C_3	30	pF
C_4	30	pF
L_1	1.0	inch of straight 18 s.w.g.
L_2	3.0	turns of 24 s.w.g. on Ferrite FX1115
L_3	5.0	turns of 18 s.w.g., $d=3/8"$, $l=3/8"$.
L_4	3.0	turns of 18 s.w.g., $d=3/8"$, $l=3/8"$.

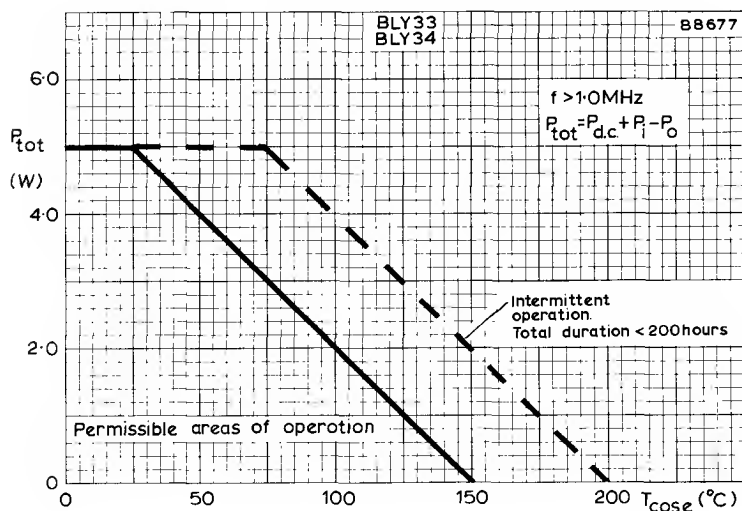
NOTE

To obtain optimum gain performance the emitter lead length should not exceed 1.6mm.

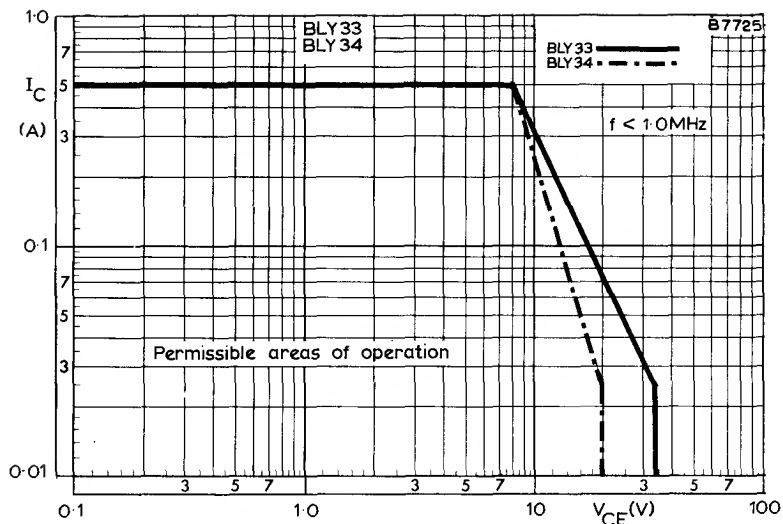


TYPICAL VARIATION OF OUTPUT POWER WITH INPUT POWER
FOR V.H.F. AMPLIFIER

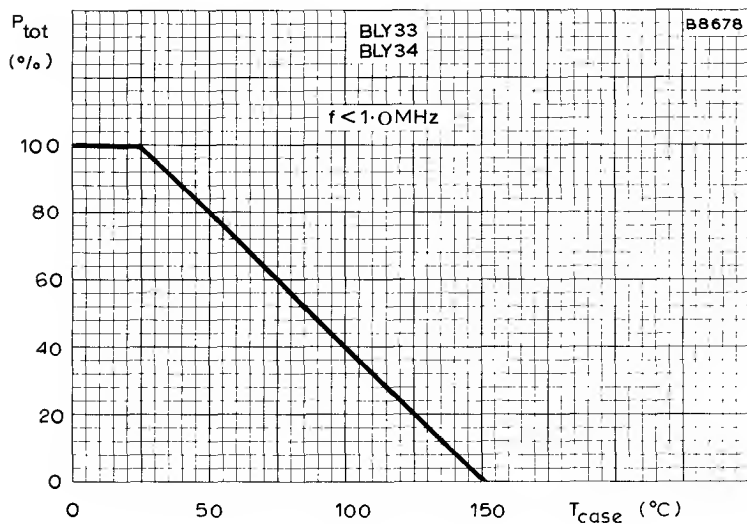
(See Recommended Operating Conditions on page 3)



MAXIMUM PERMISSIBLE POWER DISSIPATION PLOTTED AGAINST
CASE TEMPERATURE FOR FREQUENCIES $> 1.0MHz$



PERMISSIBLE AREAS OF OPERATION FOR FREQUENCIES < 1.0MHz



PERCENTAGE POWER DERATING PLOTTED AGAINST CASE TEMPERATURE FOR FREQUENCIES < 1.0MHz

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY35
BLY83

Silicon n-p-n transistors for v.h.f. mobile operation in class B. The BLY35 is mounted in a TO-60 envelope and the BLY83 is mounted in a plastic, capstan strip-line encapsulation.

The transistors are primarily intended for a.m. operation at 13.8V but are also suitable for f.m. operation at 24V.

QUICK REFERENCE DATA								
Mode	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (carrier) (W)	P_L into 50 Ω (W)	η (%)	m (%)	d_{tot} (%)
a. m.	13.8	175	0.35	7.0 typ.	-	77 typ.	80	<5
a. m.	13.8	80	0.06	7.5 typ.	-	77 typ.	80	<5
c. w.	24	175	1.35	-	13 typ.	65 typ.	-	-

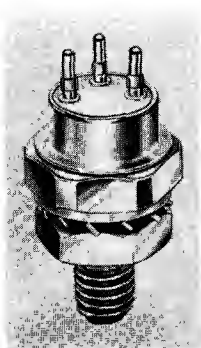
Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

BLY35 J.E.D.E.C. TO-60 (Emitter connected to stud)

BLY83 Capstan strip-line (Stud isolated)

For details see page 2



BLY35

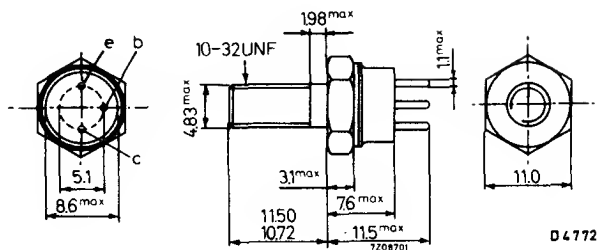


BLY83

Mullard

OUTLINE DRAWINGS (All dimensions in mm)

BLY35



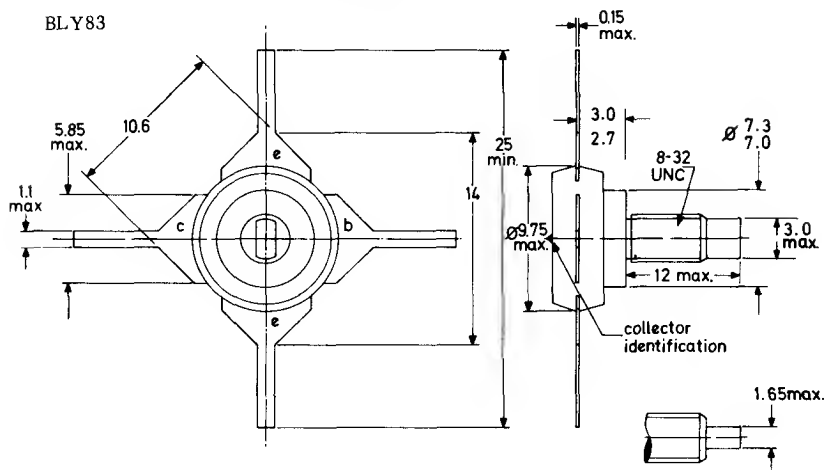
Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.8Nm (8kg cm)

max. 1.7Nm (17kg cm)

BLY83



All dimensions in mm

Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)

max. 0.85Nm (8.5kg cm)

Mullard

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY35
BLY83

RATINGS

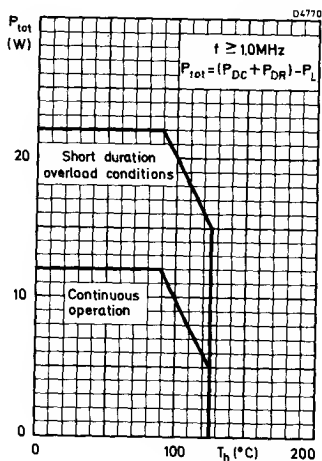
Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	66	V
V_{CESM} max.	66	V
V_{CEO} max.	33	V
V_{EBO} max.	4.0	V
I_C max.	2.5	A
I_{CM} max. ($f < 1.0\text{MHz}$)	2.5	A
I_{CM} max. ($f \geq 1.0\text{MHz}$)	7.5	A
P_{tot} max. ($f \geq 1.0\text{MHz}$, $T_h \leq 90^\circ\text{C}$)	12	W

Temperature

T_{stg}	BLY35	-65 to +200	$^\circ\text{C}$
	BLY83	-65 to +150	$^\circ\text{C}$



Mullard

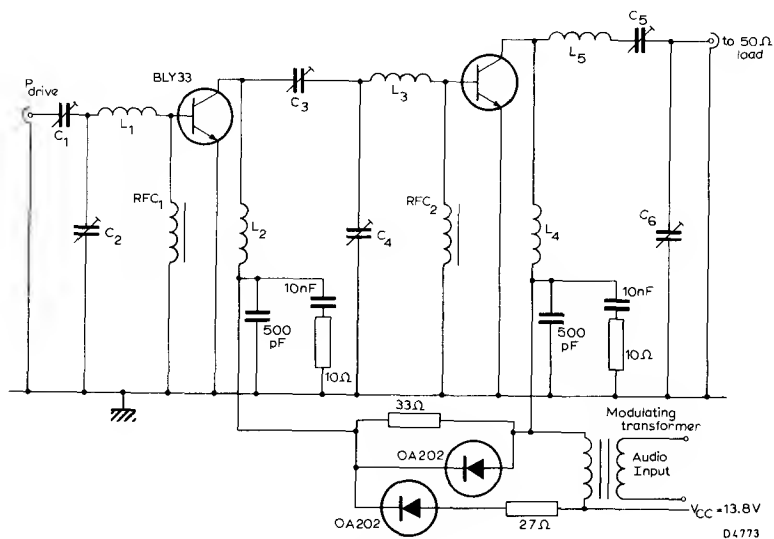
ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	66	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	66	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 50\text{mA}$	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
h_{FE}	Static forward current transfer ratio $I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$	10	60	220	
f_T	Transition frequency $I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$ $f = 100\text{MHz}$, $T_{amb} = 25^{\circ}\text{C}$	250	450	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	34	45	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	100	155	-	pF

APPLICATIONS INFORMATION

R. F. performance in a 7.0W a.m. transmitter at $f = 175\text{MHz}$,
 $f_{\text{mod.}} = 1\text{kHz}$

V_{CC} (V)	P_{DR} (W)	P_L (carrier) (W)	I_C (driver) (A)	I_C (amplifier) (A)	G_p (dB)	η (%)	m (%)	d_{tot} (%)
13.8	0.35	7.0 typ.	0.22 typ.	0.66 typ.	13	77 typ.	80	5 max.



Component values for 175MHz transmitter circuit: -

C_1 to $C_6 = 4$ to 29pF concentric trimmer capacitors

$L_1 = L_3 = 3$ turns of 1.2mm en. Cu wire, int. diam. = 6.4mm , length = 5.0mm

$L_2 = L_4 = 5$ turns of 1.2mm en. Cu wire, int. diam. = 6.4mm , length = 10mm

$L_5 = 3$ turns of 1.7mm en. Cu wire, int. diam. = 10mm , length = 10mm

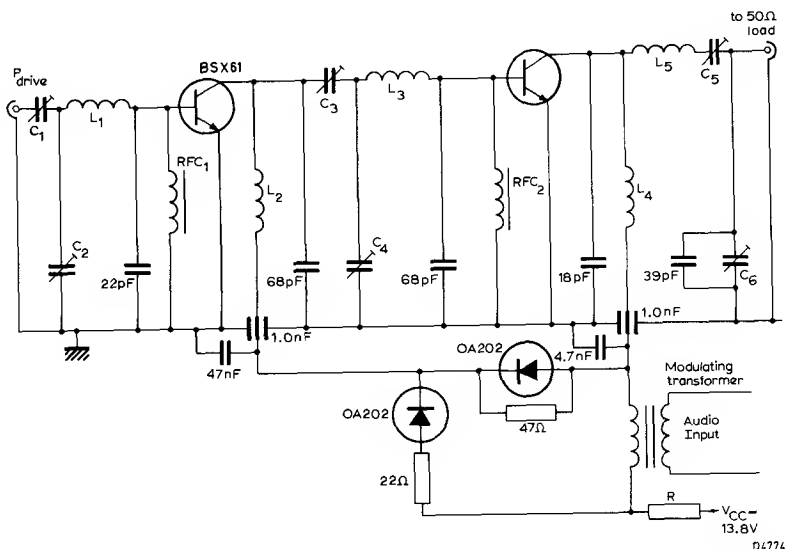
$RFC_1 = RFC_2 = 2$ turns of 0.4mm en. Cu wire on Ferrite FX1115.

The issue of the information contained in this publication does not imply
any authority or licence for the utilisation of any patented feature

APPLICATIONS INFORMATION (contd.)

R. F. performance in a 7.0W a.m. transmitter at $f = 80\text{MHz}$,
 $f_{\text{mod.}} = 1\text{kHz}$

V_{CC} (V)	P_{DR} (W)	P_L (carrier) (W)	I_C (driver) (A)	I_C (amplifier) (A)	G_p (dB)	η (%)	m (%)	d_{tot} (%)
13.8	0.06	7.5 typ.	0.06 typ.	0.7 typ.	21	70 typ.	80	5 max.



Component values for 80MHz transmitter circuit: -

C_1 to $C_6 = 4$ to 29pF concentric trimmer capacitors

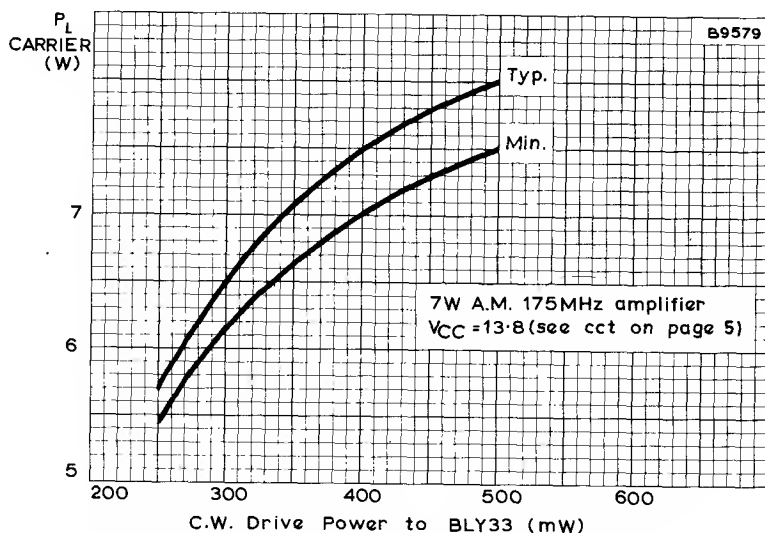
$L_1 = L_4 = 5$ turns of 1.2mm en.Cu wire, int.diam. = 6.3mm , length = 9.0mm

$L_3 = L_6 = 3$ turns of 1.2mm en.Cu wire, int.diam. = 7.0mm , length = 6.0mm

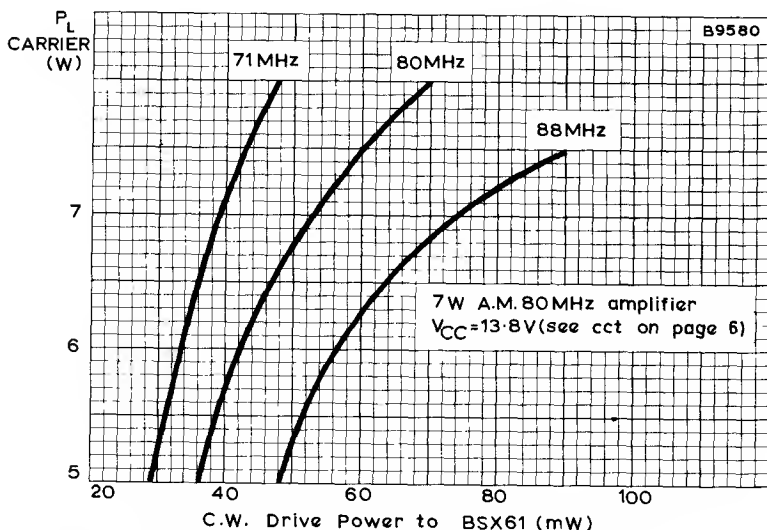
$L_7 = 6$ turns of 2.0mm en.Cu wire, int.diam. = 10mm , length = 13mm

$L_2 = L_5 = 1$ turn of 0.4mm en.Cu wire on Ferrite FX1115

R This resistor is incorporated to reduce the carrier level to 8W or below.



AERIAL CARRIER POWER PLOTTED AGAINST C. W. DRIVE POWER FOR
THE 7W A.M. 175MHz AMPLIFIER (see page 5)

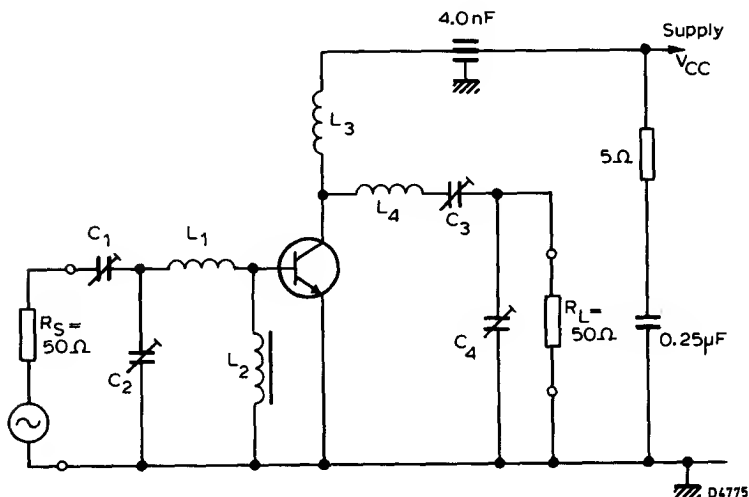


AERIAL CARRIER POWER PLOTTED AGAINST C. W. DRIVE POWER FOR
THE 7W A.M. 80MHz AMPLIFIER (see page 6)

APPLICATIONS INFORMATION (contd.)

R. F. performance in c. w. operation at $f = 175\text{MHz}$, $T_h \leq 40^\circ\text{C}$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	G_p (dB)
24	1.35	13 typ.	65 typ.	9.8
13.8	1.35	7.5 typ.	-	-



Component values for 175MHz amplifier circuit: -

$C_1 = C_3 = C_4 = 30\text{pF max.}$
 $C_2 = 60\text{pF max.}$

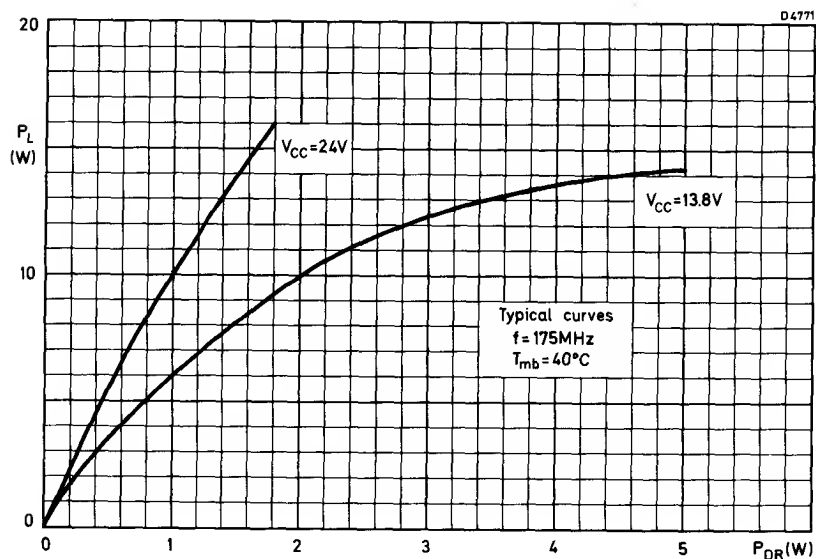
concentric trimmer capacitors

$L_1 = 25.4\text{mm}$ of straight 1.7mm Cu wire

$L_2 = 3$ turns of 0.5mm Cu wire on Ferrite FX1115

$L_3 = 3$ turns of 1.7mm Cu wire, int. diam. = 9.5mm, length = 9.5mm

$L_4 = 2$ turns of 2.0mm Cu wire, int. diam. = 12.7mm, length = 9.5mm

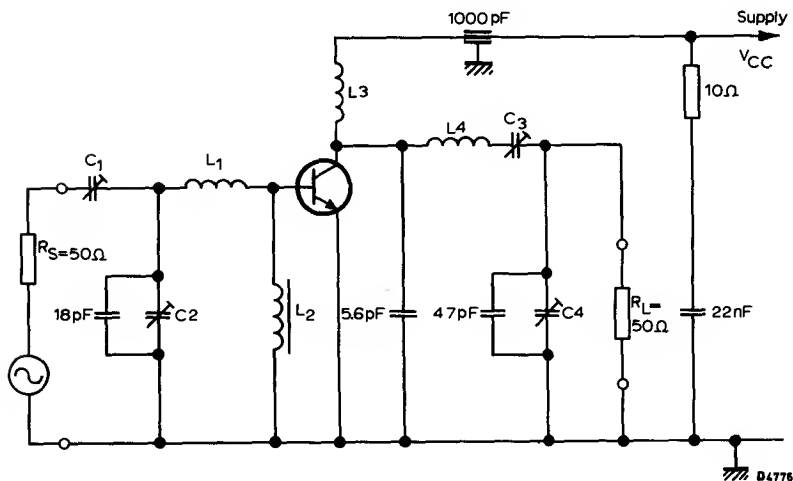


LOAD POWER PLOTTED AGAINST DRIVE POWER

APPLICATIONS INFORMATION (contd.)

R. F. performance in c.w. operation at $f = 80\text{MHz}$, $T_h \leq 40^\circ\text{C}$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)
13.8	0.5	12.5 typ.
6.9	0.5	5.0 typ.



Component values for 80MHz amplifier circuit: -

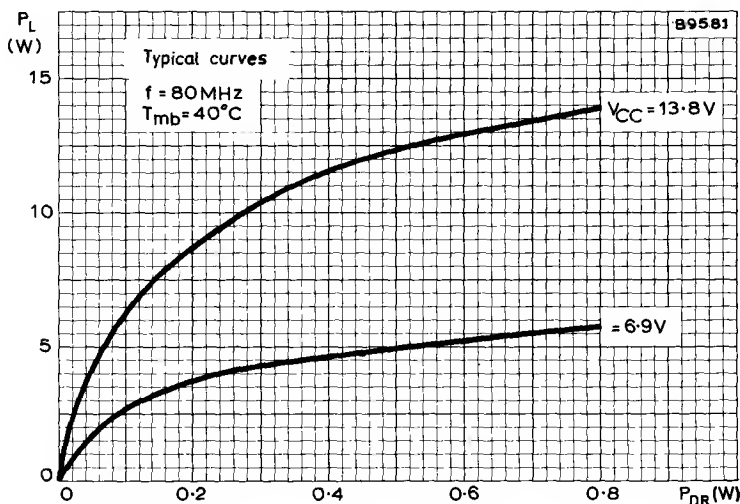
$C_1 = C_2 = C_3 = C_4 = 4$ to 29pF concentric trimmer capacitors

$L_1 = 4$ turns of 1.2mm Cu wire, int. diam. = 6.3mm , length = 8.0mm

$L_2 = 2$ turns of 0.35mm Cu wire, on Ferrite FX1115

$L_3 = 5$ turns of 1.2mm Cu wire, int. diam. = 6.3mm , CLOSE WOUND

$L_4 = 5$ turns of 1.7mm Cu wire, int. diam. = 9.6mm , length = 12mm



LOAD POWER PLOTTED AGAINST DRIVE POWER

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY36
BLY84

Silicon n-p-n transistors for v.h.f. mobile operation in class B. The BLY36 is mounted in a TO-60 envelope and the BLY84 is mounted in a plastic, capstan strip-line encapsulation.

The transistors are primarily intended for f. m. operation at 13.8V.

QUICK REFERENCE DATA					
V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50 Ω (W)	η (%)	Circuit
13.8	175	1.2	7.0 typ.	77 typ.	Un-neutralised
13.8	175	3.4	13.2 typ.	79 typ.	common-emitter
13.8	80	0.5	13.5 typ.	80 typ.	class B.

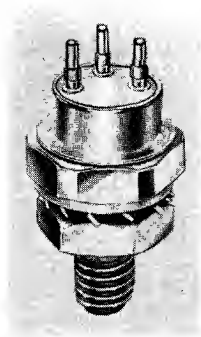
Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

BLY36 J. E. D. E. C. TO-60 (Emitter connected to stud)

BLY84 Capstan strip-line (Stud isolated)

For details see page 2



BLY36

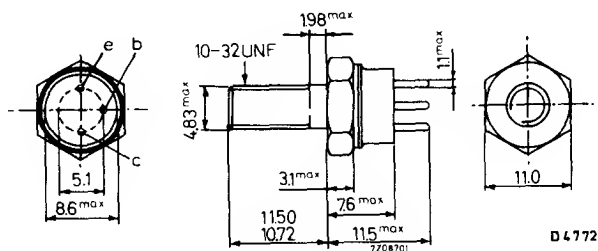


BLY84

Mullard

OUTLINE DRAWINGS (All dimensions in mm)

BLY36



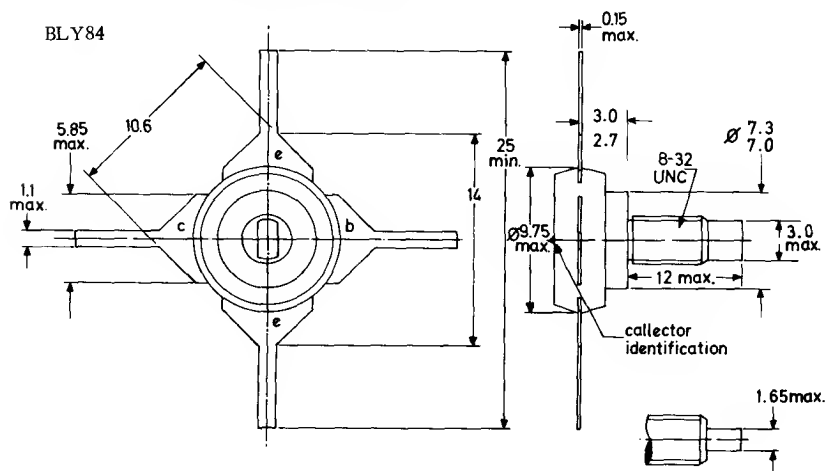
Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.8Nm (8kg cm)

max. 1.7Nm (17kg cm)

BLY84



Accessories

All dimensions in mm

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)

max. 0.85Nm (8.5kg cm)

D 3370

Mullard

RATINGS

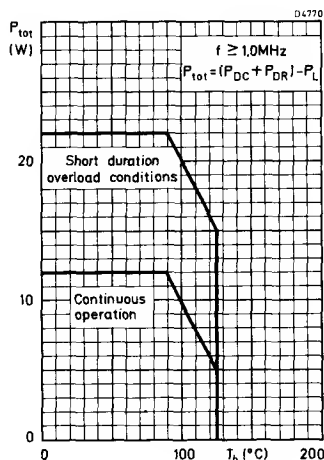
Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	40	V
V_{CESM} max. ($R_{BE} = 0$)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	4.0	V
I_C max.	2.5	A
I_{CM} max. ($f < 1.0\text{MHz}$)	2.5	A
I_{CM} max. ($f \geq 1.0\text{MHz}$)	7.5	A
P_{tot} max. ($f \geq 1.0\text{MHz}$, $T_h \leq 90^\circ\text{C}$)	12	W

Temperature

T_{stg}	BLY36	-65 to +200	$^\circ\text{C}$
	BLY84	-65 to +150	$^\circ\text{C}$



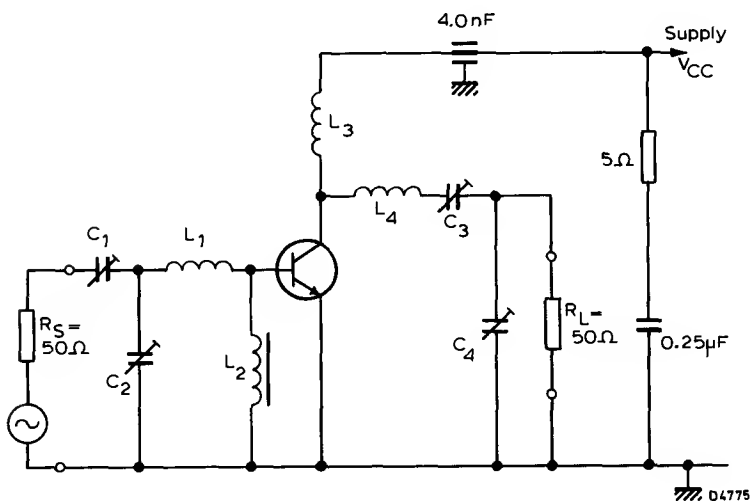
ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	40	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	40	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 50\text{mA}$	20	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	-	V
h_{FE}	Static forward current transfer ratio $I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$	10	60	-	
f_T	Transition frequency $I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$ $f = 100\text{MHz}$, $T_{amb} = 25^{\circ}\text{C}$	250	450	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	37	45	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	100	155	-	pF

APPLICATIONS INFORMATION

R. F. performance in c. w. operation at $f = 175\text{MHz}$, $T_h \leq 40^\circ\text{C}$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	G_p (dB)
13.8	1.2	7.0 typ.	77 typ.	7.6
13.8	3.4	13.2 typ.	79 typ.	5.8



Component values for 175MHz amplifier circuit: -

$C_1 = C_3 = C_4 = 30\text{pF}$ max. concentric trimmer capacitors

$C_2 = 60\text{pF}$ max. concentric trimmer capacitor

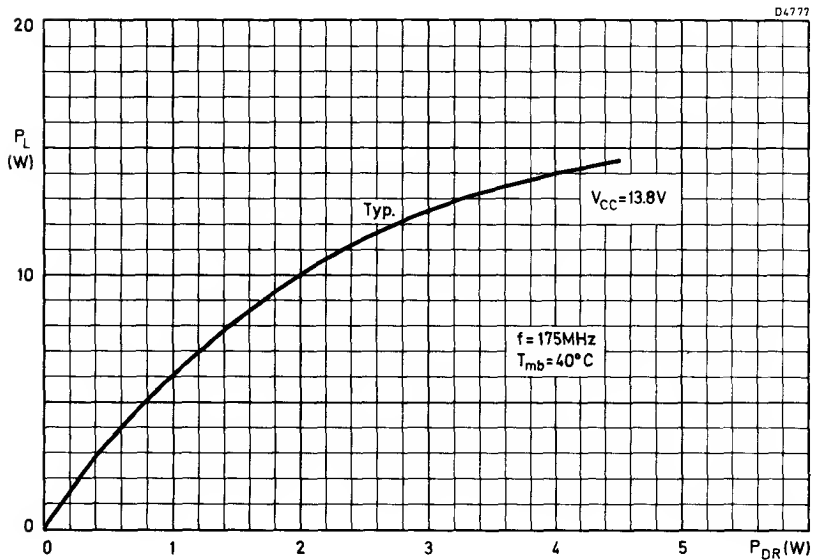
$L_1 = 25.4\text{mm}$ of straight 1.7mm Cu wire

$L_2 = 3$ turns of 0.5mm Cu wire on Ferrite FX1115

$L_3 = 3$ turns of 1.7mm Cu wire, int. diam. $\approx 9.5\text{mm}$, length $= 9.5\text{mm}$

$L_4 = 2$ turns of 2.0mm Cu wire, int. diam. $\approx 12.7\text{mm}$, length $= 9.5\text{mm}$

The issue of the information contained in this publication does not imply any authority or licence for the utilisation of any patented feature

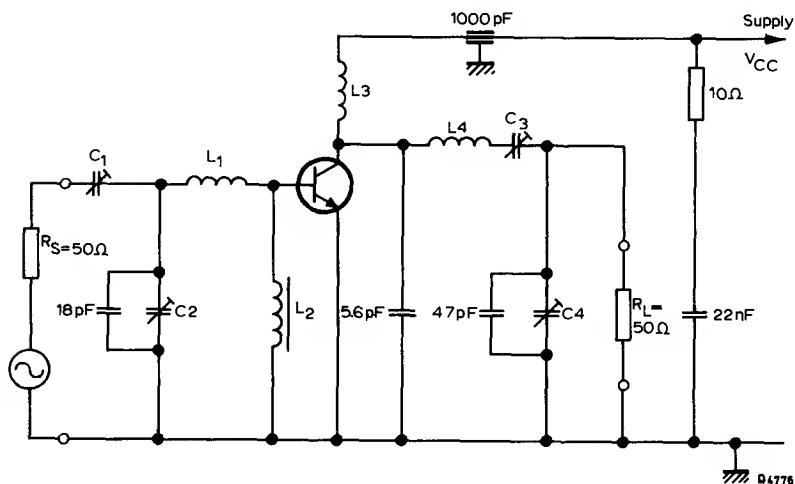


LOAD POWER PLOTTED AGAINST DRIVE POWER

APPLICATIONS INFORMATION (contd.)

R. F. performance in c.w. operation at $f = 80\text{MHz}$, $T_h \leq 40^\circ\text{C}$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	G_p (dB)
13.8	0.5	13.5 typ.	80 typ.	14.2
6.9	0.5	5.5 typ.	80 typ.	10.3



Component values for 80MHz amplifier circuit: -

$C_1 = C_2 = C_3 = C_4 = 4$ to 29pF concentric trimmer capacitors

$L_1 = 4$ turns of 1.2mm Cu wire, int. diam. = 6.3mm , length = 8.0mm

$L_2 = 2$ turns of 0.35mm Cu wire, on Ferrite FX1115

$L_3 = 5$ turns of 1.2mm Cu wire, int. diam. = 6.3mm , CLOSE WOUND

$L_4 = 5$ turns of 1.7mm Cu wire, int. diam. = 9.6mm , length = 12mm

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLY53A

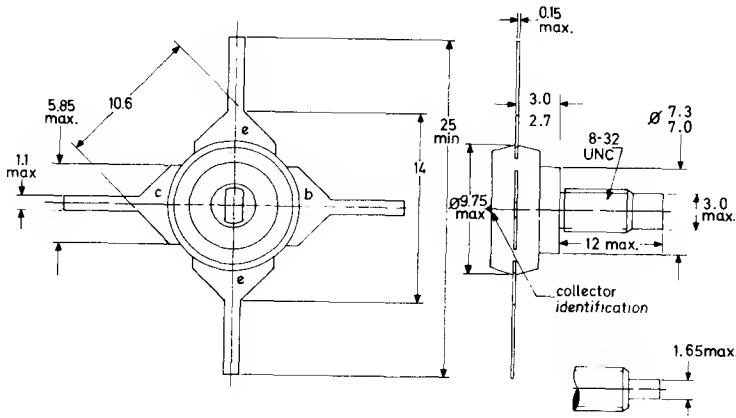
Silicon n-p-n transistor for v.h.f./u.h.f. mobile applications. The device is mounted in a plastic, capstan strip-line encapsulation.

With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLY53A will produce 7.0W output into a 50 Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50 Ω (W)	η (%)	T_h (°C)	Circuit
12.5	470	2.2	7.0 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	2.0	7.0 min.	65 min.	25	
13.8	470	2.0	7.8 typ.	70 typ.	25	
12.5	175	0.4	7.2 typ.	66 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D 3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

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RATINGS

Limiting values of operation according to the absolute maximum system.

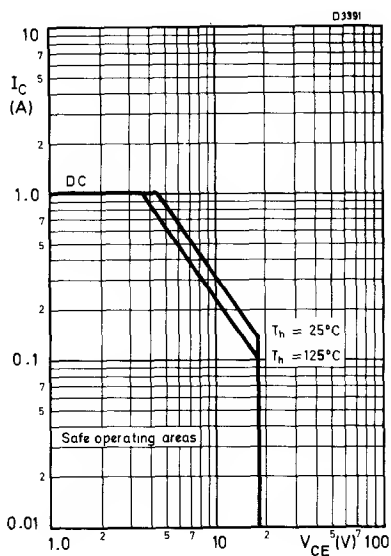
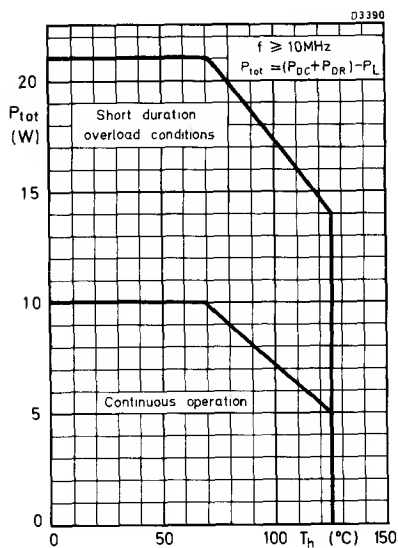
Electrical

V_{CBOM} max.	36	V
V_{CESM} max. ($R_{BE} = 0$)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	1.0	A
I_{CM} max. ($f \geq 10\text{MHz}$)	4.0	A
P_{tot} max. ($f \geq 10\text{MHz}$, $T_h \leq 70^\circ\text{C}$)	10	W

See also graph below

Temperature

T_{stg}	-65 to +150	$^\circ\text{C}$
-----------	-------------	------------------



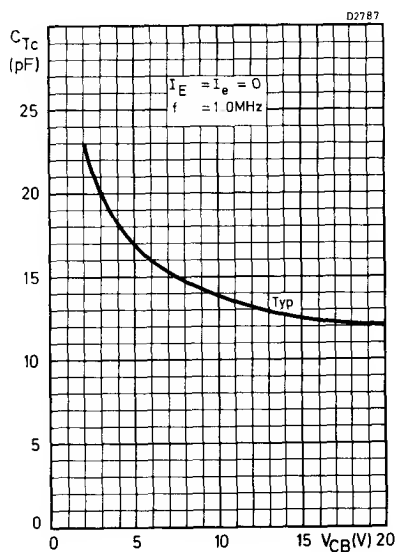
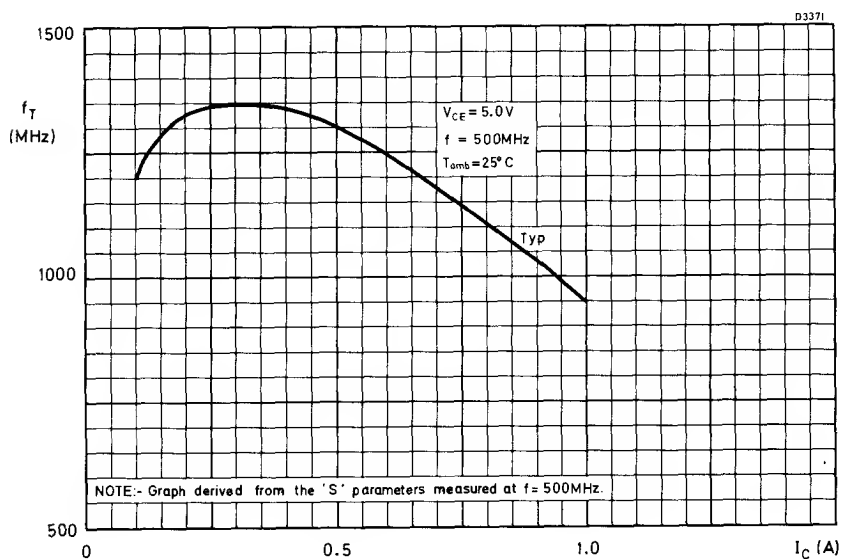
N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLY53A

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\text{mA}$	36	-	- V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\text{mA}$, $R_{BE} = 0$	36	-	- V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 25\text{mA}$	18	-	- V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 1.0\text{mA}$	4.0	-	- V
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 0.5\text{A}$, $I_B = 0.1\text{A}$	-	0.2	- V
h_{FE}	Static forward current transfer ratio $I_C = 0.5\text{A}$, $V_{CE} = 5.0\text{V}$	10	40	-
$*f_T$	Transition frequency $I_C = 0.5\text{A}$, $V_{CE} = 5.0\text{V}$, $f = 500\text{MHz}$	-	1300	- MHz
C_{Tc}	Collector capacitance $V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	14	20 pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	-	65	- pF
C_{cs}	Collector-stud capacitance	-	2.0	- pF

*Derived from the 'S' parameters measured at $f = 500\text{MHz}$, $T_{amb} = 25^{\circ}\text{C}$.



N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLY53A

APPLICATION INFORMATION

R. F. Performance in c. w. operation ($T_h = 25^\circ\text{C}$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mmho)
12.5	470	2.2	7.0 min.	65 min.	-	-
13.8	470	2.0	7.0 min.	65 min.	-	-
13.8	470	2.0	7.8 typ.	70 typ.	$2.3+j\ 6.3$	$50-j\ 36$
12.5	175	0.4	7.2 typ.	66 typ.	$3+j\ 0.5$	$90-j\ 40$

At $P_L = 7.0\text{W}$ and $V_{CC} = 12.5\text{V}$, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by $10\text{mW}/^\circ\text{C}$.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$$V_{CC} = 16.5\text{V} \quad f = 470\text{MHz} \quad T_h = 70^\circ\text{C}$$

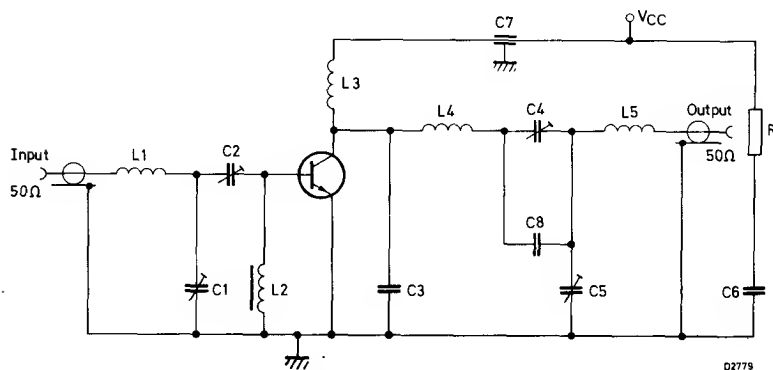
$$V.S.W.R. = 50:1 \quad \text{at any phase}$$

$$P_{DR} = P_{DR \text{ nom.}} + 20\%$$

$$\text{Where } P_{DR \text{ nom.}} = P_{DR} \text{ for } 7.0\text{W transistor output into } 50\Omega$$

$$\text{load at } V_{CC} = 13.8\text{V.}$$

470MHz Amplifier circuit



The issue of the information contained in this publication does not imply any authority or licence for the utilisation of any patented feature.

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APPLICATION INFORMATION (contd.)

Component values for 470MHz amplifier circuit

C1 = C2 = C4 = C5 = 1.8 to 18pF film dielectric trimmer capacitors

C3 = 6.8pF ceramic capacitor

C6 = 0.1μF ceramic capacitor

C7 = 4000pF feed-through capacitor

C8 = 10pF ceramic capacitor

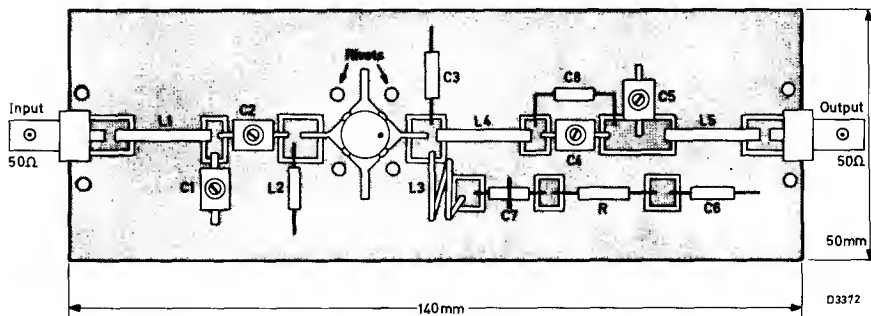
L1 = L4 = L5 = 20mm of straight 1.2mm copper wire. Height above board = 2mm

L2 = 0.47μH choke

L3 = 1 turn of 1.7mm copper wire, int. dia. 10mm, lead length = 5mm

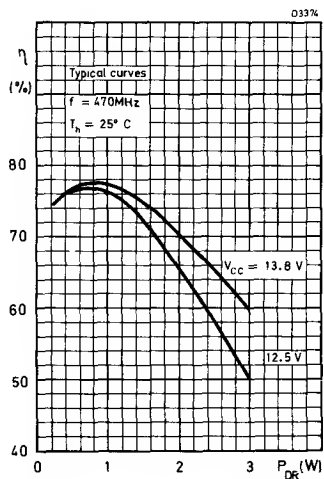
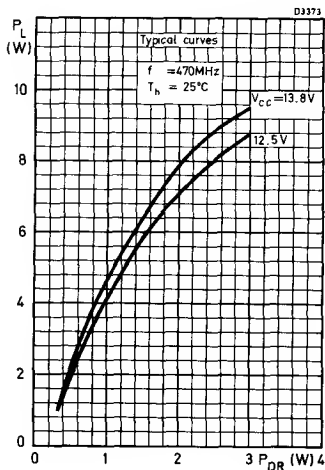
R = 10Ω - carbon

Component layout on 1.5mm double copper clad fibre-glass board



Shaded area copper

Underside area completely copper clad

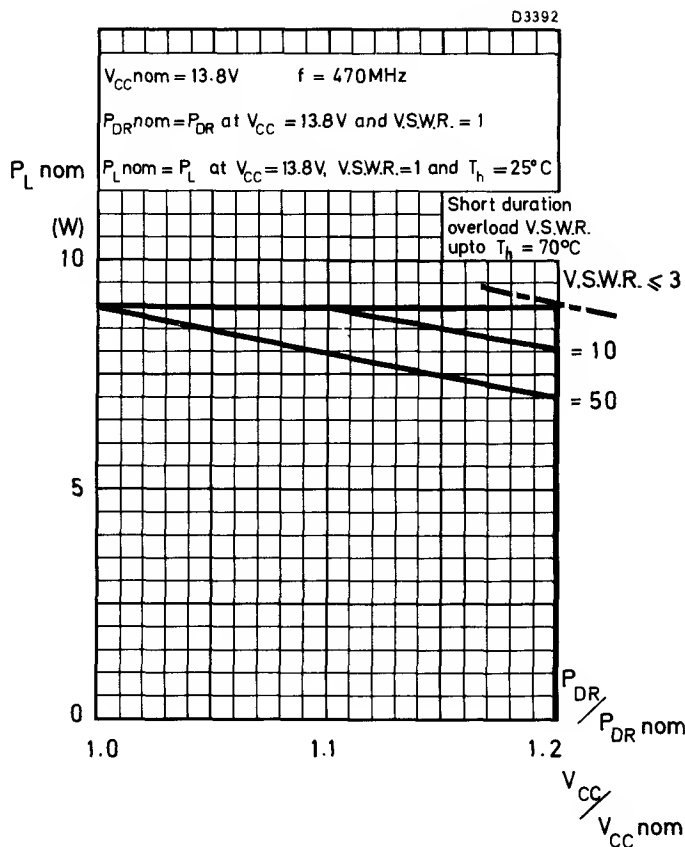


TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLY53A

APPLICATION INFORMATION (contd.)



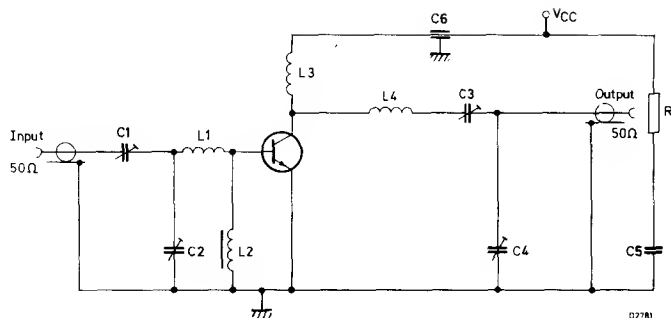
INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 9 watts load power in the circuit on page 5, and subsequently subjected to various voltage overloads and mismatch conditions with v. s. w. r. up to 50:1 at a heatsink temperature of 70°C . This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v. s. w. r. in the recommended circuit.

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APPLICATION INFORMATION (contd.)

175MHz Amplifier circuit



Component values for 175MHz amplifier circuit

$C1 = 30\text{pF}$
 $C2 = 60\text{pF}$
 $C3 = 30\text{pF}$
 $C4 = 30\text{pF}$

concentric trimmer capacitors

$C5 = 0.25\mu\text{F}$ ceramic capacitor

$C6 = 4.0\text{nF}$ feed-through capacitor

$L1 = 25\text{mm}$ of straight 1.2mm copper wire. Height above board = 3mm

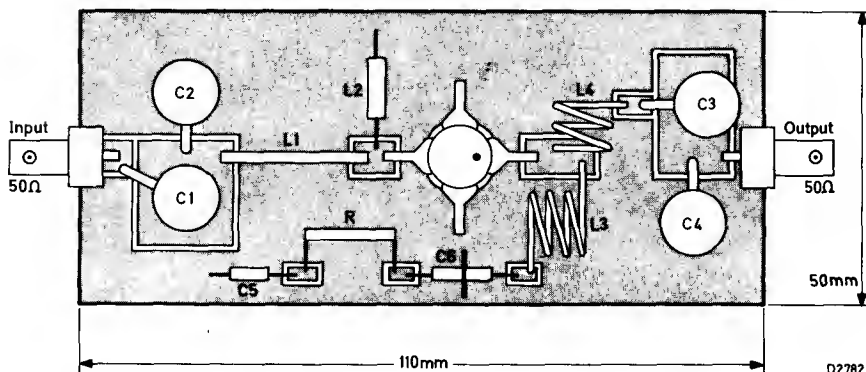
$L2 = 3$ turns of 0.5mm copper wire on Ferrite FX1115

$L3 = 5$ turns of 1.2mm copper wire $d = 10\text{mm}$. Close wound, lead length = 5mm

$L4 = 3$ turns of 1.2mm copper wire $d = 10\text{mm}$. Close wound, lead length = 5mm

$R = 10\Omega$ - carbon

Component layout on 1.5mm single copper clad fibre-glass board



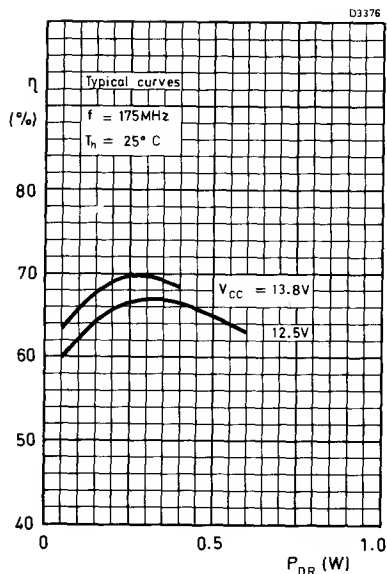
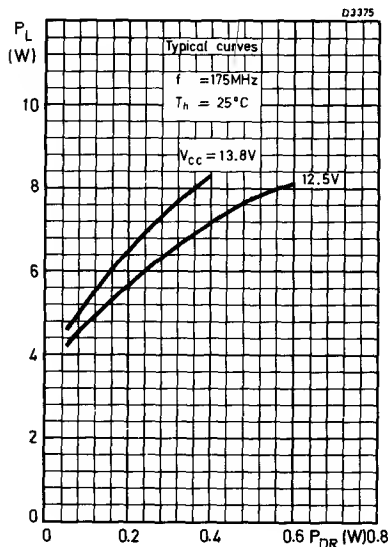
Shaded area copper

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N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLY53A

APPLICATION INFORMATION (contd.)



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
 MULLARD LIMITED
 P.O. BOX 142
 NEW ROAD
 MITCHAM
 SURREY, CR4 4SR.

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N-P-N SILICON V.H.F. POWER TRANSISTOR

BLY55

TENTATIVE DATA

Silicon n-p-n high frequency medium power transistor primarily intended for class B operation in v.h.f. amplifiers. The emitter is electrically connected to the envelope.

QUICK REFERENCE DATA

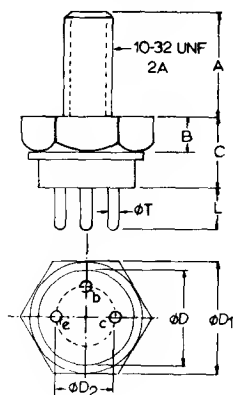
V_{CES} max. (peak r.f. $\geq 1.0\text{MHz}$)	40	V
V_{CEO} max.	20	V
I_{CM} max. (peak r.f. $\geq 1.0\text{MHz}$)	3.0	A
P_{tot} max. ($T_{mb} \leq 100^\circ\text{C}$)	4.0	W
T_j max.	150	$^\circ\text{C}$
f_T min. ($I_C = 0.2\text{A}$, $V_{CE} = 5.0\text{V}$, $f = 100\text{MHz}$)	250	MHz

Performance in a 175MHz common emitter amplifier:

Operation:		f.m.	
V_{CC}	Supply voltage	13.8	V
P_o	Output power	4.0	W
G_p	Power gain (typ.)	10	dB
η	Efficiency (typ.)	70	%

OUTLINE AND DIMENSIONS

Conforms to J. E. D. E. C. TO-60



Millimetres

	Min.	Max.
A	9.53	11.56
B	2.29	3.43
C	5.46	8.13
ϕD	8.13	9.14
ϕD_1	10.77	11.10
ϕD_2	4.58	5.58
L	3.56	4.06
ϕT	0.76	1.17

Emitter electrically connected to envelope

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CES} max. (peak r.f. $\geq 1.0\text{MHz}$)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	4.0	V
I_C max.	1.0	A
I_{CM} max. (peak r.f. $\geq 1.0\text{MHz}$)	3.0	A
I_{CM} max. (peak r.f. $< 1.0\text{MHz}$)	1.0	A
P_{tot} max. $T_{mb} = 25^\circ\text{C}$, $f \geq 1.0\text{MHz}$	10	W
$T_{mb} = 25^\circ\text{C}$, $f < 1.0\text{MHz}$	8.0	W

See also pages 5 and 6

Temperature

T_{stg} range	-65 to +150	$^\circ\text{C}$
T_j max. Continuous operation	150	$^\circ\text{C}$
Intermittent operation, total duration 200 hours	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	12.5	degC/W
----------------	------	--------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CES}	Collector-emitter cut-off current				
	$V_{CE} = 40\text{V}$, $V_{EB} = 0$	-	0.10	5.0	mA
	$V_{CE} = 20\text{V}$, $V_{EB} = 0$	-	0.02	0.5	mA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 4.0\text{V}$, $I_C = 0$	-	0.1 μ	0.5m	A
h_{FE}	Static forward current transfer ratio				
	$I_C = 0.2\text{A}$, $V_{CE} = 5.0\text{V}$	10	60	-	

N-P-N SILICON V.H.F. POWER TRANSISTOR

BLY55

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 0.2A$, $V_{CE} = 5.0V$, $f = 100MHz$, $T_{amb} = 25^{\circ}C$	250	450	-	MHz
C_{tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_C = 0$, $f = 0.5MHz$	-	11	15	pF
C_{te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_E = 0$, $f = 0.5MHz$	45	65	90	pF

RECOMMENDED OPERATING CONDITIONS

As a medium power amplifier for the output stage of a small transmitter or as a driver for larger output stages.

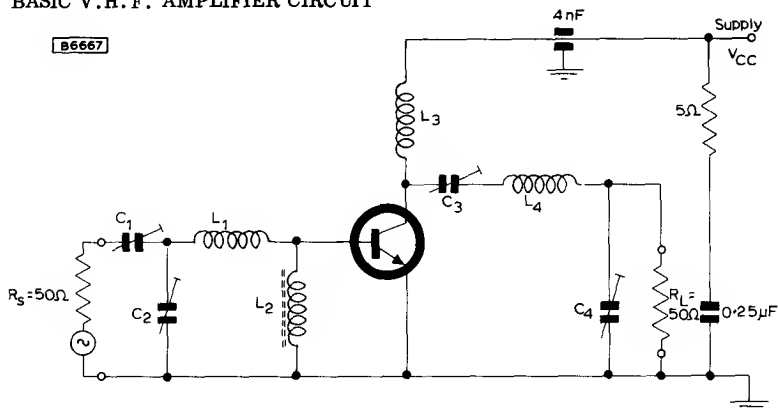
F.M. Operation

f	Operating frequency		175	MHz
V_{CC}	Supply voltage	nom.	13.8	V
		max.	16.5	V
V_B	Base bias voltage		0	V
P_o	Output power		4.0	W
P_i	Input power	typ.	0.4	W
		max.	0.6	W
I_{CC}	Supply current	typ.	420	mA
η	Efficiency	typ.	70	%

A heatsink of thermal resistance $10^{\circ}C/W$ is recommended for operation in ambient temperatures up to $65^{\circ}C$. At temperatures $> 65^{\circ}C$, derating is necessary.

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BASIC V.H. F. AMPLIFIER CIRCUIT



The emitter is earthed via the case and the emitter pin is not connected

Component values for 175MHz amplifier circuit:-

C_1	30	pF
C_2	60	pF
C_3	30	pF
C_4	30	pF
L_1	1.0	inch of straight 18 s.w.g.
L_2	3.0	turns of 24 s.w.g. on Ferrite FX1115
L_3	5.0	turns of 18 s.w.g., $d=3/8"$, $l=3/8"$.
L_4	3.0	turns of 18 s.w.g., $d=3/8"$, $l=3/8"$.

CAUTION

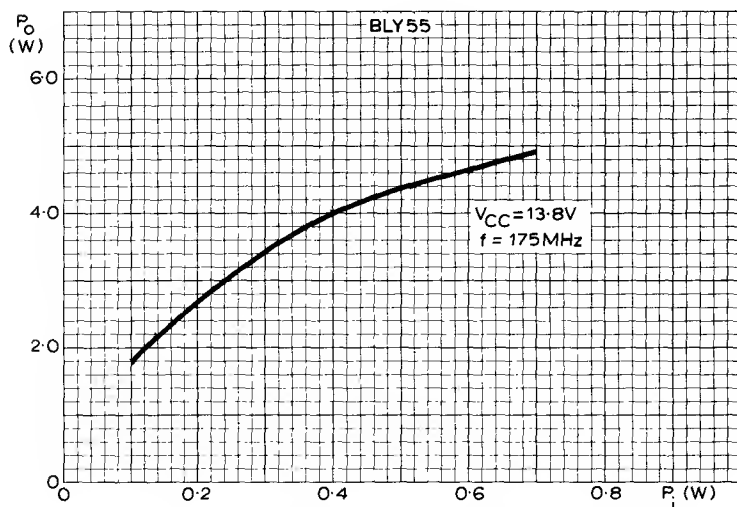
This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

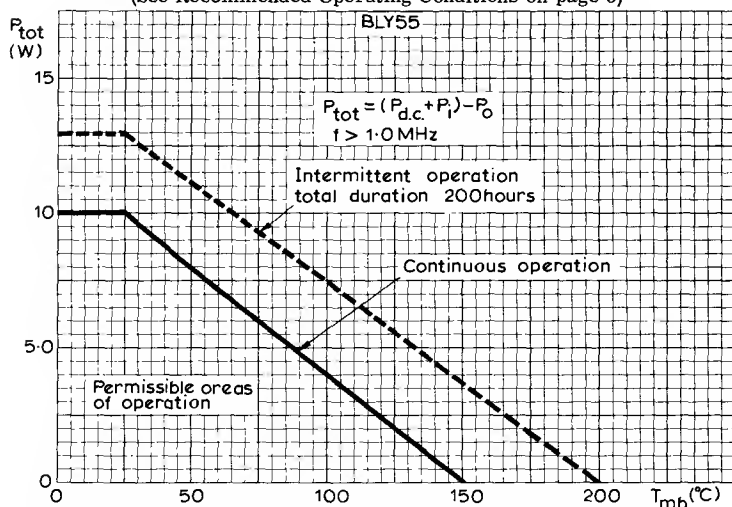
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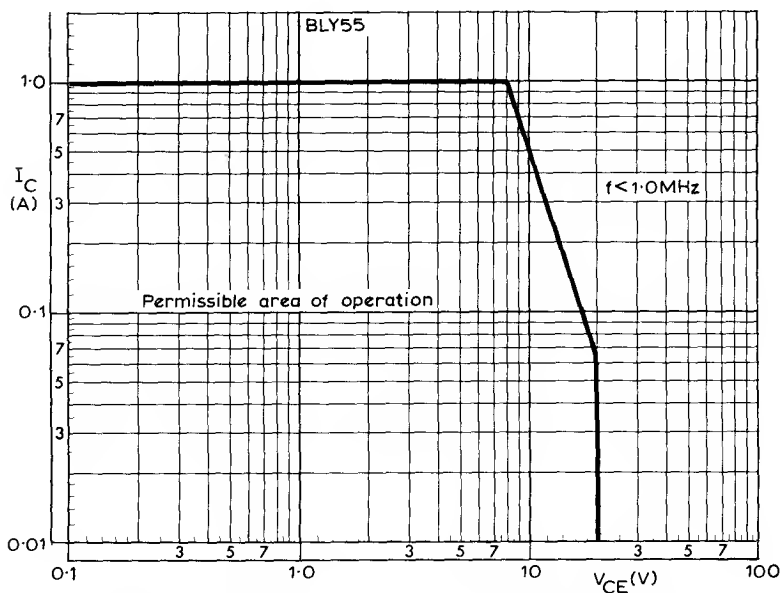


**TYPICAL VARIATION OF OUTPUT POWER WITH INPUT POWER
FOR V.H.F. AMPLIFIER**

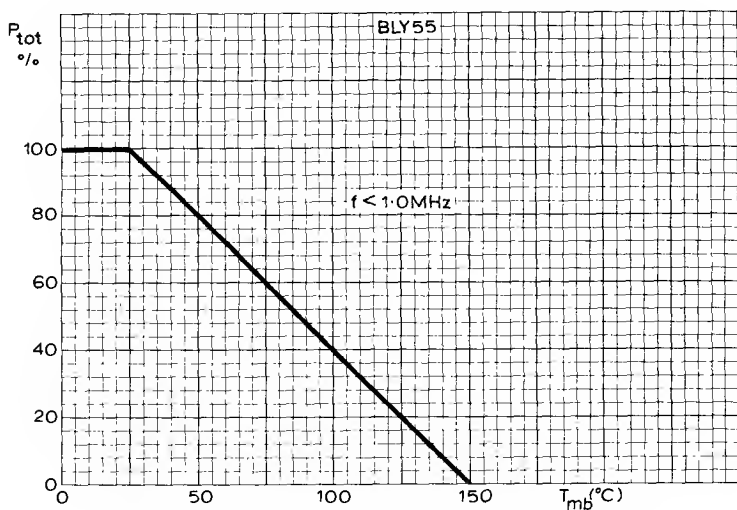
(See Recommended Operating Conditions on page 3)



**MAXIMUM PERMISSIBLE POWER DISSIPATION P_{TOT} PLOTTED AGAINST
MOUNTING-BASE TEMPERATURE FOR FREQUENCIES > 1.0 MHz**



PERMISSIBLE AREA OF OPERATION FOR FREQUENCIES < 1.0 MHz



PERCENTAGE POWER DERATING PLOTTED AGAINST
MOUNTING-BASE TEMPERATURE FOR FREQUENCIES < 1.0 MHz

**N-P-N SILICON PLANAR
V.H.F. TRANSISTORS**

**BLY83
BLY84**

For details see data sheets for types BLY35, BLY36 respectively

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY85
BLY97

TENTATIVE DATA

The BLY85 and BLY97 are primarily intended for class B operation in the v.h.f. driver stages of mobile transmitters. The BLY85 is designed for 4W f.m. operation at 13.8V supply and the BLY97 for 4W f.m. operation at 24V supply.

QUICK REFERENCE DATA

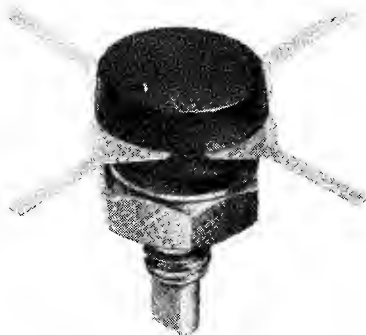
Typical c.w. performance at $T_{mb} \leq 40^{\circ}\text{C}$

Type No.	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	η (%)
BLY85	13.8	175	0.2	4.0	64
BLY97	24	175	0.14	4.0	52

Unless otherwise stated data are applicable to both types

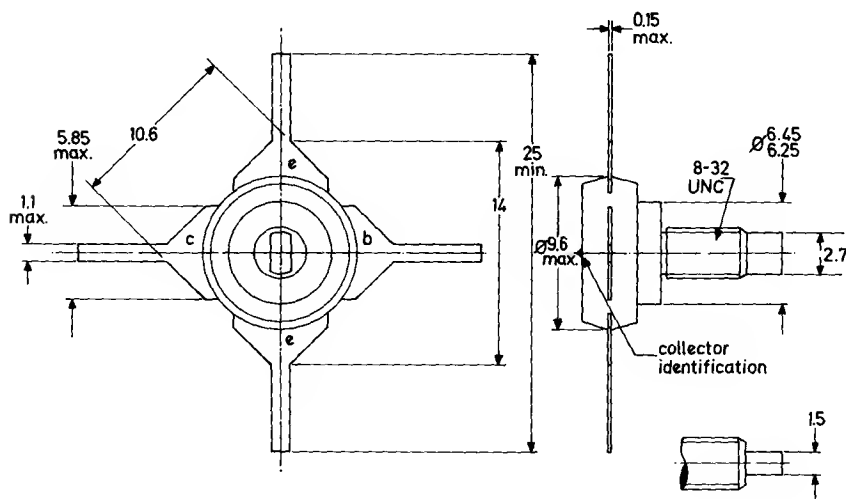
OUTLINE AND DIMENSIONS

For details see page 2



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OUTLINE AND DIMENSIONS



All dimensions in mm.

D828

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)

max. 0.85Nm (8.5kg cm)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical		BLY85	BLY97	
V_{CES}	max. ($f \geq 1.0\text{MHz}$)	40	66	V
V_{CEO}	max.	20	33	V
V_{EBO}	max.	4.0	4.0	V
I_C	max.	1.0	1.0	A
I_{CM}	max. ($f < 1.0\text{MHz}$)	1.0	1.0	A
I_{CM}	max. ($f \geq 1.0\text{MHz}$)	3.0	3.0	A
P_{tot}	max. ($f \geq 1.0\text{MHz}$, $T_{mb} \leq 25^\circ\text{C}$)	10	10	W
P_{tot}	max. ($f < 1.0\text{MHz}$, $T_{mb} \leq 25^\circ\text{C}$)	8.0	8.0	W
Temperature				
T_{stg}	range	-30 to +150		$^\circ\text{C}$
T_j	max. (continuous operation)	150		$^\circ\text{C}$
T_j	max. (short duration overload conditions)	200		$^\circ\text{C}$

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N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY85
BLY97

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$ 12.5 degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Max.	
I_{CES}	Collector cut-off current			
	$V_{CE} = V_{CES \text{ max.}}, V_{BE} = 0$	-	5.0	mA
	$V_{CE} = 20V, V_{BE} = 0$	-	0.5	mA
I_{EBO}	Emitter cut-off current			
	$V_{EB} = 4.0V, I_C = 0$	-	0.5	mA
h_{FE}	Static forward current transfer ratio			
	$I_C = 0.2A, V_{CE} = 5.0V$	10	-	
f_T	Transition frequency			
	$I_C = 0.2A, V_{CE} = 5.0V$			
	$f = 100\text{MHz}, T_{amb} = 25^\circ\text{C}$	250	-	MHz
C_{Tc}	Collector capacitance			
	$V_{CB} = 10V, I_E = I_C = 0, f = 0.5\text{MHz}$	-	15	pF
C_{Te}	Emitter capacitance			
	$V_{EB} = 0, I_C = I_E = 0, f = 0.5\text{MHz}$	45	90	pF

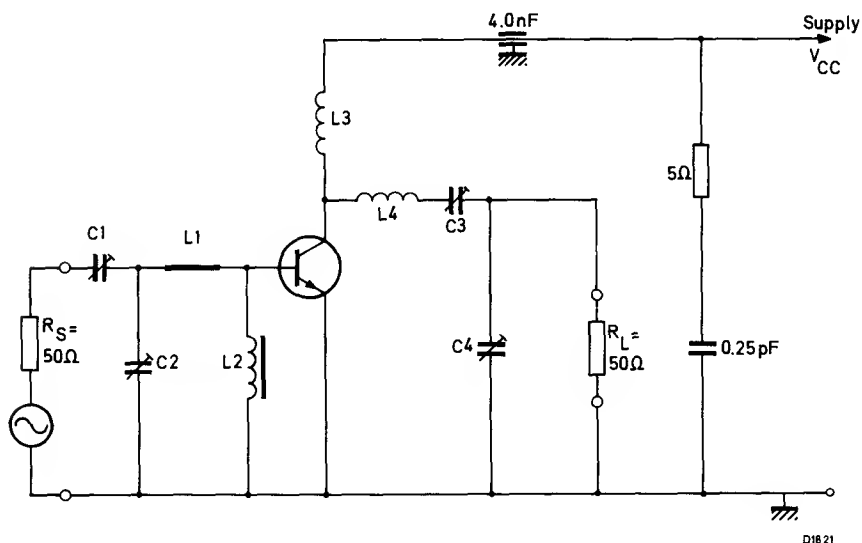
R.F. Performance in c.w. operation

$T_{mb} \leq 40^\circ\text{C}$

Type number	V_{CC} (V)		f (MHz)	$V_{CC} = \text{nom.}$		I_C (mA)	G_p (dB)	η (%)
				P_{DR} (W)	P_L (W)			
	nom.	max.			min.	max.	min.	min.
BLY85	13.8	16.5	175	0.4	4.0	480	10	60
BLY97	24	28	175	0.2	4.0	278	13	50

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BASIC V.H.F. AMPLIFIER CIRCUIT



Component values for 175MHz amplifier circuit

C1 = 30pF	L1 = 1.0 inch of straight 18 s.w.g.
C2 = 60pF	L2 = 3.0 turns of 24 s.w.g. on Ferrite FX1115
C3 = 30pF	L3 = 5.0 turns of 18 s.w.g., $d = 3/8"$, $l = 3/8"$
C4 = 30pF	L4 = 3.0 turns of 18 s.w.g., $d = 3/8"$, $l = 3/8"$

CAUTION

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DISPOSAL SERVICE

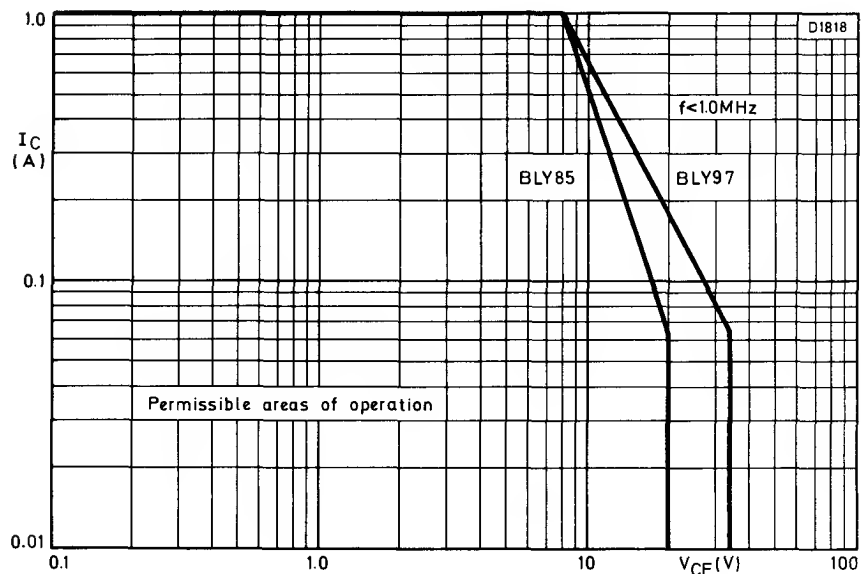
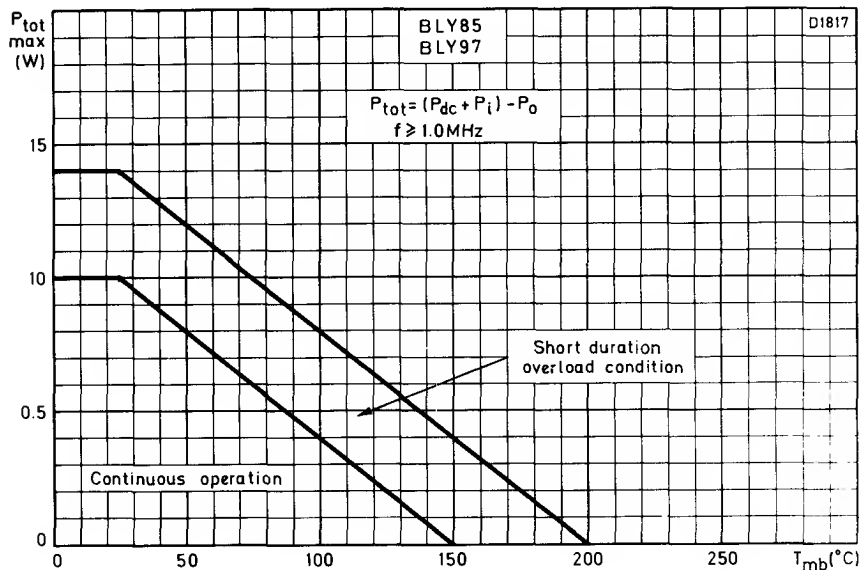
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MULLARD LIMITED
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SURREY, CR4 4XY.

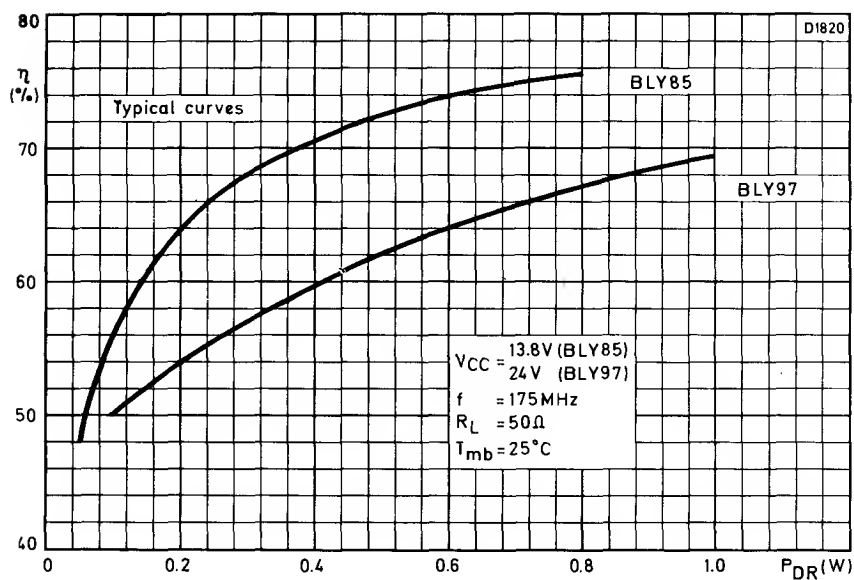
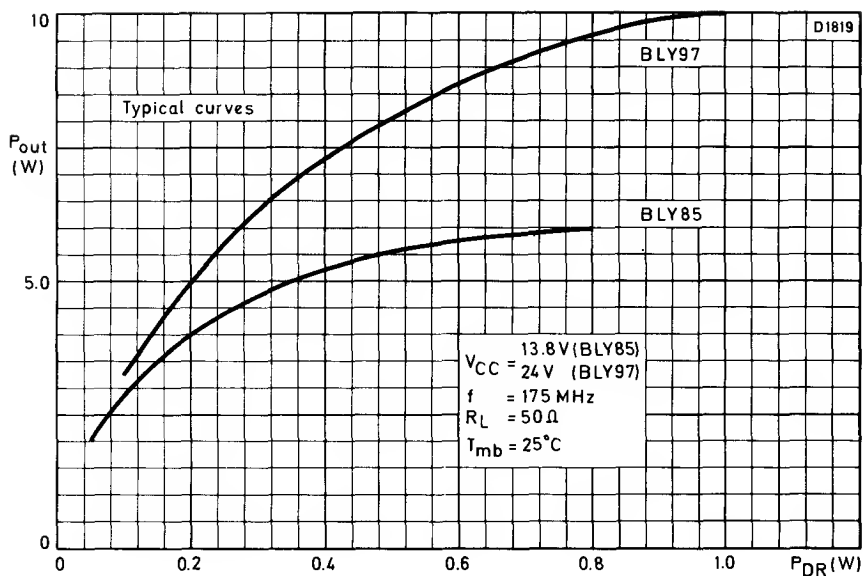
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N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY85
BLY97



Mullard



N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A

N-P-N epitaxial planar transistor intended for use in class A, B and C operated mobile, industrial and military transmitters with a supply voltage of 13.5 V. The transistor is resistance stabilized. Every transistor is tested under severe load mismatch conditions with a supply overvoltage to 16.5 V. It has a $\frac{1}{4}$ " capstan envelope with a moulded cap. All leads are isolated from the stud.

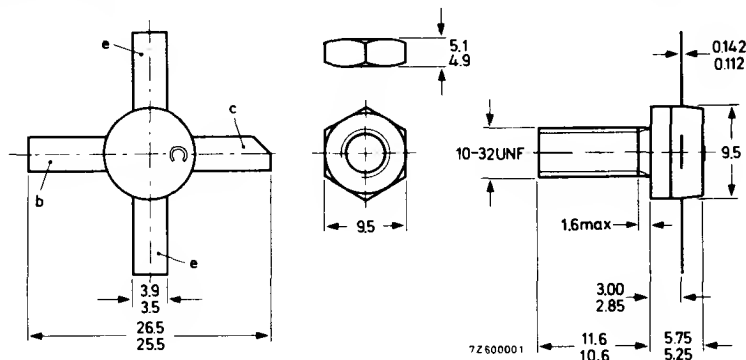
QUICK REFERENCE DATA

R. F. performance up to $T_{mb} = 25^{\circ}\text{C}$ in an unneutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mA/V)
c. w.	13.5	175	< 6.25	25	< 2.64	> 6	> 70	$1.7+j1.4$	$209+j13.7$

MECHANICAL DATA

Dimensions in mm



Torque on nut: min. 15 kg cm
(1.5 Newton metres)
max. 17 kg cm
(1.7 Newton metres)

Diameter of clearance hole in heatsink: max. 5.0 mm.

Mounting hole to have no burrs at either end. De-burring must leave surface flat; do not chamfer or countersink either end of hole.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Collector-base voltage (open emitter)
peak value

V_{CBOM} max. 36 V

Collector-emitter voltage (open base)

V_{CEO} max. 18 V

Emitter-base voltage (open collector)

V_{EBO} max. 4 V

Currents

Collector current (average)

$I_{C(AV)}$ max. 5 A

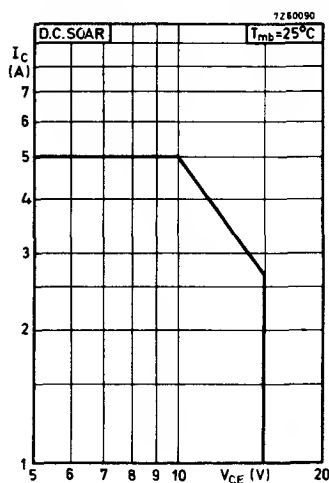
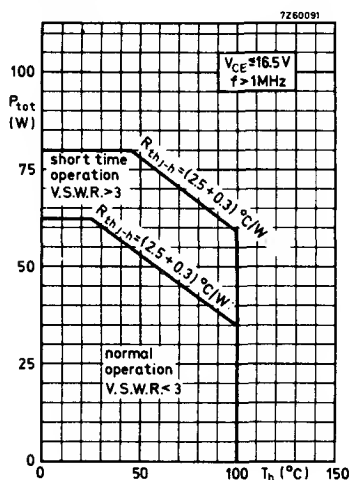
Collector current (peak value) $f > 1$ MHz

I_{CM} max. 10 A

Power dissipation

Total power dissipation up to $T_{mb} = 25^\circ\text{C}$
 $f > 1$ MHz

P_{tot} max. 70 W



Temperature

Storage temperature

T_{stg} -30 to +200 $^\circ\text{C}$

Operating junction temperature

T_j max. 200 $^\circ\text{C}$

THERMAL RESISTANCE

From junction to mounting base

$R_{th\ j-mb} = 2.5$ $^\circ\text{C/W}$

From mounting base to heatsink

$R_{th\ mb-h} = 0.3$ $^\circ\text{C/W}$

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A

CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

Breakdown voltages

Collector-base voltage open emitter, $I_C = 50\text{ mA}$	$V_{(BR)CBO}$	>	36	V
Collector-emitter voltage open base, $I_C = 50\text{ mA}$	$V_{(BR)CEO}$	>	18	V
Emitter-base voltage open collector; $I_E = 10\text{ mA}$	$V_{(BR)EBO}$	>	4	V

Transient energy

$L = 25\text{ mH}$; $f = 50\text{ Hz}$

open base	E	>	8	mWs
$-V_{BE} = 1.5\text{ V}$; $R_{BE} = 33\ \Omega$	E	>	8	mWs

D.C. current gain

$I_C = 1\text{ A}$; $V_{CE} = 5\text{ V}$	h_{FE}	typ.	50
		10 to	120

Transition frequency

$I_C = 4\text{ A}$; $V_{CE} = 10\text{ V}$	f_T	typ.	650	MHz
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Collector capacitance at $f = 1\text{ MHz}$

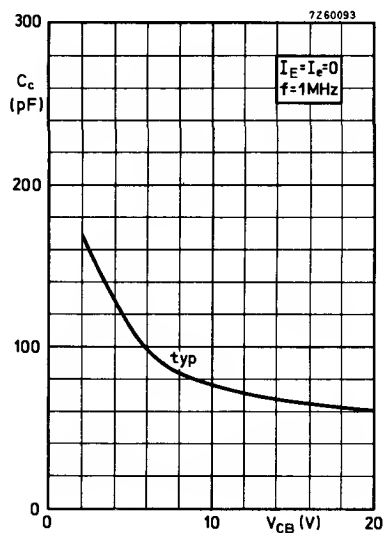
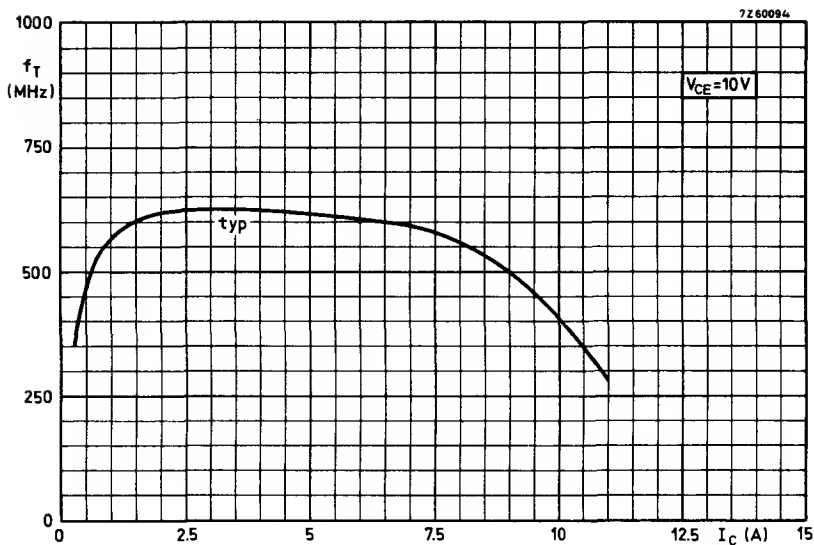
$I_E = I_C = 0$; $V_{CB} = 15\text{ V}$	C_c	typ.	65	pF
		<	90	pF

Feedback capacitance at $f = 1\text{ MHz}$

$I_C = 100\text{ mA}$; $V_{CE} = 15\text{ V}$	$-C_{re}$	typ.	41	pF
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Collector-stud capacitance

	C_{cs}	typ.	2	pF
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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

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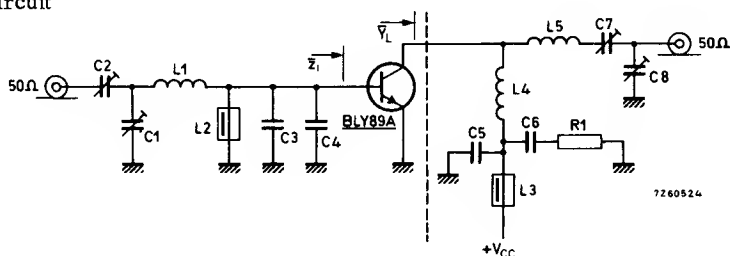
APPLICATION INFORMATION

R. F. performance in c. w. operation (unneutralised common-emitter class B circuit)

$V_{CC} = 13.5 \text{ V}$; T_{mb} up to 25°C

f(MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{z}_1 (Ω)	\bar{Y}_L (mA/V)
175	< 6.25	25	< 2.64	> 6	> 70	$1.7+j1.4$	$209+j13.7$

Test circuit



C1 = 4 to 44 pF film dielectric trimmer

C2 = 2 to 22 pF film dielectric trimmer

C3 = C4 = 47 pF ceramic

C5 = 100 pF ceramic

C6 = 150 nF polyester

C7 = 4 to 104 pF film dielectric trimmer

C8 = 4 to 64 pF film dielectric trimmer

L1 = 0.5 turn enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2 x 6 mm

L2 = L3 = ferroxcube choke

L4 = 3.5 turns closely wound enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2 x 6 mm

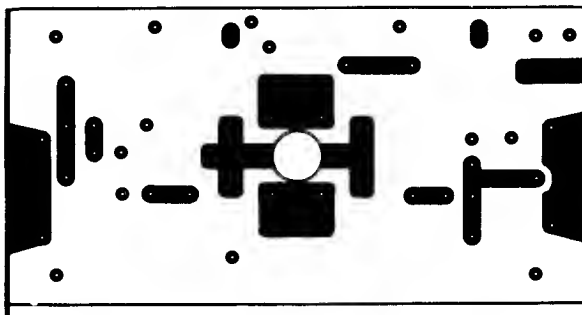
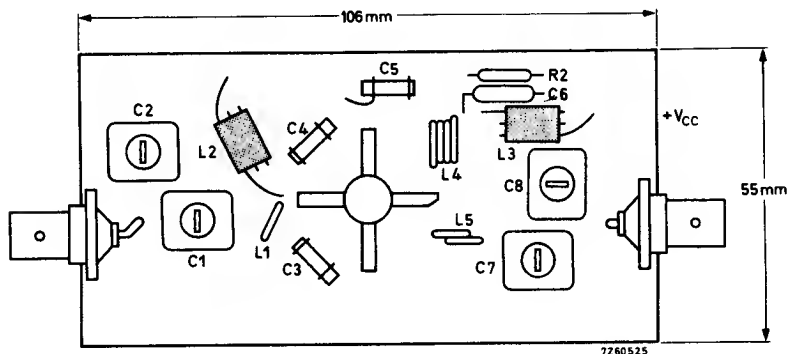
L5 = 1 turn enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2 x 6 mm

R1 = 10 Ω carbon

Component lay-out for 175 MHz see page 6.

APPLICATION INFORMATION (continued)

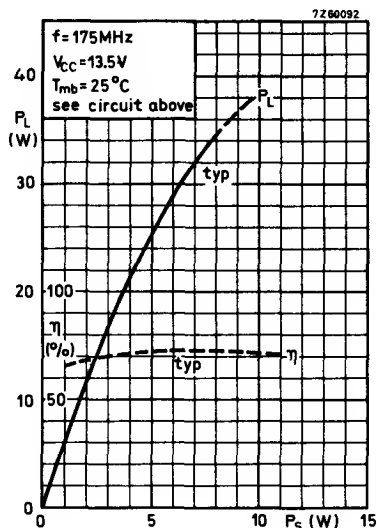
Component lay-out and printed circuit board for 175 MHz test circuit.



The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A



CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
 MULLARD LIMITED
 2, NEW ROAD, MITCHAM JUNCTION
 SURREY, CR4 4XY.

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY90

N-P-N silicon planar epitaxial v.h.f. power transistor for use in class A, B and C operated mobile transmitters with a 12.5V supply. It can withstand severe load mismatch conditions with a supply overvoltage up to 15V.

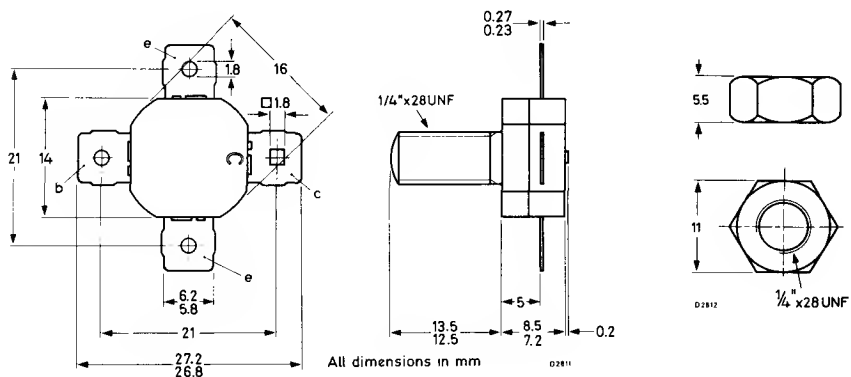
The BLY90 has a plastic encapsulated stripline package with all leads isolated from the stud.

QUICK REFERENCE DATA

R.F. performance in an un-neutralised common-emitter class B circuit,
 $T_h \leq 25^{\circ}\text{C}$.

Operation	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mA/V)
c. w.	12.5	175	<15.8	50	<5.33	>5.0	>75	$1.3 + j1.6$	$270 + j160$

OUTLINE AND DIMENSIONS



Torque on nut: min. 23kg cm (2.3N m), max. 27kg cm (2.7N m)

Diameter of clearance hole in heatsink: max. 6.5mm

Note: Do not chamfer the edges of the mounting hole when removing burrs.

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RATINGS

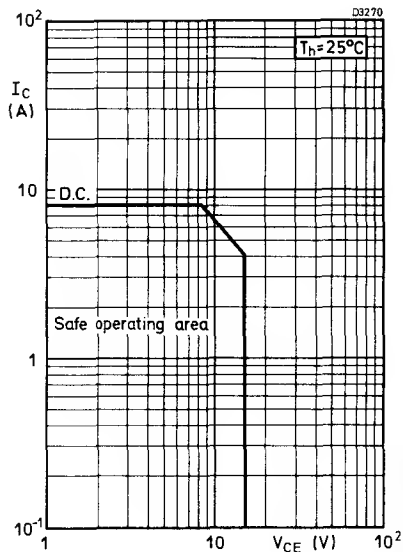
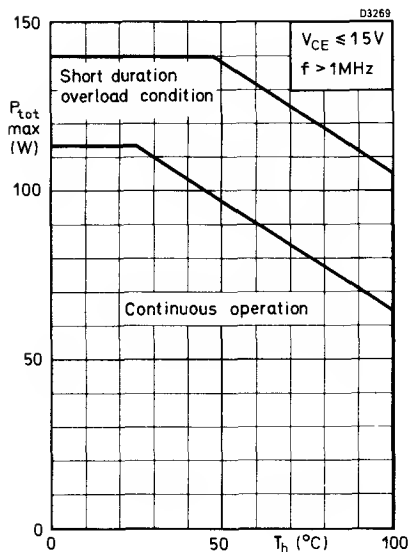
Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	8.0	A
I_{CM} max. ($f > 1\text{MHz}$)	20	A
P_{tot} max. ($f > 1\text{MHz}$, $T_h \leq 25^\circ\text{C}$)	130	W

Temperature

T_{stg}	-65 to +200	$^\circ\text{C}$
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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

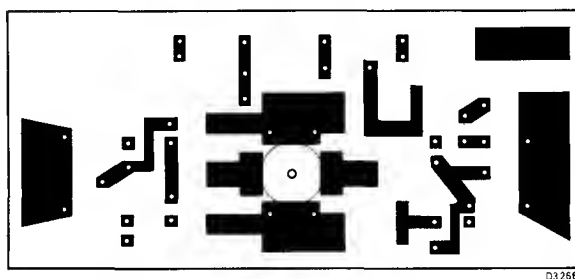
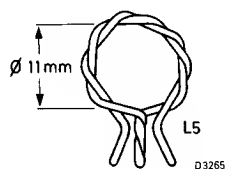
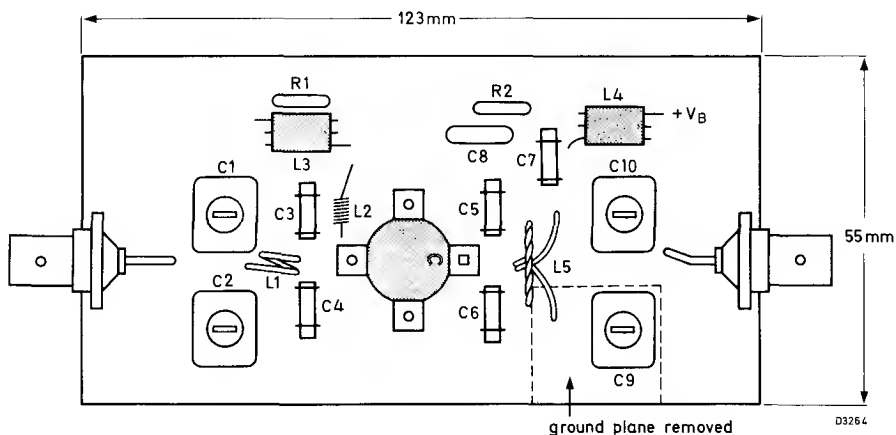
BLY90

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter, $I_C = 100\text{mA}$	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage open base, $I_C = 100\text{mA}$	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector, $I_E = 25\text{mA}$	4.0	-	-	V
E	Transient energy $L = 25\text{mH}$, $f = 50\text{Hz}$				
	open base	8.0	-	-	mWs
	$-V_{BE} = 1.5\text{V}$, $R_{BE} = 33\Omega$	8.0	-	-	mWs
h_{FE}	Static forward current transfer ratio $I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$	10	50	-	
f_T	Transition frequency $I_C = 6.0\text{A}$, $V_{CE} = 10\text{V}$	-	550	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 15\text{V}$, $f = 1\text{MHz}$	-	130	160	pF
$-C_{re}$	Feedback capacitance $I_C = 200\text{mA}$, $V_{CE} = 15\text{V}$	-	82	-	pF
C_{cs}	Collector-stud capacitance	-	3.5	-	pF

APPLICATION INFORMATION (contd.)

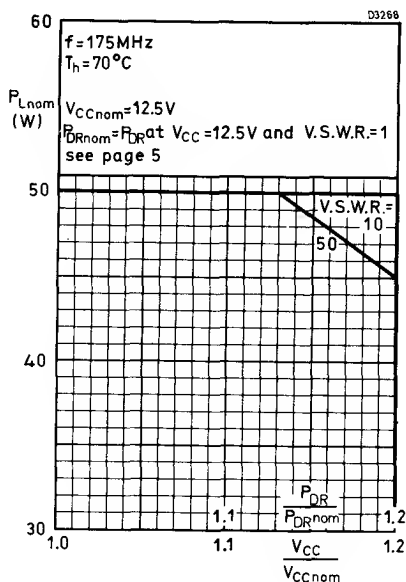
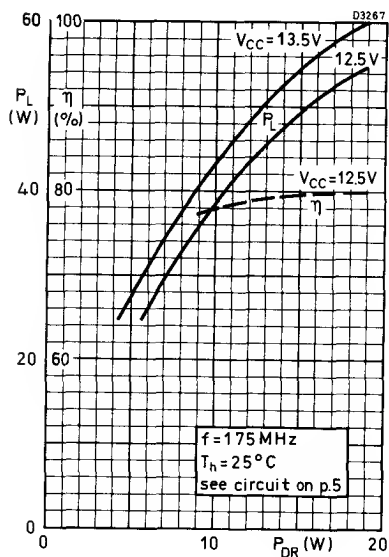
Component layout and printed circuit board for 175MHz test circuit



The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY90



INDICATED LOAD POWER
AS A FUNCTION OF OVERLOAD
(see note below)

NOTE

The transistor is developed for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 50 watts load power in the circuit on page 5, and subsequently subjected to various voltage overloads and mismatch conditions with V.S.W.R. up to 50:1 at a heatsink temperature of 70°C . This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and V.S.W.R. in the recommended circuit.

CAUTION

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any authority or licence for the utilisation of any patented feature

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A

N-P-N epitaxial planar transistor intended for use in class A, B and C operated mobile, industrial and military transmitters with a supply voltage of 28 V. The transistor is resistance stabilized. Every transistor is tested under severe load mismatch conditions. It has a $\frac{1}{4}$ " capstan envelope with a moulded cap. All leads are isolated from the stud.

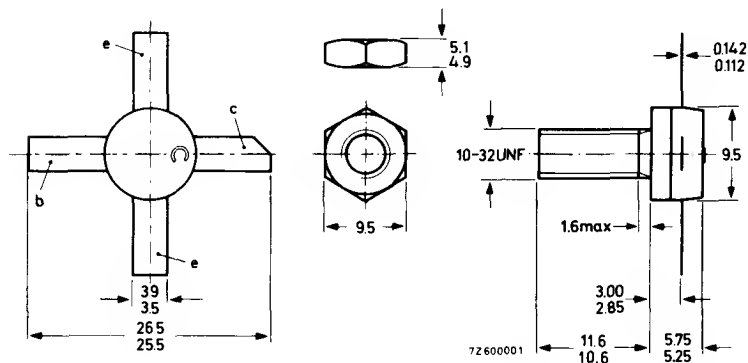
QUICK REFERENCE DATA

R.F. performance up to $T_{mb} = 25^{\circ}\text{C}$ in an unneutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{Z}_i (Ω)	\bar{Y}_L (mA/V)
c. w.	28	175	< 3.1	25	< 1.5	> 9	> 60	1.0+j1.2	57.7-j52.7

MECHANICAL DATA

Dimensions in mm



Torque on nut: min. 15 kg cm
(1.5 Newton metres)
max. 17 kg cm
(1.7 Newton metres)

Diameter of clearance hole in heatsink: max.
5.0 mm.

Mounting hole to have no burrs at either end.
De-burring must leave surface flat; do not
chamfer or countersink either end of hole.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Collector-base voltage (open emitter)
peak value

V_{CBOM} max. 65 V

Collector-emitter voltage (open base)

V_{CEO} max. 36 V

Emitter-base voltage (open collector)

V_{EBO} max. 4 V

Currents

Collector current (average)

$I_{C(AV)}$ max. 3 A

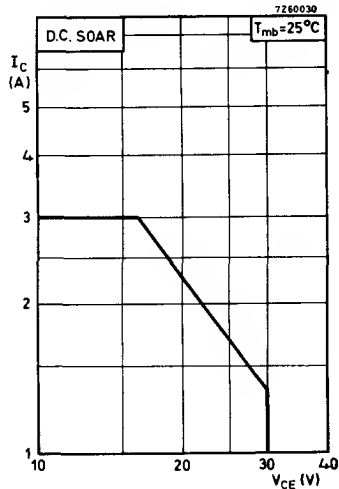
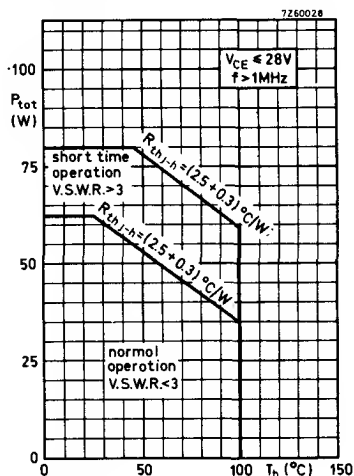
Collector current (peak value) $f > 1$ MHz

I_{CM} max. 9 A

Power dissipation

Total power dissipation up to $T_{mb} = 25^{\circ}\text{C}$
 $f > 1$ MHz

P_{tot} max. 70 W



Temperature

Storage temperature

T_{stg} -30 to $+200^{\circ}\text{C}$

Operating junction temperature

T_j max. 200°C

THERMAL RESISTANCE

From junction to mounting base

$R_{th j-mb} = 2.5^{\circ}\text{C/W}$

From mounting base to heatsink

$R_{th mb-h} = 0.3^{\circ}\text{C/W}$

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A

CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

Breakdown voltages

Collector-base voltage open emitter, $I_C = 50\text{ mA}$	$V_{(BR)CBO}$	>	65 V
Collector-emitter voltage open base, $I_C = 50\text{ mA}$	$V_{(BR)CEO}$	>	36 V
Emitter-base voltage open collector; $I_E = 10\text{ mA}$	$V_{(BR)EBO}$	>	4 V

Transient energy

$L = 25\text{ mH}$; $f = 50\text{ Hz}$

open base	E	>	8 mWs
$-V_{BE} = 1.5\text{ V}$; $R_{BE} = 33\ \Omega$	E	>	8 mWs

D.C. current gain

$I_C = 1\text{ A}$; $V_{CE} = 5\text{ V}$	h_{FE}	typ. 50 10 to 120
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Transition frequency

$I_C = 3\text{ A}$; $V_{CE} = 20\text{ V}$	f_T	typ. 500 MHz
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Collector capacitance at $f = 1\text{ MHz}$

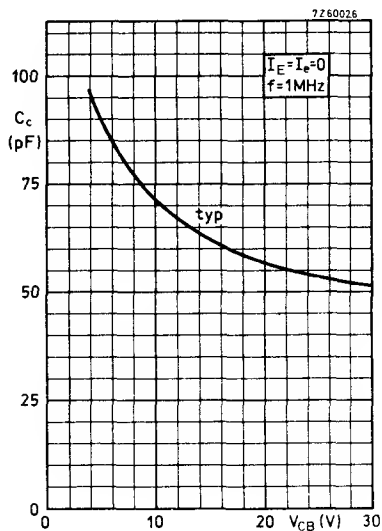
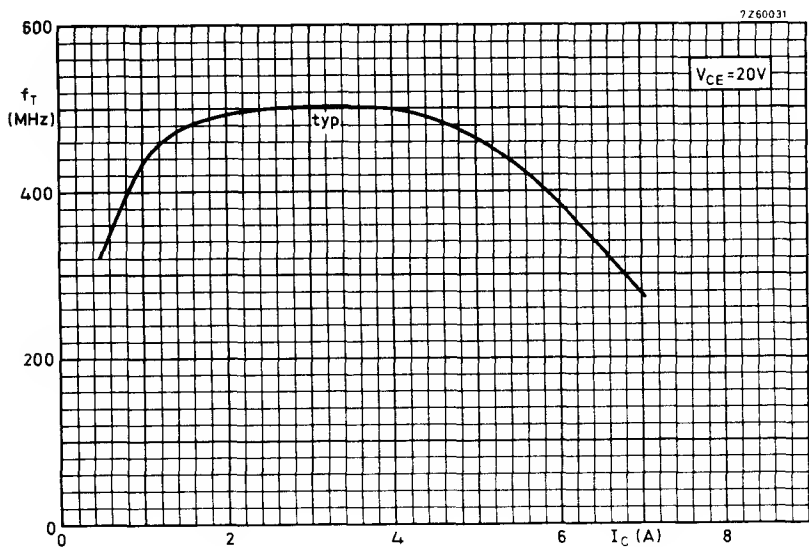
$I_E = I_e = 0$; $V_{CB} = 30\text{ V}$	C_c	typ. 50 pF < 65 pF
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Feedback capacitance at $f = 1\text{ MHz}$

$I_C = 100\text{ mA}$; $V_{CE} = 30\text{ V}$	$-C_{re}$	typ. 31 pF
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Collector-stud capacitance

	C_{cs}	typ. 2 pF
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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A

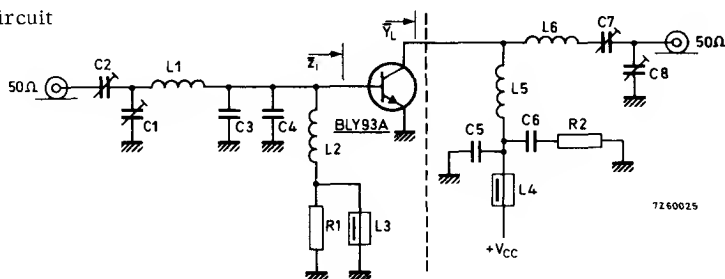
APPLICATION INFORMATION

R. F. performance in c. w. operation (unneutralised common-emitter class B circuit)

$$V_{CC} = 28 \text{ V}; T_{mb} = 25^{\circ}\text{C}$$

f(MHz)	P _S (W)	P _L (W)	I _C (A)	G _p (dB)	η (%)	\bar{Z}_i (Ω)	\bar{Y}_L (mA/V)
175	< 3.1	25	< 1.5	> 9	> 60	1.0 + j1.2	57.7-j52.7

Test circuit



C1 = 4 to 44 pF film dielectric trimmer

C2 = 2 to 22 pF film dielectric trimmer

C3 = C4 = 47 pF ceramic

C5 = 100 pF ceramic

C6 = 150 nF polyester

C7 = 4 to 104 pF film dielectric trimmer

C8 = 4 to 64 pF film dielectric trimmer

L1 = 0.5 turn enamelled Cu wire (1.5 mm); int.diam.6 mm; leads 2 x 6 mm

L2 = 6 turns closely wound enamelled Cu wire (0.7 mm); int.diam.4 mm;
leads 2 x 4 mm

L3 = L4 = ferroxcube choke

L5 = 3.5 turns enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2 x 6 mm

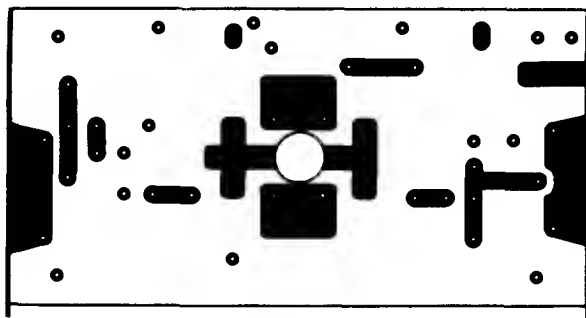
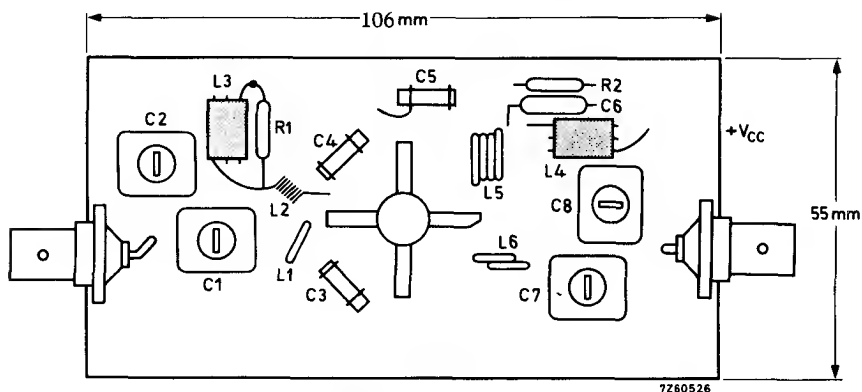
L6 = 1.5 turns enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2 x 6 mm

R1 = R2 = 10 Ω carbon

Component lay-out for 175 MHz see page 6.

APPLICATION INFORMATION (continued)

Component lay-out and printed circuit board for 175 MHz test circuit.

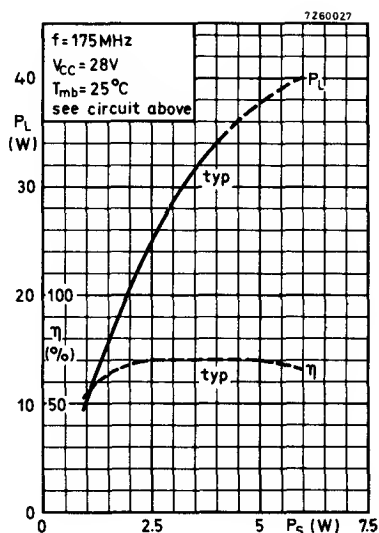


The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.

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N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A



CAUTION

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 SURREY, CR4 4XY.

Mullard

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY94

Silicon n-p-n planar epitaxial transistor intended for use in class A, Band C operated mobile transmitters with a 28V supply. It is designed to withstand severe load mismatch conditions.

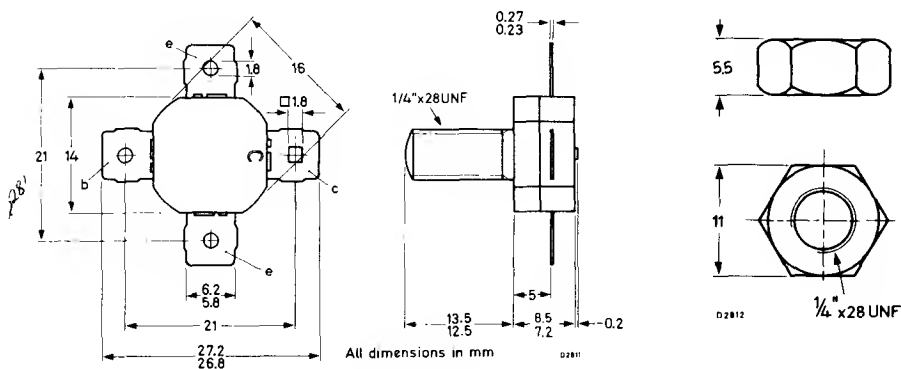
The BLY94 is in a plastic-encapsulated stripline package with all leads isolated from the stud.

QUICK REFERENCE DATA

R. F. performance up to $T_h = 25^\circ\text{C}$ in an un-neutralised common-emitter class B circuit.

Operation	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	\bar{z}_i (Ω)	\bar{Y}_L (mA/V)
c.w.	28	175	< 10	50	< 2.75	> 7	> 65	$0.7 + j1.45$	$120 - j70$

OUTLINE AND DIMENSIONS



Torque on nut: min. 23 kg cm (2.3 N m)
max. 27 kg cm (2.7 N m)

Diameter of clearance hole in heatsink: max. 6.5 mm

Note: Do not chamfer the edges of the mounting holes when removing burrs.

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

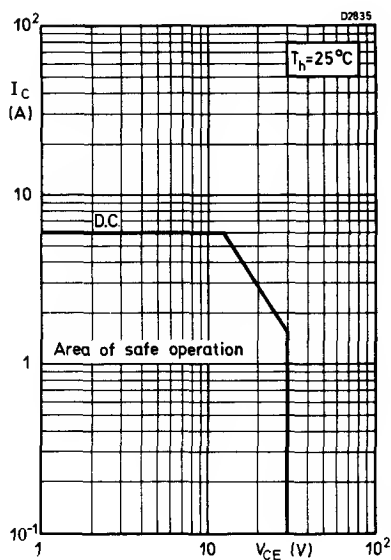
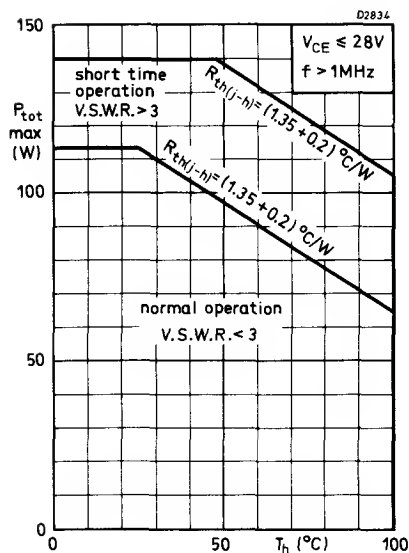
V_{CBOM} max.	65	V
V_{CEO} max.	36	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	6.0	A
I_{CM} max. ($f > 1\text{MHz}$)	12	A
P_{tot} max. ($T_h \leq 25^\circ\text{C}$, $f > 1\text{MHz}$)	130	W

Temperature

T_{stg}	-65 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$	1.35	degC/W
$R_{th(mb-h)}$	0.2	degC/W



N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

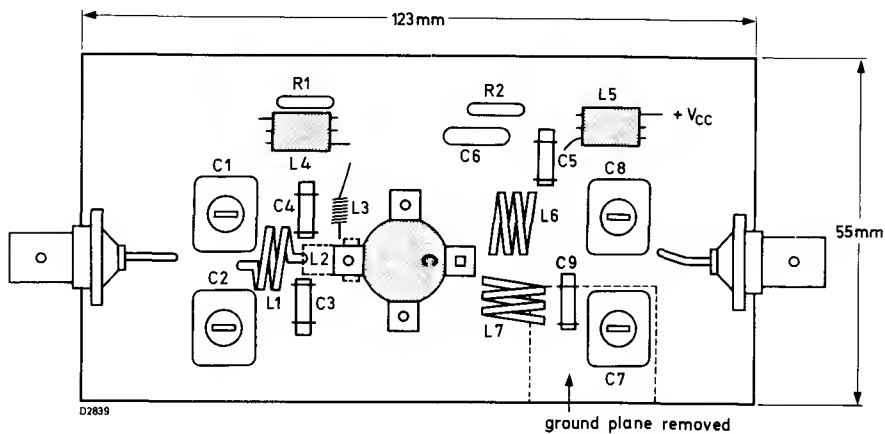
BLY94

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter, $I_C = 100\text{mA}$	65	-	-
				V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage open base, $I_C = 100\text{mA}$	36	-	-
				V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector, $I_E = 25\text{mA}$	4.0	-	-
				V
E	Transient energy $L = 25\text{mH}$, $f = 50\text{Hz}$			
	open base	8.0	-	-
				mWs
	$-V_{BE} = 1.5\text{V}$, $R_{BE} = 33\Omega$	8.0	-	-
				mWs
h_{FE}	Static forward current transfer ratio			
	$I_C = 1.0\text{A}$, $V_{CE} = 5\text{V}$	10	-	120
f_T	Transition frequency $I_C = 6.0\text{A}$, $V_{CE} = 20\text{V}$	-	500	-
				MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 30\text{V}$, $f = 1.0\text{MHz}$	-	75	130
				pF
$-C_{re}$	Feedback capacitance $I_C = 100\text{mA}$, $V_{CE} = 30\text{V}$	-	47	-
				pF
C_{cs}	Collector-stud capacitance	-	3.5	-
				pF

APPLICATION INFORMATION (contd.)

Component layout on a printed circuit board for 175MHz test circuit

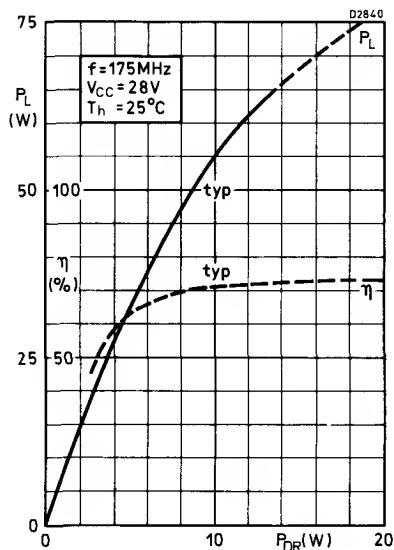


The underside of the epoxy fibre-glass board is completely metallised and serves as earth.

Earth connections are made by means of hollow rivets.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY94



CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
2 NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.

Mullard

**N-P-N SILICON PLANAR
V.H.F. TRANSISTOR**

BLY97

For details see data sheet for type BLY85

For use as a PROGRAMMABLE UNIJUNCTION TRANSISTOR

The BRY39 is a planar p-n-p-n trigger device in a TO-72 metal envelope, intended for use in switching applications such as motor control, oscillators, relay replacement, timers, pulse shaper, trigger device, etc.

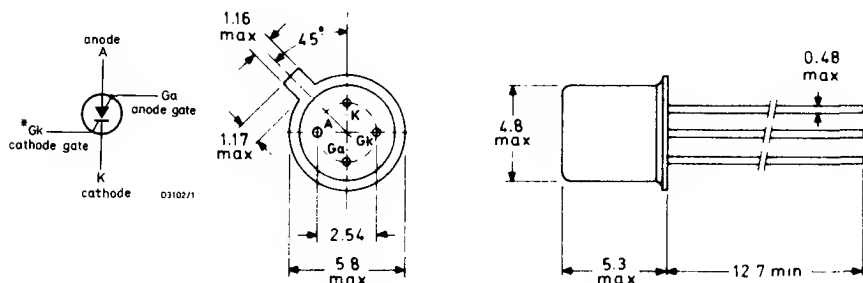
See also data on BRY39 as a Silicon Controlled Switch and as a Thyristor Tetrode.

QUICK REFERENCE DATA

V_{GaA} max.	Anode gate to anode voltage	70	V
I_A max.	Anode current, d.c. ($T_{case} \leq 85^\circ C$)	250	mA
T_j max.	Junction temperature	150	$^\circ C$
I_P	Peak point current ($V_S = 10V$, $R_G = 10k\Omega$)	<5.0	μA
I_V	Valley point current ($V_S = 10V$, $R_G = 10k\Omega$)	>50	μA

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



All dimensions in mm

03073

Anode gate connected to case

*For the application of the BRY39 as a programmable unijunction transistor, cathode gate is not used.

Accessories available: 56246 (distance disc) and 56263 (cooling clip)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{GaA} max.	Anode gate to anode voltage	70	V
I_A max.	Anode current (d. c.) $T_{amb} \leq 25^{\circ}C$	175	mA
	$T_{case} \leq 85^{\circ}C$	250	mA
I_{ARM} max.	Repetitive peak anode current $t = 10\mu s, d = 0.01$	2.5	A
I_{ASM} max.	Non-repetitive peak anode current $t = 10\mu s, T_j = 150^{\circ}C$	3.0	A
$\frac{dI_A}{dt}$	Rate of rise of anode current up to $I_A = 2.5A$	20	A/ μs

Temperature

T_{stg}	Storage temperature	-65 to +200	$^{\circ}C$
T_j max.	Junction temperature	150	$^{\circ}C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance from junction to ambient, in free air	0.45	$^{\circ}C/mW$
$R_{th(j-case)}$	Thermal resistance from junction to case	0.15	$^{\circ}C/mW$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_P	Peak point current				
	$V_S = 10V, R_G = 10k\Omega$	-	-	5.0	μA
	$V_S = 10V, R_G = 1M\Omega$	-	-	1.0	μA
I_V	Valley point current				
	$V_S = 10V, R_G = 10k\Omega$	50	-	-	μA
	$V_S = 10V, R_G = 1M\Omega$	-	-	50	μA

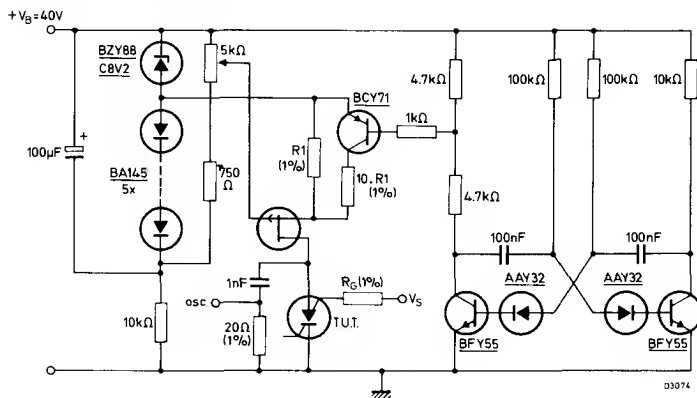
SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

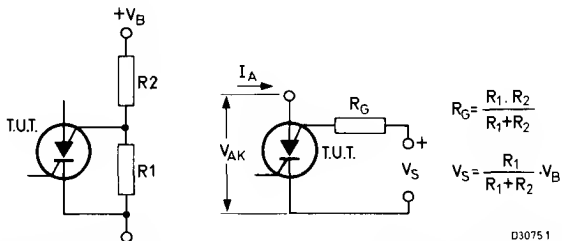
ELECTRICAL CHARACTERISTICS (contd.)

Practical test circuit

- (1) Remove BCY71 for measurement of I_p
- (2) The value of R_1 depends on the voltage range of the voltmeter used.



Equivalent test circuit

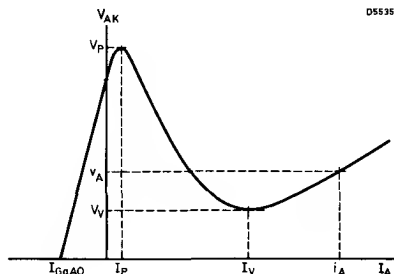


BRY39 with "program"
resistors R1 and R2

Equivalent test circuit
for characteristics testing

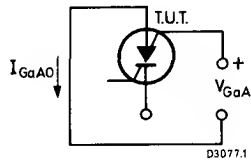
Offset voltage (see graph on page 6)

$$V_{\text{offset}} = V_P - V_S \quad (I_A = 0)$$

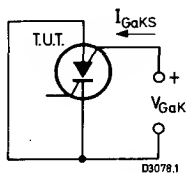


ELECTRICAL CHARACTERISTICS (contd.)

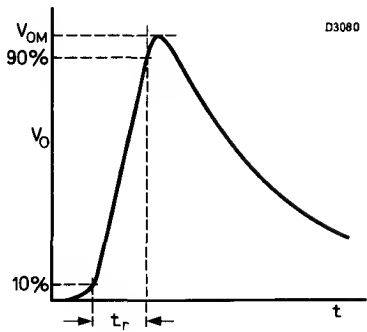
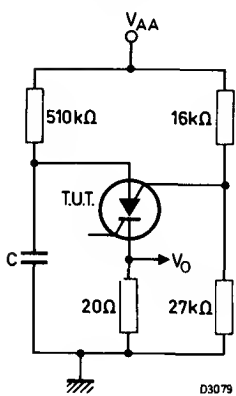
		Min.	Typ.	Max.	
I_{GaAO}	Anode gate to anode leakage current				
	$I_K = 0, V_{GaA} = 70V$	-	-	10	nA



I_{GaKS}	Anode gate to cathode leakage current				
	$V_{AK} = 0, V_{GaK} = 70V$	-	-	100	nA

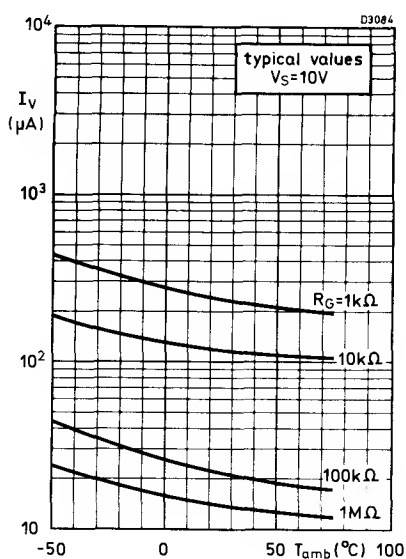
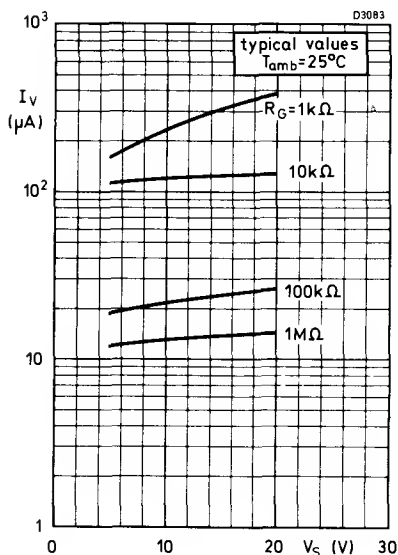
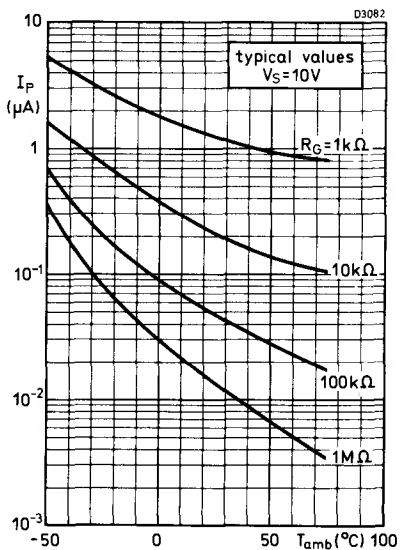
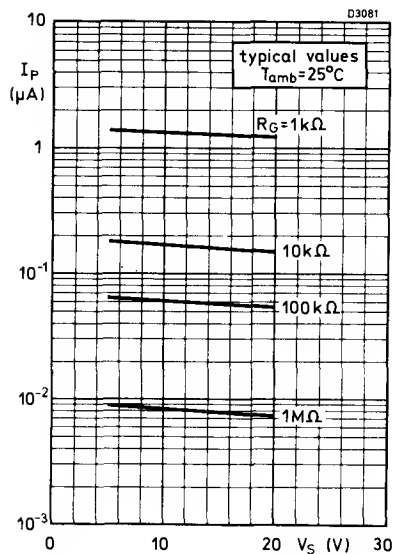


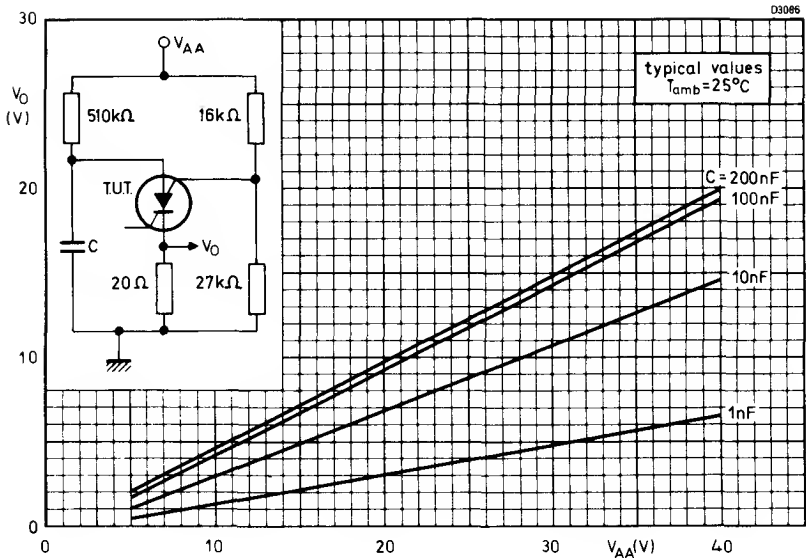
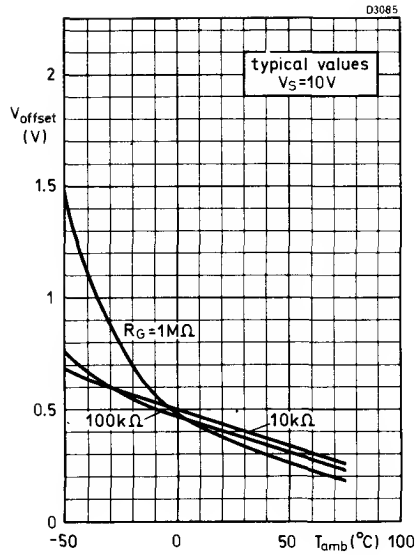
V_A	Anode voltage				
	$I_A = 100mA$	-	-	1.4	V
V_{OM}	Peak output voltage				
	$V_{AA} = 20V, C = 0.2\mu F$	6.0	-	-	V
t_r	Rise time				
	$V_{AA} = 20V, C = 10nF$	-	-	80	ns



SILICON P-N-P-N PLANAR TRANSISTOR

BRY39





SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

For use as a SILICON CONTROLLED SWITCH

The BRY39 is a silicon planar p-n-p-n switch in a TO-72 metal envelope, intended as a driver for numerical indicator tubes and other switching applications. It is an integrated pnp-npn transistor pair, with all electrodes accessible. See also data on BRY39 as a Thyristor Tetrode and as a Programmable Unijunction Transistor.

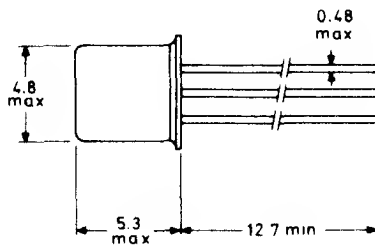
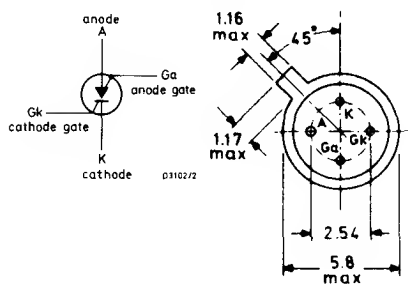
QUICK REFERENCE DATA

$-V_{EBO}$	Max. emitter-base voltage of the P-N-P transistor (open collector)	70	V
V_{CBO}	Max. collector-base voltage of the N-P-N transistor (open emitter)	70	V
$-I_{ERM}$	Max. repetitive peak emitter current	2.5	A
P_{tot}	Max. total dissipation ($T_{amb} \leq 25^{\circ}C$)	275	mW
T_j	Max. operating junction temperature	150	$^{\circ}C$
V_{AK}	Forward on-state voltage $I_A = 50mA$, $I_{Ga} = 0$, $R_{GkK} = 10k\Omega$	<1.4	V
I_H	Holding current $I_{Ga} = 10mA$, $-V_{BB} = 2.0V$, $R_{GkK} = 10k\Omega$	<1.0	mA
t_{on}	Turn-on time	<0.25	μs
t_q	Turn-off time	<5.0	μs

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3

J.E.D.E.C. TO-72



All dimensions in mm

D3073

The collector of the n-p-n transistor (anode gate) is connected to the case

Accessories available: 56246 (distance disc) and 56263 (cooling clip)

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	p-n-p	n-p-n	
V_{CBO} max. (open emitter)	-70	70*	V
V_{CER} max. ($R_{BE} = 10k\Omega$)	-	70*	V
V_{CEO} max. (open base)	-70	-	V
V_{EBO} max. (open collector)	-70*	5.0†	V
I_E max. (d. c.)	175	-175	mA
I_{ERM} max. (repetitive peak value, $t_p = 10\mu s$, $d = 0.01$)	2.5	-2.5	A
I_C max. (d. c.)	-	175**	mA
I_{CM} max. (peak value)	-	175†	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	275		mW

Temperature

T_j max.	150	$^\circ C$
T_{stg} range	-65 to +200	$^\circ C$

THERMAL CHARACTERISTIC

R_{th} (j-amb)	0.45	$^\circ C/mW$
------------------	------	---------------

*In numerical indicator tube driver circuits higher voltages are allowed, provided the collector current does not exceed a d. c. value of 1.0mA.

†In numerical indicator tube driver circuits higher voltages are allowed during the discharge of a capacitor of a maximum value of 390pF, provided the charge does not exceed 50nC.

**Provided the I_E rating is not exceeded.

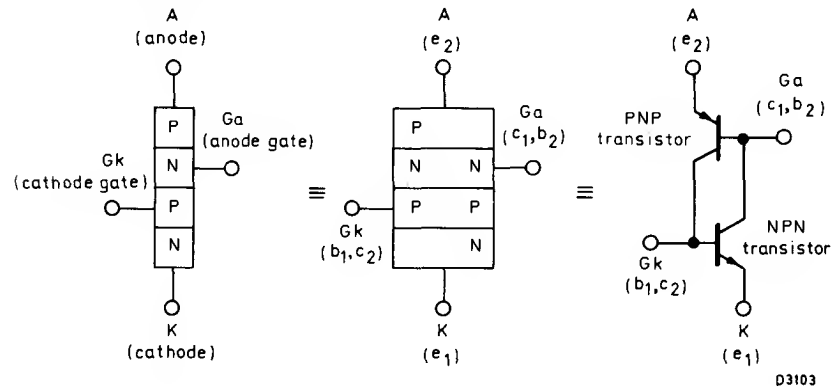
‡During switching on, the device can withstand the discharge of a capacitor of maximum value of 500pF. This capacitor is charged when the transistor is in cut-off condition, with a collector supply voltage of 160V and a series resistance of 100k Ω .

SILICON P-N-P-N PLANAR TRANSISTOR

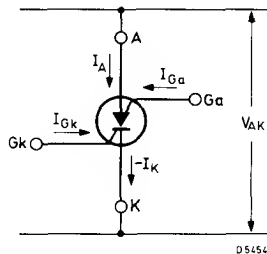
BRY39

SYMBOLS AND EQUIVALENT CIRCUITS

P-N-P-N structure and a two transistor equivalent circuit



Silicon controlled switch



ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

INDIVIDUAL N-P-N TRANSISTOR

Min. Typ. Max.

I_{CER}	Collector cut-off current				
	$V_{CE} = 70V, R_{BE} = 10k\Omega$	-	-	100	nA
	$V_{CE} = 70V, R_{BE} = 10k\Omega, T_j = 150^\circ\text{C}$	-	-	10	μA
I_{EBO}	Emitter cut-off current				
	$I_C = 0, V_{EB} = 5.0V, T_j = 150^\circ\text{C}$	-	-	10	μA

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ELECTRICAL CHARACTERISTICS (Contd.)

INDIVIDUAL N-P-N TRANSISTOR

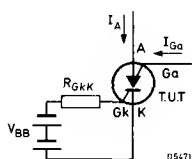
		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 10\text{mA}$, $I_B = 1.0\text{mA}$	-	-	500	mV
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 10\text{mA}$, $I_B = 1.0\text{mA}$	-	-	900	mV
h_{FE}	D.C. current gain $I_C = 10\text{mA}$, $V_{CE} = 2.0\text{V}$	50	-	-	
f_T	Transition frequency $I_C = 10\text{mA}$, $V_{CE} = 2.0\text{V}$	-	300	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 20\text{V}$	-	-	5.0	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 1.0\text{V}$	-	-	25	pF

INDIVIDUAL P-N-P TRANSISTOR

$-I_{CEO}$	Collector cut-off current $I_B = 0$, $-V_{CE} = 70\text{V}$, $T_j = 150^\circ\text{C}$	-	-	10	μA
$-I_{EBO}$	Emitter cut-off current $I_C = 0$, $-V_{EB} = 70\text{V}$, $T_j = 150^\circ\text{C}$	-	-	10	μA
h_{FE}	D.C. current gain $I_E = 1.0\text{mA}$, $V_{CB} = 0$	0.25	-	2.5	

COMBINED DEVICE

V_{AK}	Forward on-state voltage ($R_{GkK} = 10\text{k}\Omega$) $I_A = 50\text{mA}$, $I_{Ga} = 0$	-	-	1.4	V
	$I_A = 50\text{mA}$, $I_{Ga} = 0$, $T_j = -55^\circ\text{C}$	-	-	1.9	V
	$I_A = 1.0\text{mA}$, $I_{Ga} = 10\text{mA}$	-	-	1.2	V
I_H	Holding current $I_{Ga} = 10\text{mA}$, $-V_{BB} = 2.0\text{V}$, $R_{GkK} = 10\text{k}\Omega$	-	-	1.0	mA



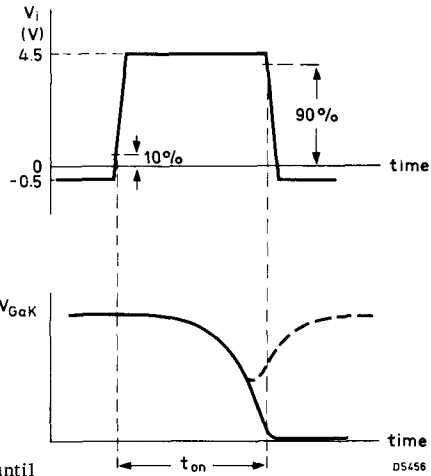
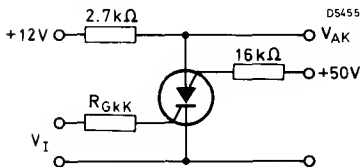
SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

ELECTRICAL CHARACTERISTICS (Contd.) ($T_j = 25^\circ\text{C}$ unless otherwise stated)

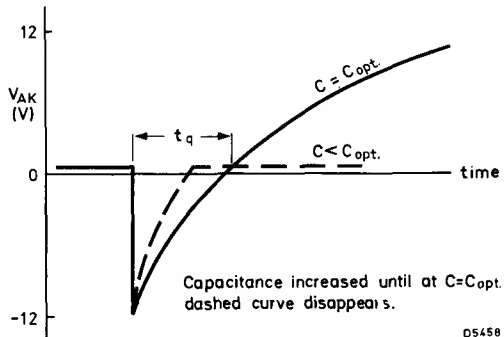
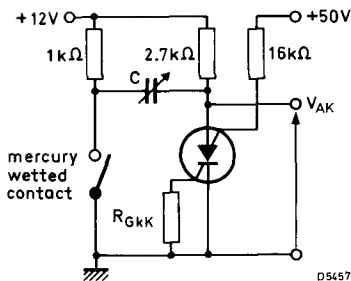
Switching times (see also page 7)

t_{on}	Turn-on time when switched from $-V_{GKK} = 0.5\text{V}$ to $+V_{GKK} = 4.5\text{V}$; $R_{GKK} = 1.0\text{k}\Omega$	< 0.25	μs
	$R_{GKK} = 10\text{k}\Omega$	< 1.5	μs



Pulse duration increased until
dashed curve disappears

t_q	Turn-off time		
	$R_{GKK} = 1.0\text{k}\Omega$	< 5.0	μs
	$R_{GKK} = 10\text{k}\Omega$	< 8.0	μs
	$R_{GKK} = 10\text{k}\Omega$, $T_j = 125^\circ\text{C}$		



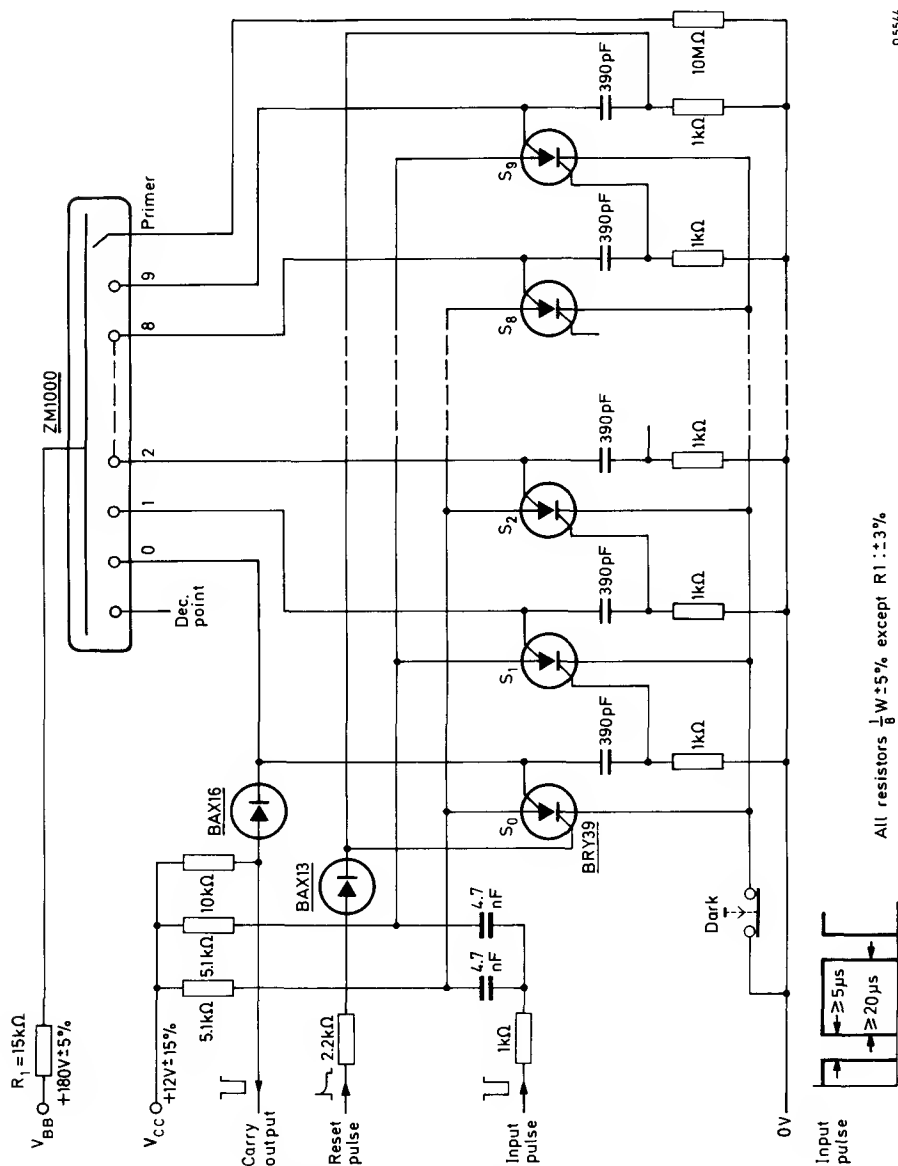
Capacitance increased until at $C = C_{opt.}$
dashed curve disappears.

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APPLICATION INFORMATION

Decade ring counter circuit with display ($f \leq 40\text{kHz}$)

Operating ambient temperature $T_{\text{amb}} = 0 \text{ to } 70^{\circ}\text{C}$



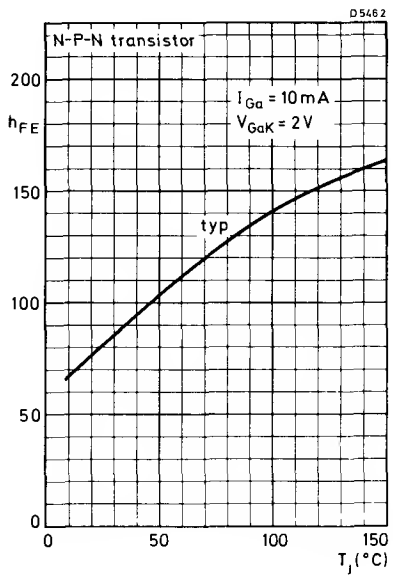
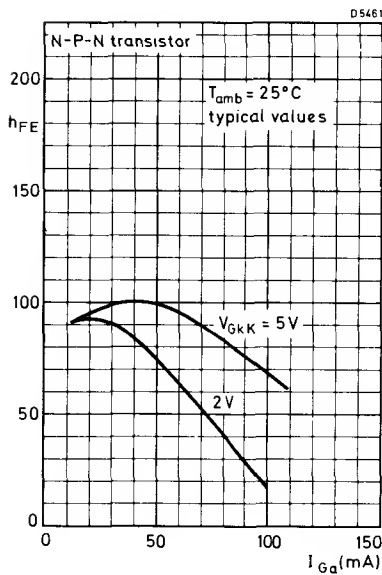
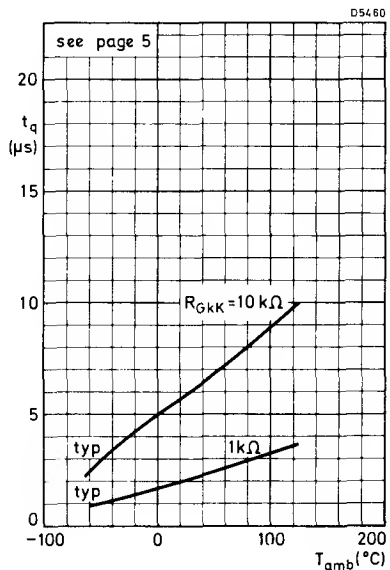
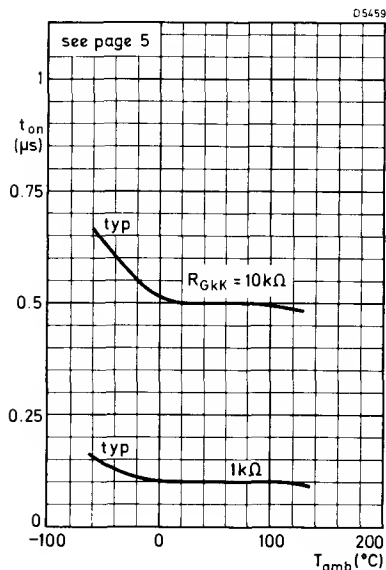
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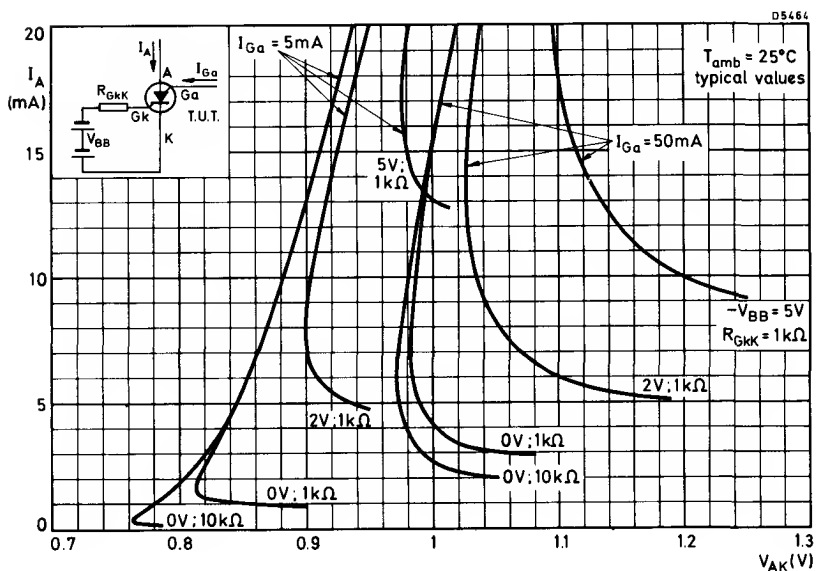
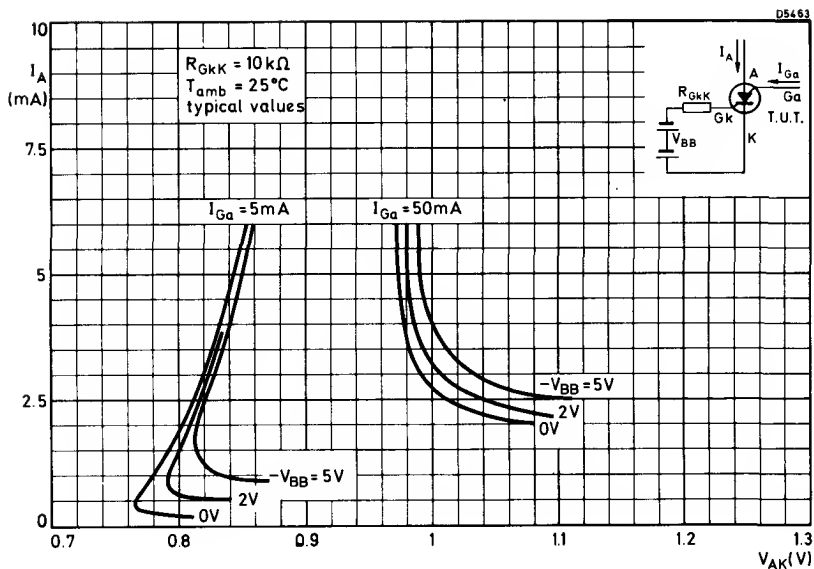
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SILICON P-N-P-N PLANAR TRANSISTOR

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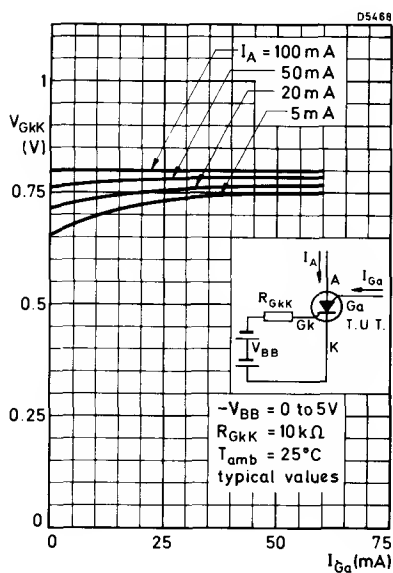
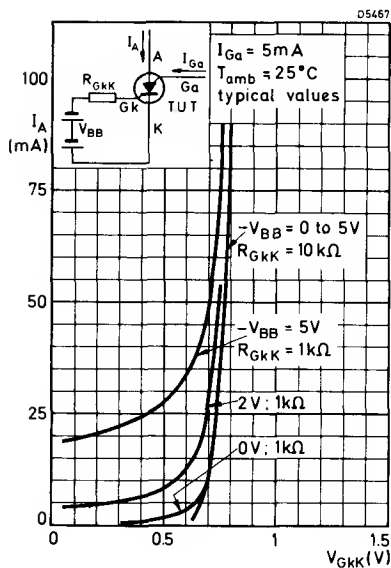
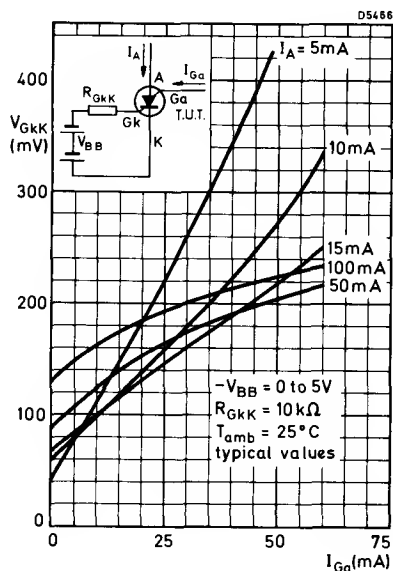
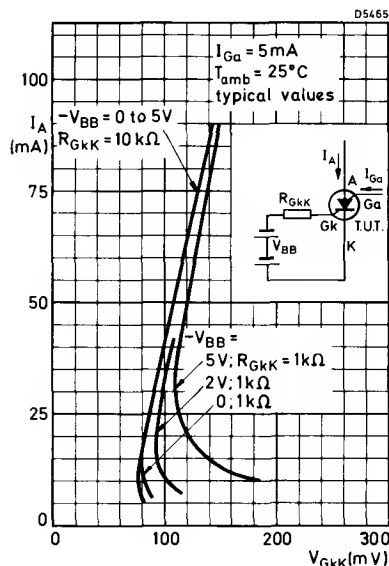


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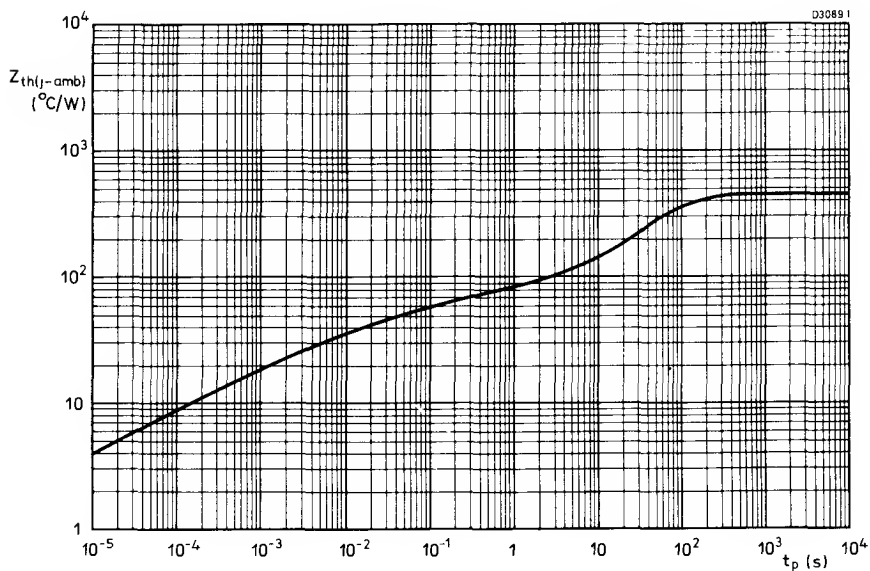
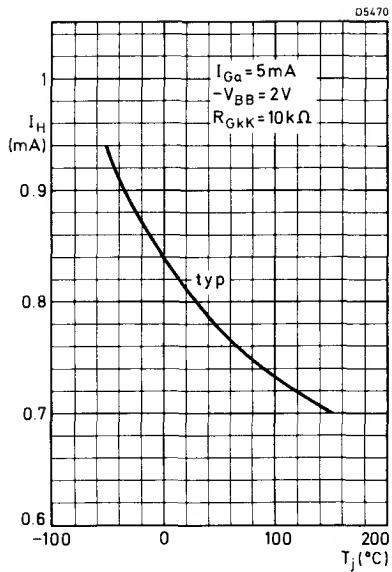
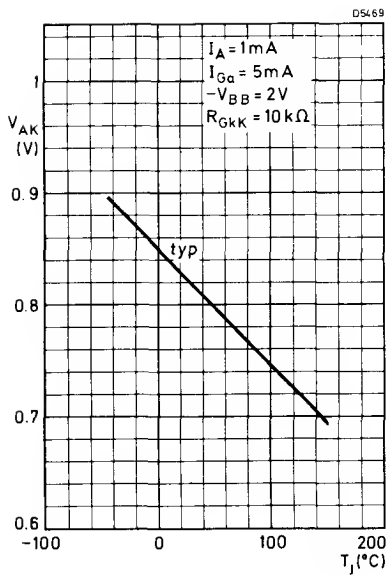


SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

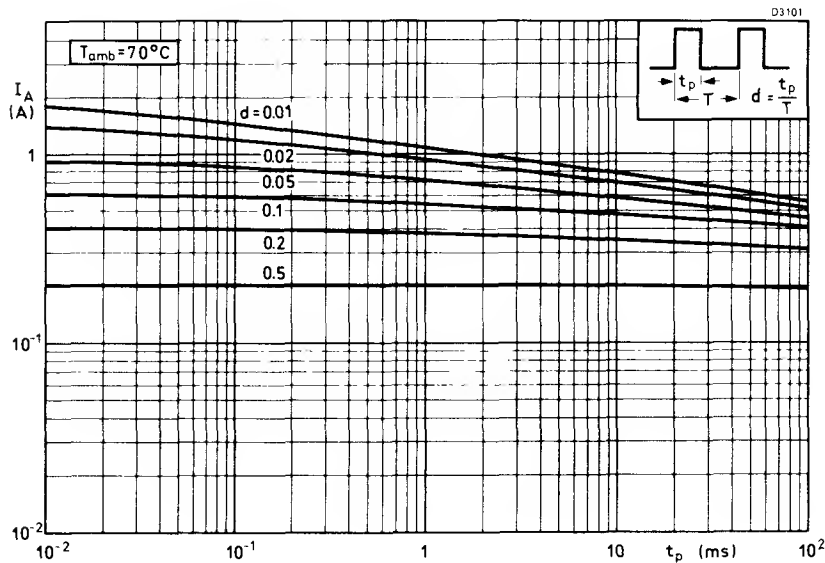
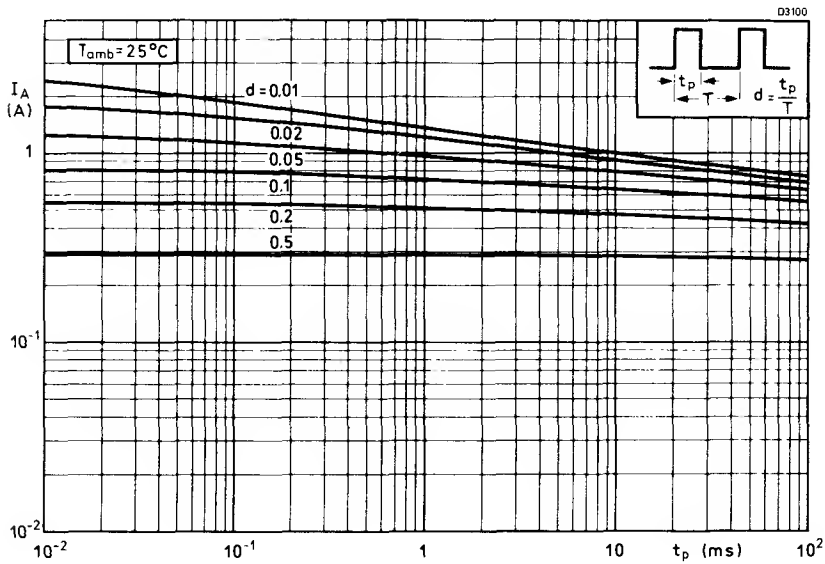


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SILICON P-N-P-N
PLANAR TRANSISTOR

BRY39



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SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

For use as a THYRISTOR TETRODE

The BRY39 is a planar p-n-p-n device in a TO-72 metal envelope, intended for use in switching applications such as relay and lamp drivers, sensing network for temperature, etc.

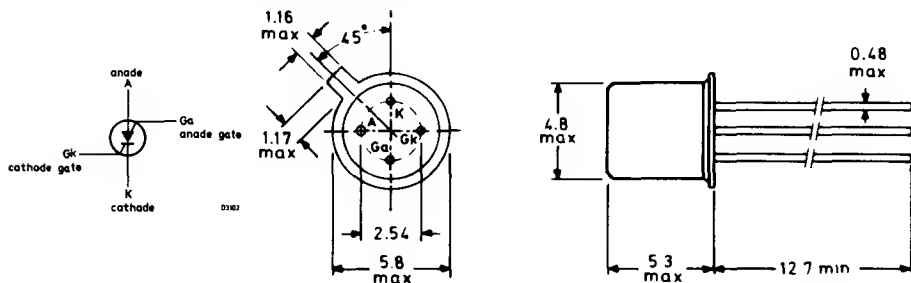
See also data on BRY39 as a Silicon Controlled Switch and as a Programmable Uni-junction Transistor.

QUICK REFERENCE DATA

$V_D = V_R$ max.	70	V
$V_{DRM} = V_{RRM}$ max.	70	V
I_T max. ($T_{case} \leq 85^\circ\text{C}$)	250	mA
I_{TSM} max. ($t = 10\mu\text{s}$, $T_j = 150^\circ\text{C}$)	3.0	A
T_j max.	150	$^\circ\text{C}$
$\frac{dI_T}{dt}$ max.	20	A/ μs

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



All dimensions in mm

D3073

Anode gate connected to case

Accessories available: 56246 (distance disc) and 56263 (cooling clip)

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RATINGS

Limiting values of operation according to the absolute maximum system.

Anode to cathode

$V_D = V_R$ max.	Continuous voltage	70*	V
$V_{DRM} = V_{RRM}$ max.	Repetitive peak voltage	70*	V
$V_{DSM} = V_{RSM}$ max.	Non-repetitive peak voltage	70*	V
I_T max.	On-state current, d. c.		
	$T_{amb} \leq 25^{\circ}\text{C}$	175	mA
	$T_{case} \leq 85^{\circ}\text{C}$	250	mA
I_{TRM} max.	Repetitive peak on-state current, $t = 10\mu\text{s}$, $d = 0.01$	2.5	A
I_{TSM} max.	Non-repetitive peak on-state current, $t = 10\mu\text{s}$, $T_j = 150^{\circ}\text{C}$ prior to surge	3.0	A
$\frac{dI_T}{dt}$ max.	Rate of rise of on-state current after triggering to $I_T = 2.5\text{A}$	20	A/ μs

Cathode gate to cathode

V_{GKM} max.	Reverse peak voltage	5.0	V
I_{GKM} max.	Forward peak current	100	mA

Anode gate to anode

V_{GaM}	Reverse peak voltage	70	V
I_{GaM}	Forward peak current	100	mA

Temperature

T_{stg}	Storage temperature	-65 to +200	$^{\circ}\text{C}$
T_j	Junction temperature	150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance from junction to ambient in free air	0.45	$^{\circ}\text{C}/\text{mW}$
$R_{th(j-case)}$	Thermal resistance from junction to case	0.15	$^{\circ}\text{C}/\text{mW}$

*These ratings apply for zero or negative bias on the cathode gate with respect to the cathode, and when a resistor $R \leq 10\text{k}\Omega$ is connected between cathode gate and cathode.

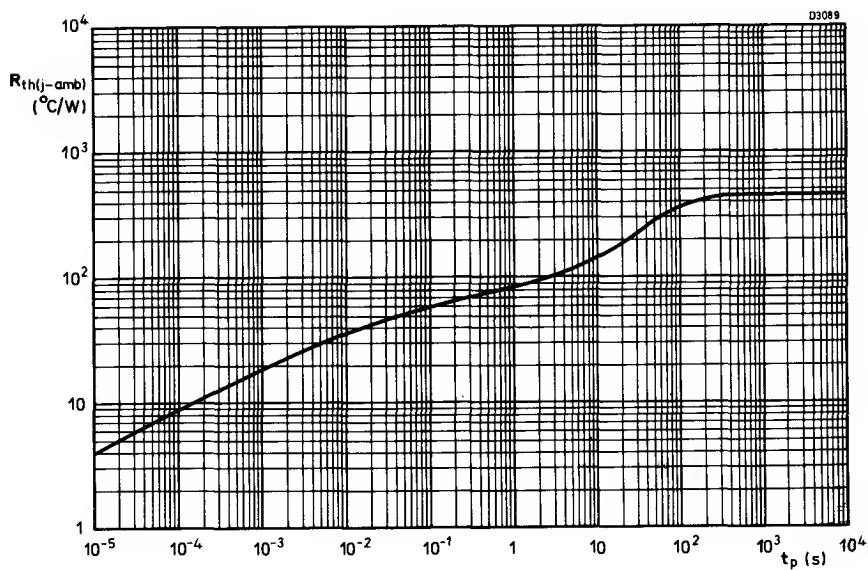
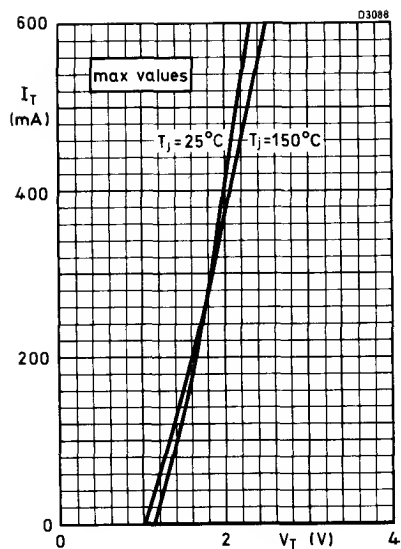
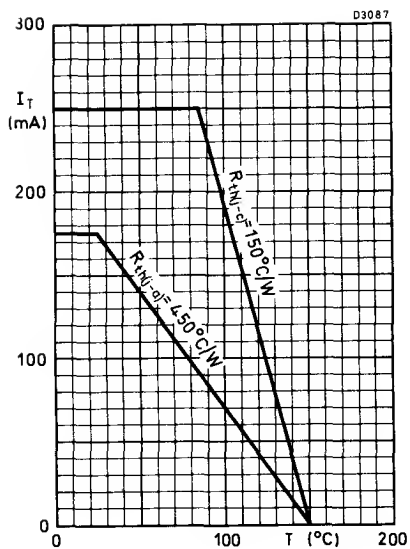
SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

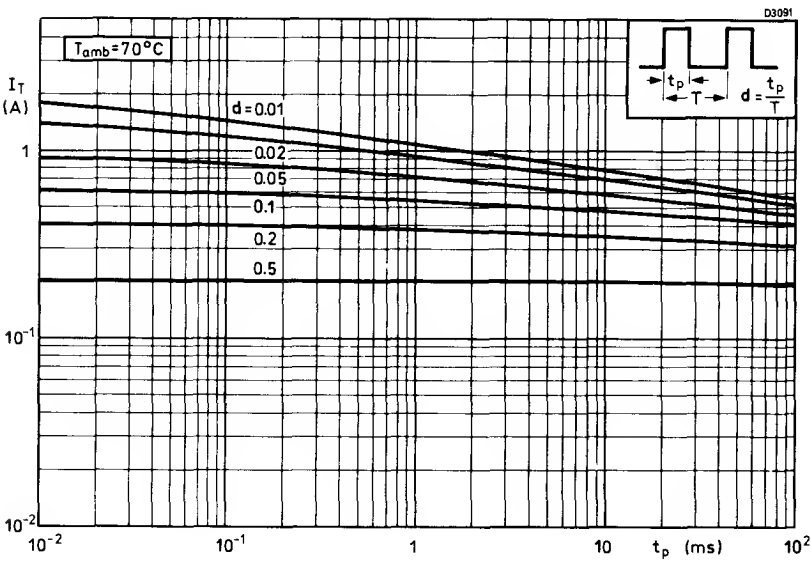
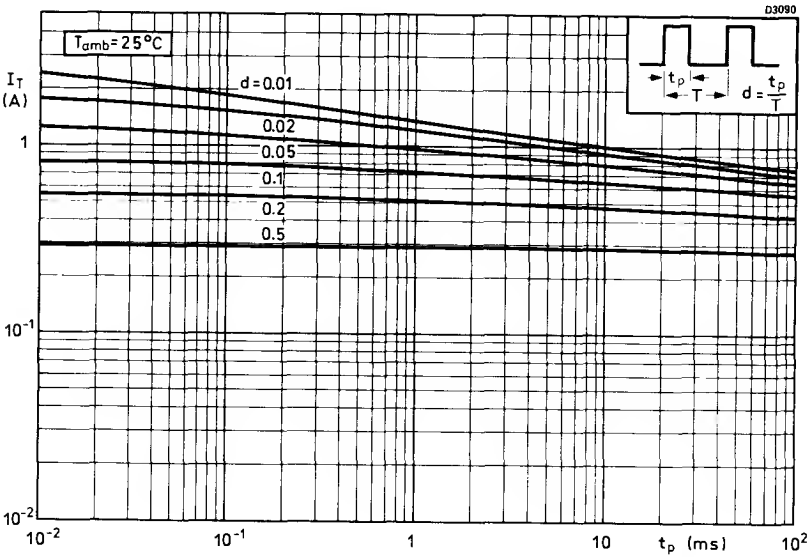
Anode to cathode		Min.	Typ.	Max.	
V_T	On-state voltage $I_T = 100\text{mA}$	-	-	1.4	V
$\frac{dV_D}{dt}$	Rate of rise of off-state voltage that will not trigger any device			See note below	
I_{RM}	Peak reverse current $V_{RM} = 70\text{V}$	-	1.0	100	nA
	$V_{RM} = 70\text{V}, T_j = 150^{\circ}\text{C}$	-	-	2.0	μA
I_{DM}	Peak off-state current $V_{DM} = 70\text{V}$	-	1.0	100	nA
	$V_{DM} = 70\text{V}, T_j = 150^{\circ}\text{C}$	-	-	2.0	μA
I_H	Holding current $R_{GK} = 10\text{k}\Omega, R_{GaA} = 220\text{k}\Omega$	-	-	250	μA
Cathode gate to cathode					
V_{GKT}	Voltage that will trigger all devices $V_D = 6\text{V}$	0.5	-	-	V
I_{GKT}	Current that will trigger all devices $V_D = 6\text{V}$	1.0	-	-	μA
Anode gate to anode					
V_{GaT}	Voltage that will trigger all devices $V_D = 6\text{V}$	1.0	-	-	V
I_{GaT}	Current that will trigger all devices $V_D = 6\text{V}, R_{GK} = 10\text{k}\Omega$	100	-	-	μA
Switching characteristics					
t_{on}	Turn-on time ($t_{on} = t_d + t_r$) $V_D = 15\text{V}, I_T = 150\text{mA}, R_{GK} = 10\text{k}\Omega$	-	-	300	ns
t_{off}	Circuit-commutated turn-off time $V_D = V_R = 15\text{V}, I_T = 150\text{mA}, R_{GK} = 10\text{k}\Omega$	-	-	3.0	μs

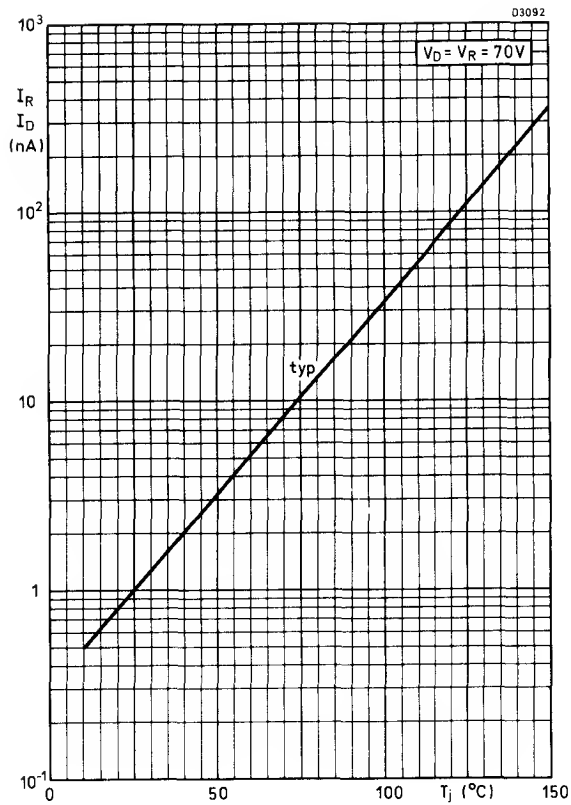
Note: - The dV_D/dt is unlimited when the anode gate lead is returned to the anode supply voltage through a current limiting resistor.



SILICON P-N-P-N
PLANAR TRANSISTOR

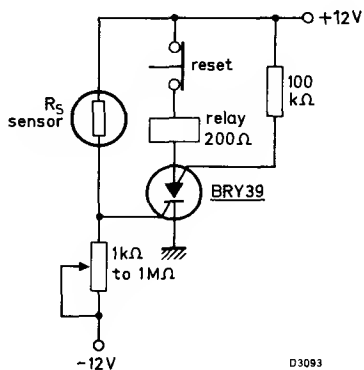
BRY39





APPLICATION INFORMATION

Sensing network



D3093

R_S must be chosen in accordance with the light, temperature, or radiation intensity to be sensed; its resistance should be of the same order as that of the potentiometer.

In the arrangement shown, a decrease in resistance of R_S triggers the thyristor, closing the relay that activates the warning system. If the positions of R_S and the potentiometer are interchanged, an increase in the resistance of R_S will trigger the thyristor.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BSS40
BSS41

Silicon planar epitaxial n-p-n transistors intended for use in driving very high speed core or semiconductor memories and for similar applications.

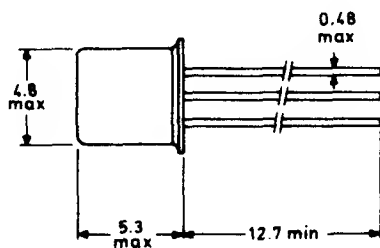
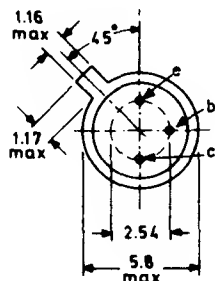
QUICK REFERENCE DATA

	BSS40	BSS41	
V_{CBO} max.	60	60	V
V_{CEO} max.	40	30	V
I_{CM} max.	1.0	1.0	A
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	360	360	mW
h_{FE} min. ($I_C = 500mA$, $V_{CE} = 1V$)	25	25	
$V_{CE(sat)}$ max. ($I_C = 500mA$, $I_B = 50mA$)	0.5	0.5	V
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$)	200	200	MHz
t_{on} max. ($-V_{BE(off)} = 2V$, $I_C = 500mA$, $I_{B(on)} = 50mA$)	35	35	ns
t_{off} max. ($I_C = 500mA$, $I_{B(on)} = -I_{B(off)} = 50mA$)	45	45	ns

Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

Conforming to BS3934 SO-12A/SB3-6A
J. E. D. E. C. TO-18



All dimensions in mm

D3648

Collector connected to case

Accessories available: 56246, 56263

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BSS40	BSS41	
$V_{CBO} \text{ max.}$	60	60	V
$V_{CEO} \text{ max.}$	40	30	V
$V_{EBO} \text{ max.}$		5.0	V
$I_{CM} \text{ max.}$		1.0	A
$I_{BM} \text{ max.}$		0.2	A
$P_{tot} \text{ max.}, T_{amb} \leq 25^{\circ}\text{C}$	360		mW

Temperature

T_{stg}	-65 to +200	$^{\circ}\text{C}$
$T_j \text{ max.}$	200	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ (in free air)	480	$^{\circ}\text{C/W}$
$R_{th(j-case)}$	150	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 100\mu\text{A}, I_E = 0$	60	-	-	V
	Collector-emitter breakdown voltage				
$V_{(BR)CER}$	$I_C = 1.0\text{mA}, R_{BE} = 50\Omega$	BSS40 60	-	-	V
		BSS41 50	-	-	V
$V_{(BR)CEO}$	$I_C = 10\text{mA}, I_B = 0$	BSS40 40	-	-	V
		BSS41 30	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 100\mu\text{A}, I_C = 0$	5.0	-	-	V
I_{CER}	Collector cut-off current $V_{CE} = 40\text{V}, R_{BE} = 50\Omega$	-	-	1.0	μA
	$V_{CE} = 40, R_{BE} = 50\Omega, T_j = 150^{\circ}\text{C}$	-	-	1.0	mA
$-I_{BEX}$	Base cut-off current				
	$-V_{BE} = 4.0\text{V}, V_{CE} = 40\text{V}$	BSS40 -	-	1.0	μA
	$-V_{BE} = 4.0\text{V}, V_{CE} = 30\text{V}$	BSS41 -	-	1.0	μA

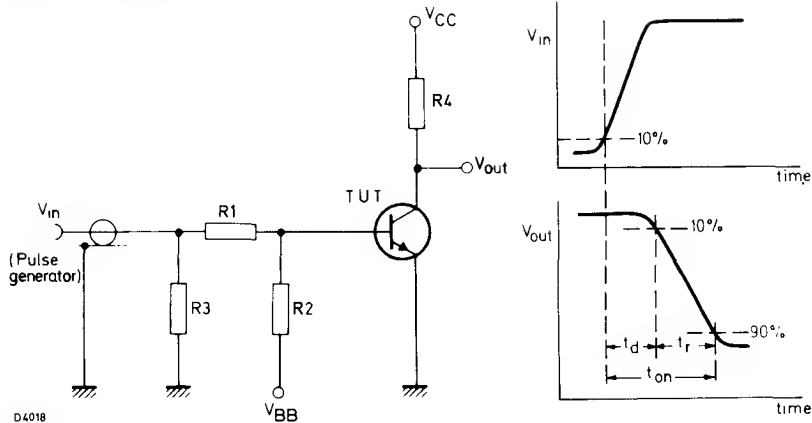
ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
$V_{CE(sat)}$	*Collector-emitter saturation voltage $I_C = 150\text{mA}, I_B = 10\text{mA}$	-	-	0.3	V
	$I_C = 500\text{mA}, I_B = 50\text{mA}$	-	-	0.5	V
$V_{BE(sat)}$	*Base-emitter saturation voltage $I_C = 150\text{mA}, I_B = 10\text{mA}$	-	-	1.0	V
	$I_C = 500\text{mA}, I_B = 50\text{mA}$	-	-	1.2	V
h_{FE}	*Static forward current transfer ratio $I_C = 150\text{mA}, V_{CE} = 1.0\text{V}$	30	-	-	
	$I_C = 500\text{mA}, V_{CE} = 1.0\text{V}$	25	-	-	
f_T	Transition frequency $I_C = 50\text{mA}, V_{CE} = 10\text{V}, f = 100\text{MHz}$	200	-	-	MHz
C_{Tc}	Collector capacitance $I_E = I_C = 0, V_{CB} = 10\text{V}, f = 1.0\text{MHz}$	-	-	10	pF
C_{Te}	Emitter capacitance $I_C = I_E = 0, V_{EB} = 0.5\text{V}, f = 1.0\text{MHz}$	-	-	50	pF
Switching characteristics (see test circuits on page 4)					
t_{on}	Turn-on time when switched from $-V_{BE(off)} = 2\text{V}$ to $I_C = 500\text{mA}, I_{B(on)} = 50\text{mA}$	-	-	35	ns
t_{off}	Turn-off time when switched from $I_C = 500\text{mA}, I_{B(on)} = 50\text{mA}$ to cut-off				
	with $-I_{B(off)} = 1.0\text{mA}$	-	-	250	ns
	with $-I_{B(off)} = 50\text{mA}$	-	-	45	ns
t_s	Storage time when switched from $I_C = 500\text{mA}, I_{B(on)} = 50\text{mA}$ to cut-off with $-I_{B(off)} = 50\text{mA}$	10	-	-	ns

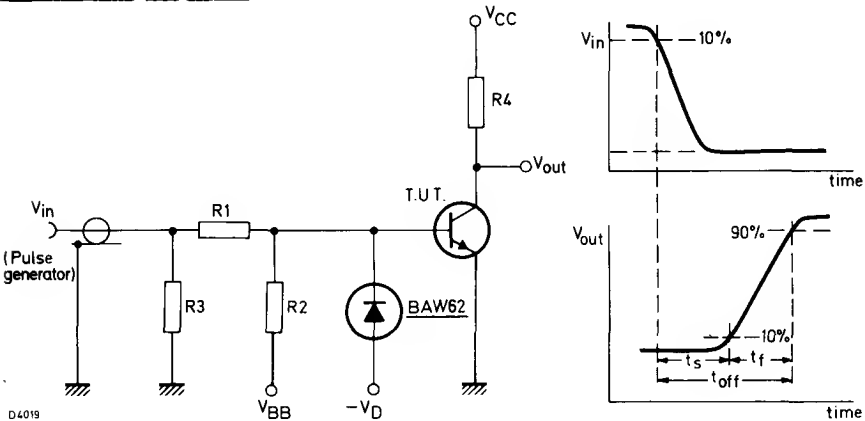
*Measured under pulsed conditions $t_p = 300\mu\text{s}$, $d = 0.01$

ELECTRICAL CHARACTERISTICS (contd.)

Turn-on time test circuit



Turn-off time test circuit



BSS40, BSS41								t_{on}		t_{off}		
I_C (mA)	$I_{B(on)}$ (mA)	$I_{B(off)}$ (mA)	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	$-V_{BB}$ (V)	V_{in} (V)	$+V_{BB}$ (V)	V_{in} (V)	$-V_D$ (V)
500	50	50	30	375	400	56	60	4	24.75	16.7	37.5	3
500	50	1	30	750	∞	56	60				37.5	

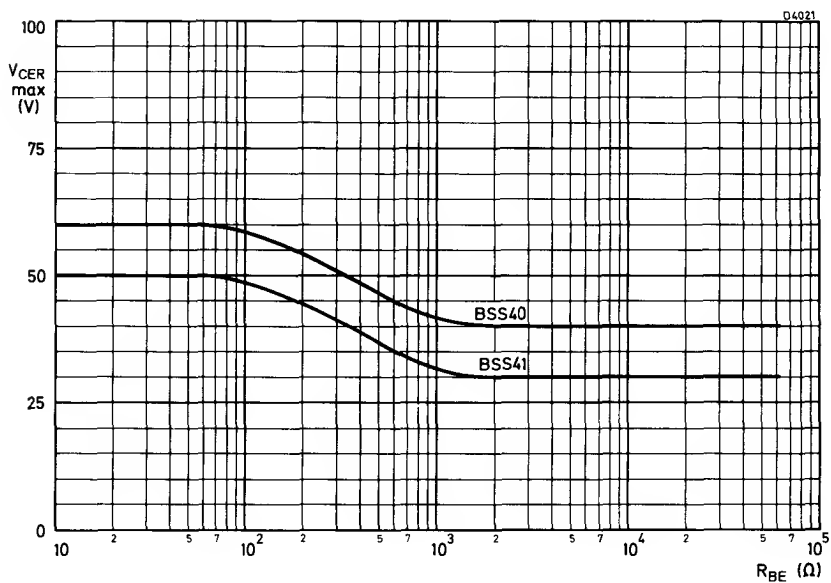
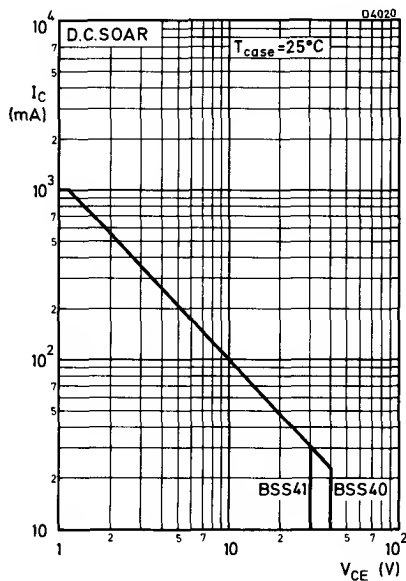
Pulse generator

Pulse duration $t_p \geq 500\text{ns}$
Rise time $t_r \leq 5\text{ns}$

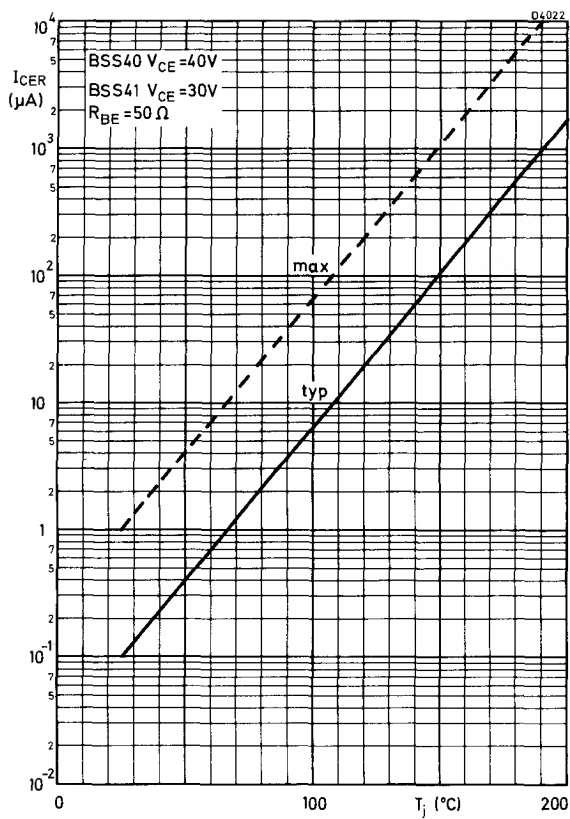
Fall time $t_f \leq 5\text{ns}$
Source impedance $R_S = 50\Omega$

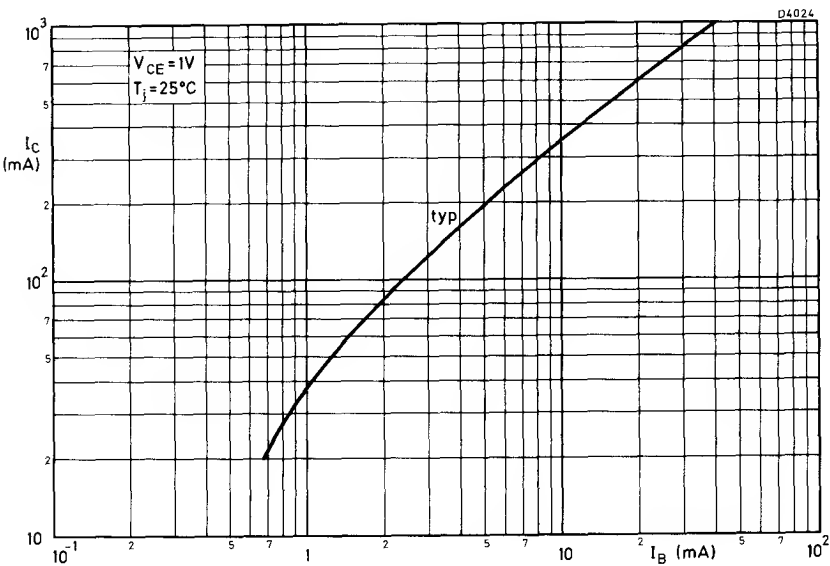
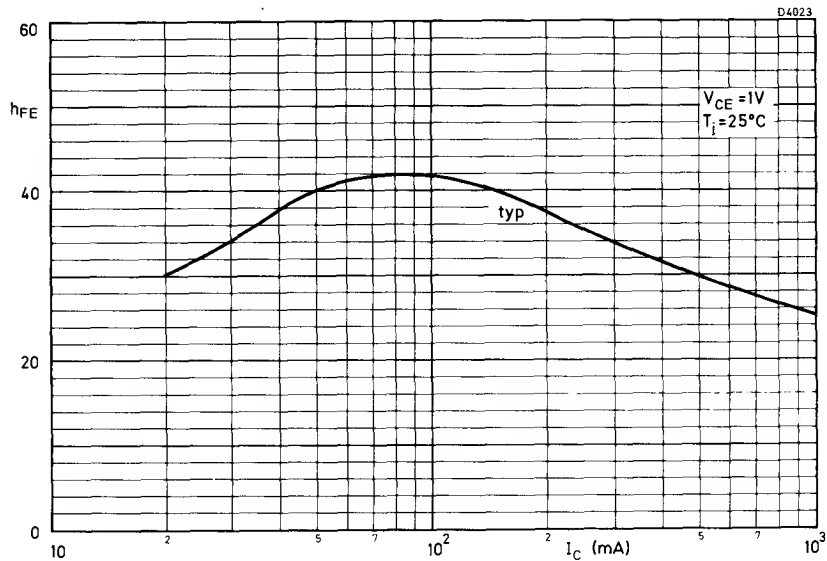
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

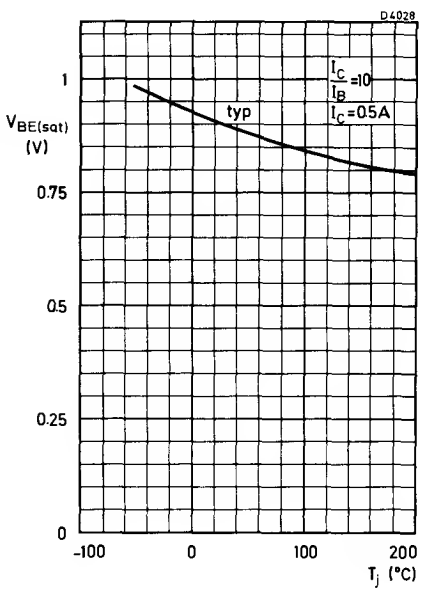
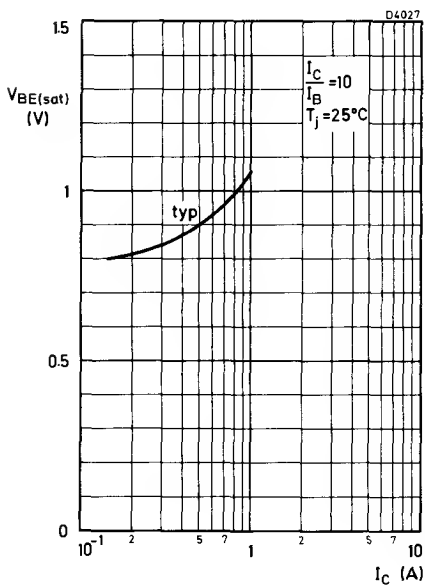
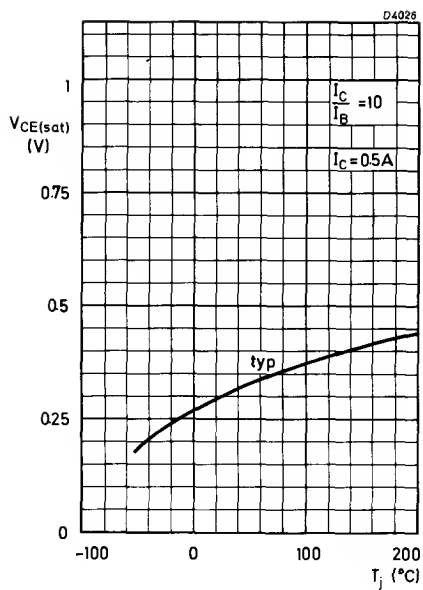
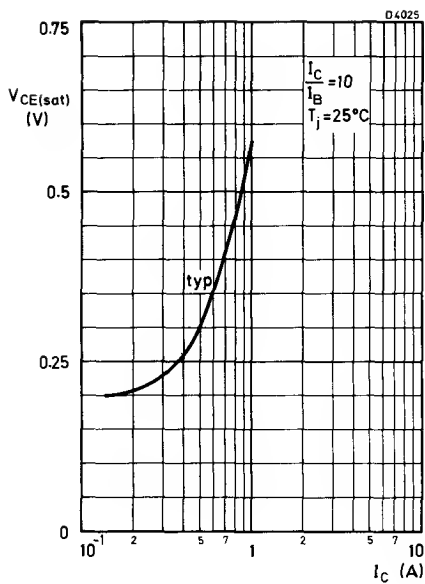
BSS40
BSS41



Mullard

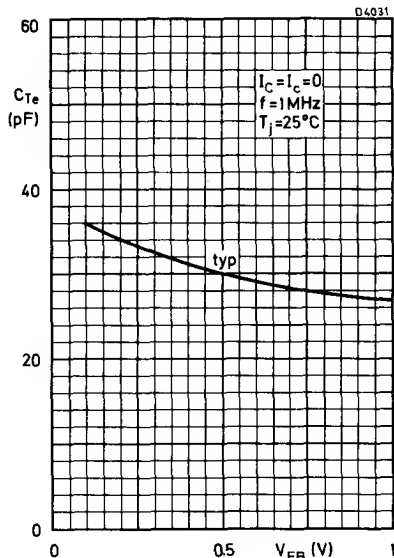
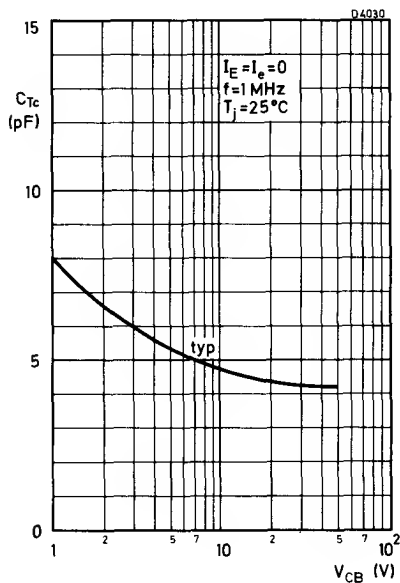
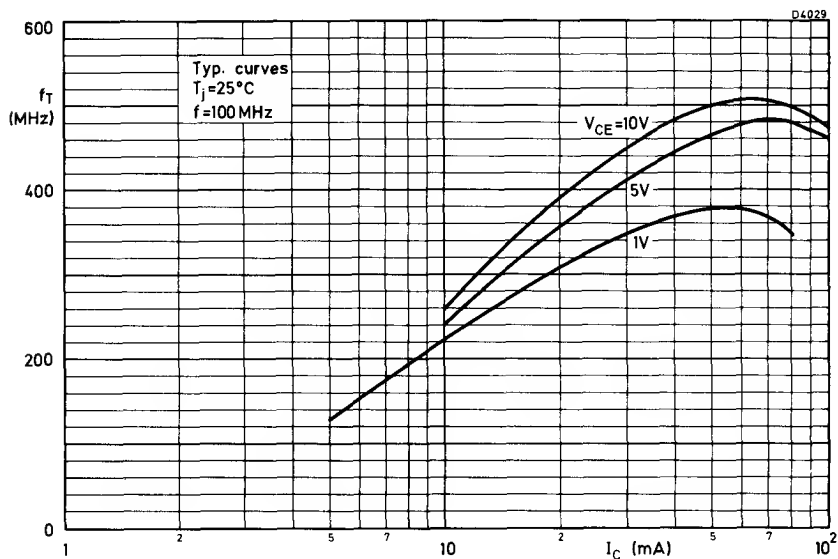




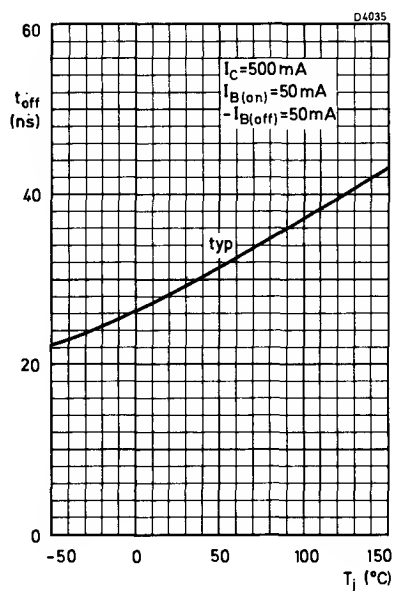
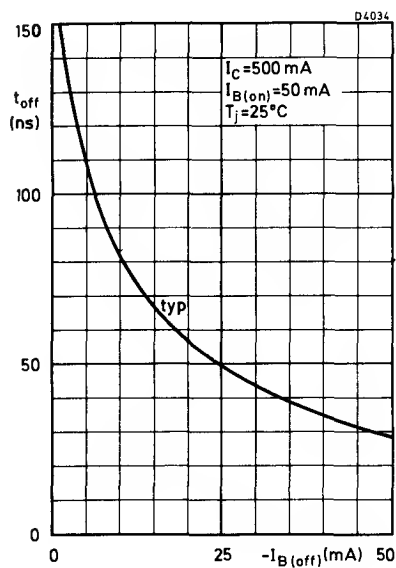
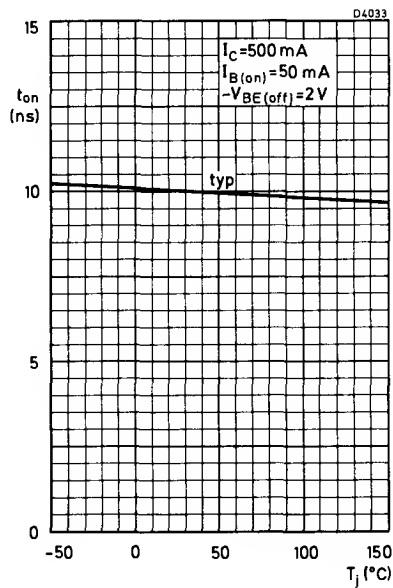
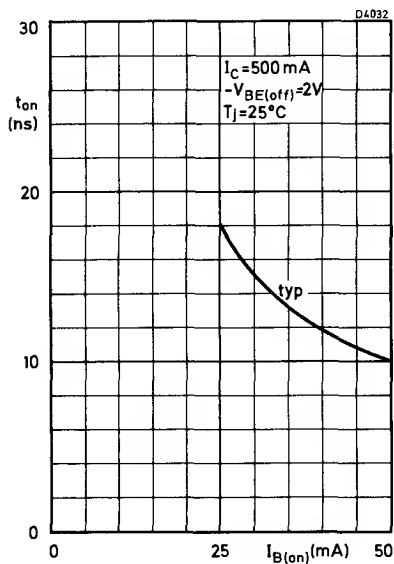


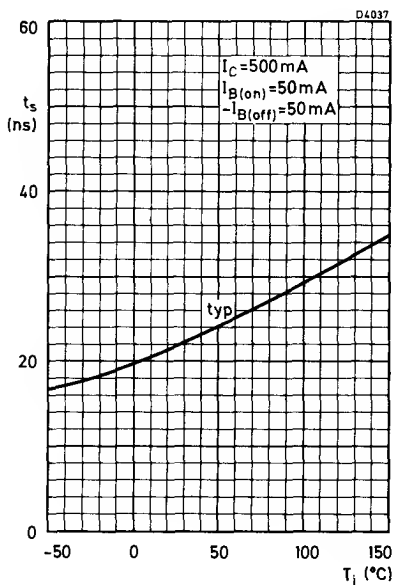
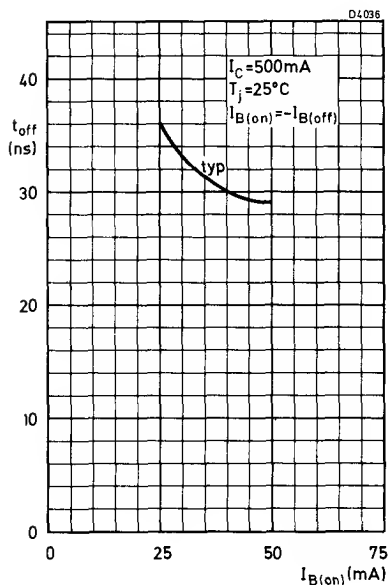
N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BSS40
BSS41



Mullard





N-P-N SILICON PLANAR DARLINGTON TRANSISTORS

BSS50
BSS51
BSS52

Silicon n-p-n planar Darlington transistors for industrial switching applications e.g. print hammer, solenoid, relay and lamp driving. Encapsulated in a TO-39 envelope with the collector connected to the can.

QUICK REFERENCE DATA

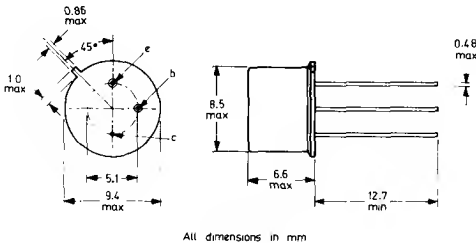
	BSS50	BSS51	BSS52	
V_{CBO} max.	60	80	100	V
V_{CE} max.	45	60	80	V
I_C max.	1.0	1.0	1.0	A
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	0.8	0.8	0.8	W
P_{tot} max. ($T_{case} \leq 25^\circ C$)	5.0	5.0	5.0	W
h_{FE} min. ($I_C = 500mA$, $V_{CE} = 10V$)	1500	1500	1500	
$V_{CE(sat)}$ max. ($I_C = 1.0A$, $I_B = 1.0mA$)	-	1.6	-	V
$V_{CE(sat)}$ max. ($I_C = 1.0A$, $I_B = 4.0mA$)	1.6	-	1.6	V
t_{off} typ. ($I_C = 500mA$, $I_{B(on)} = -I_{B(off)} = 0.5mA$)	1.0	1.0	1.0	μs

Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39

Collector connected to the envelope



04930

Max. lead diameter is only guaranteed for 12.7mm from the can.

Accessories available: 56218, 56245, 56265

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BSS50	BSS51	BSS52	
V_{CBO} max.	60	80	100	V
* V_{CE} max.	45	60	80	V
V_{EBO} max.	5.0	5.0	5.0	V
I_C max.	1.0	1.0	1.0	A
I_{CM} max. (peak value)	2.0	2.0	2.0	A
I_B max.	0.1	0.1	0.1	A
P_{tot} max. ($T_{amb} \leq 25^\circ\text{C}$)	0.8	0.8	0.8	W
($T_{case} \leq 25^\circ\text{C}$)	5.0	5.0	5.0	W

Temperature

T_{stg} range	-65 to +200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	220	$^\circ\text{C/W}$
$R_{th(j-case)}$	35	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 45\text{V}, I_E = 0$ BSS50	-	-	50	nA
	$V_{CB} = 60\text{V}, I_E = 0$ BSS51	-	-	50	nA
	$V_{CB} = 80\text{V}, I_E = 0$ BSS52	-	-	50	nA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 4.0\text{V}, I_C = 0$	-	-	50	nA
h_{FE}	Static forward current transfer ratio				
	$I_C = 150\text{mA}, V_{CE} = 10\text{V}$	1500	-	-	
	$I_C = 500\text{mA}, V_{CE} = 10\text{V}$	1500	-	-	

*External R_{BE} not to exceed value shown on page 5.

N-P-N SILICON PLANAR DARLINGTON TRANSISTORS

BSS50
BSS51
BSS52

ELECTRICAL CHARACTERISTICS (Cont'd)

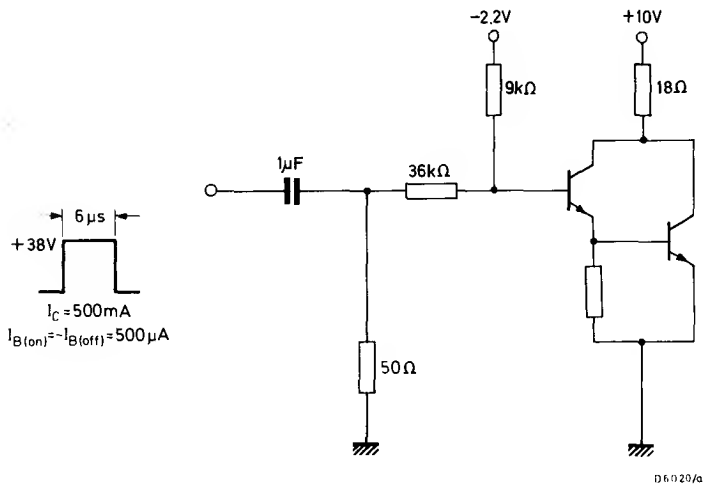
		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 500\text{mA}$, $I_B = 0.5\text{mA}$	-	-	1.3	V
	$I_C = 1.0\text{A}$, $I_B = 1.0\text{mA}$ BSS51	-	-	1.6	V
	$I_C = 1.0\text{A}$, $I_B = 4.0\text{mA}$ BSS50	-	-	1.6	V
	BSS52	-	-	1.6	V
	$I_C = 500\text{mA}$, $I_B = 0.5\text{mA}$, $T_j = 200^\circ\text{C}$	-	-	1.3	V
	$I_C = 1.0\text{A}$, $I_B = 1.0\text{mA}$, $T_j = 200^\circ\text{C}$ BSS51	-	-	2.3	V
	$I_C = 1.0\text{A}$, $I_B = 4.0\text{mA}$, $T_j = 200^\circ\text{C}$ BSS50	-	-	1.6	V
	BSS52	-	-	1.6	V
$V_{BE(sat)}$	Base-emitter saturation voltage 1) $I_C = 500\text{mA}$, $I_B = 0.5\text{mA}$	-	-	1.9	V
	$I_C = 1.0\text{A}$, $I_B = 1.0\text{mA}$ BSS51	-	-	2.2	V
	$I_C = 1.0\text{A}$, $I_B = 4.0\text{mA}$ BSS50	-	-	2.2	V
	BSS52	-	-	2.2	V
V_{BE}	Base-emitter voltage 2) $I_C = 150\text{mA}$, $V_{CE} = 10\text{V}$	1.4	1.45	1.55	V
	$I_C = 500\text{mA}$, $V_{CE} = 10\text{V}$	1.5	1.55	1.65	V
h_{fe}	Small signal forward current transfer ratio $I_C = 500\text{mA}$, $V_{CE} = 5.0\text{V}$, $f = 35\text{MHz}$	7.5	10	-	
Saturated switching times					
	$I_C = 500\text{mA}$, $I_{B(on)} = -I_{B(off)} = 0.5\text{mA}$				
t_{on}	Turn-on time	-	-	400	ns
t_{off}	Turn-off time	-	1.0	2.0	μs
	$I_C = 1.0\text{A}$, $I_{B(on)} = -I_{B(off)} = 1.0\text{mA}$				
t_{on}	Turn-on time	-	-	400	ns
t_{off}	Turn-off time	-	1.0	2.0	μs

Notes: 1) $V_{BE(sat)}$ decreases by about $2.5\text{mV}/^\circ\text{C}$ with increasing temperature.

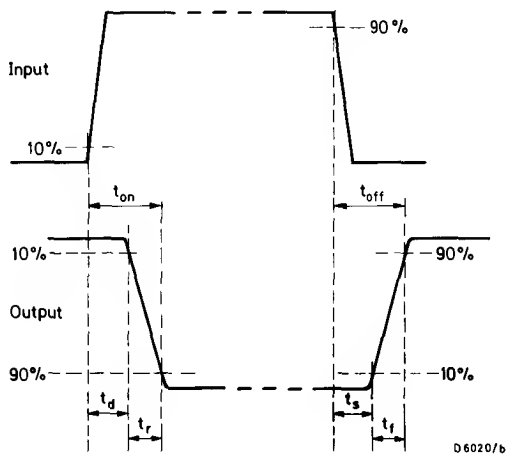
2) V_{BE} decreases by about $3.5\text{mV}/^\circ\text{C}$ with increasing temperature.

MEASUREMENT OF SATURATED SWITCHING TIMES

Test circuit for 500mA switching.

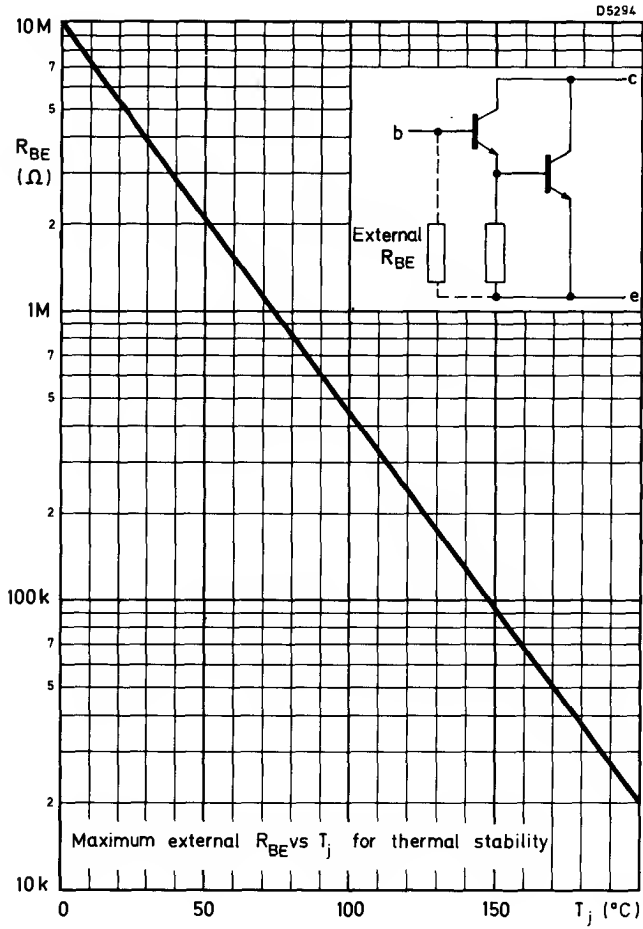


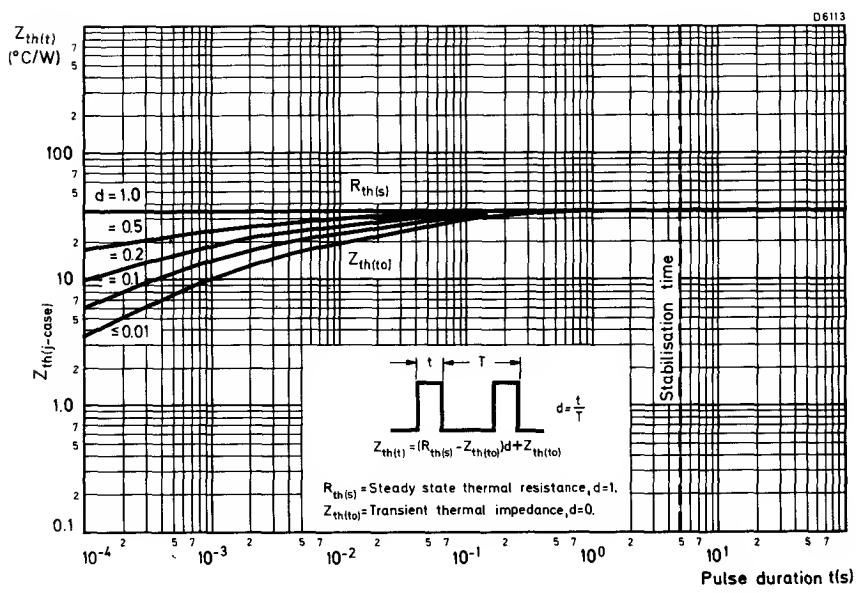
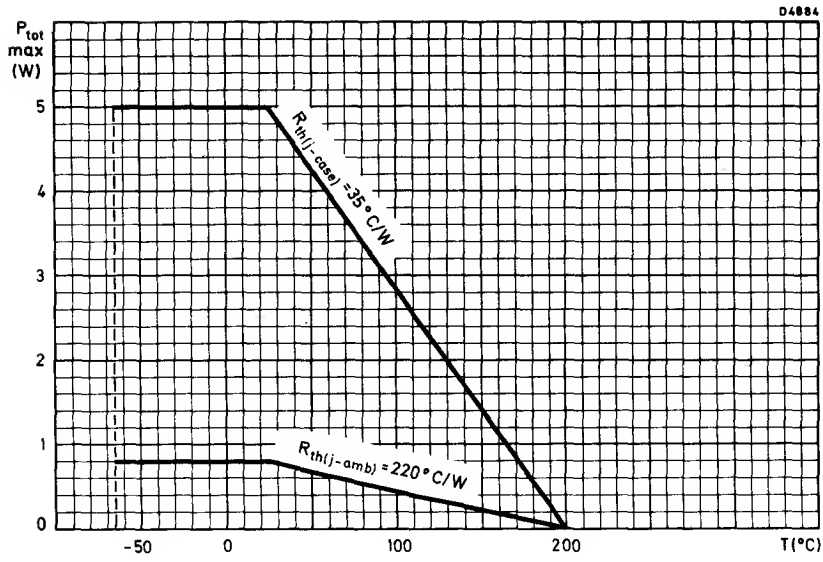
Switching waveforms



**N-P-N SILICON PLANAR
DARLINGTON TRANSISTORS**

**BSS50
BSS51
BSS52**

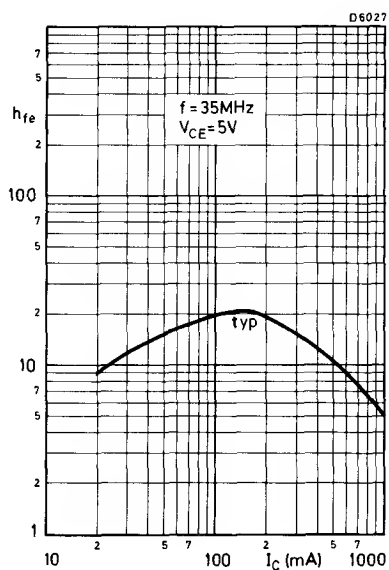
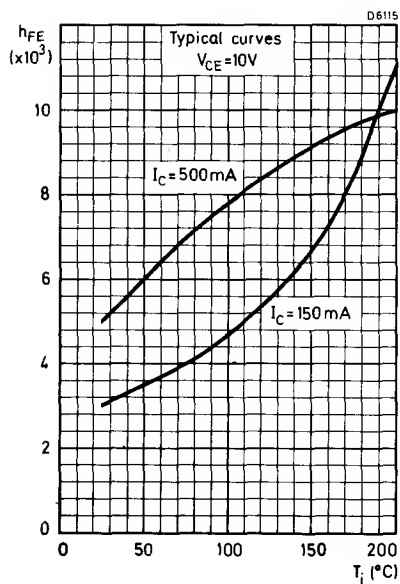
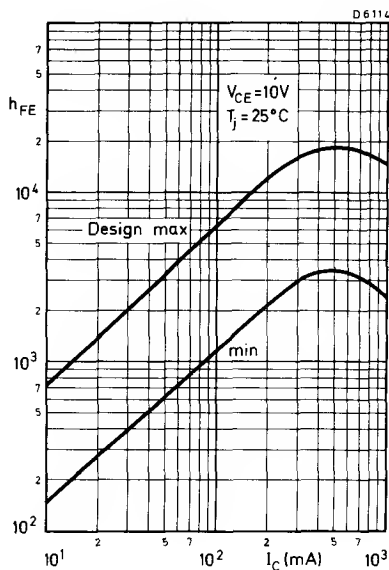
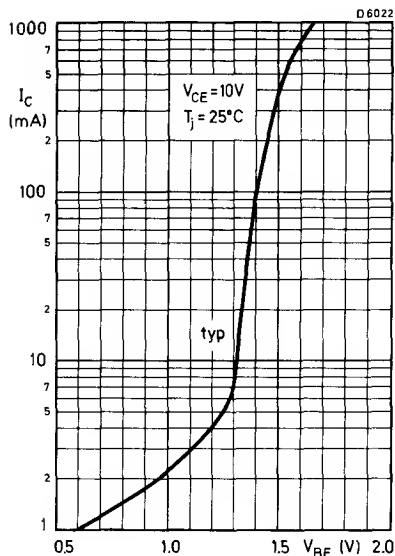




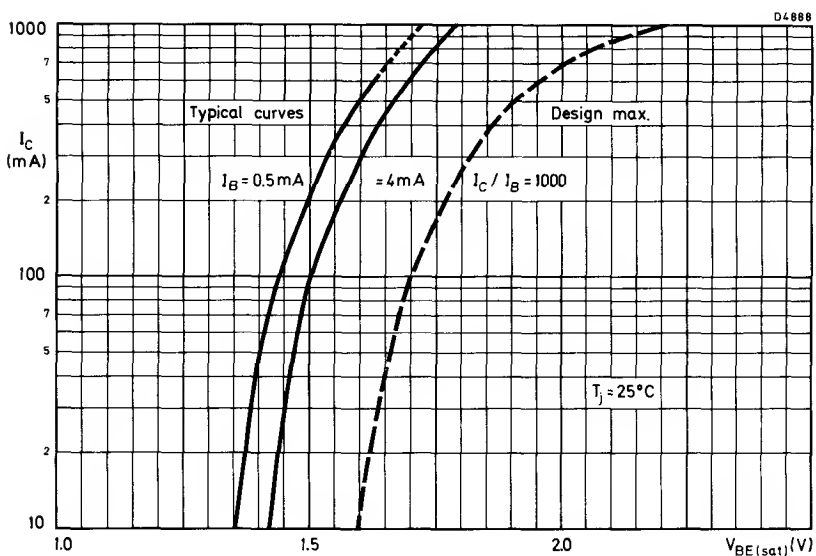
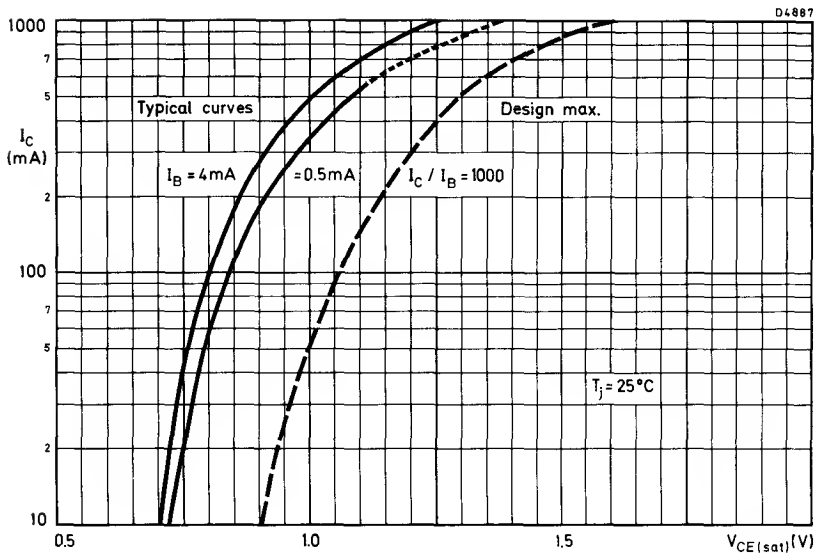
Mullard

N-P-N SILICON PLANAR DARLINGTON TRANSISTORS

BSS50
BSS51
BSS52



Mullard



μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

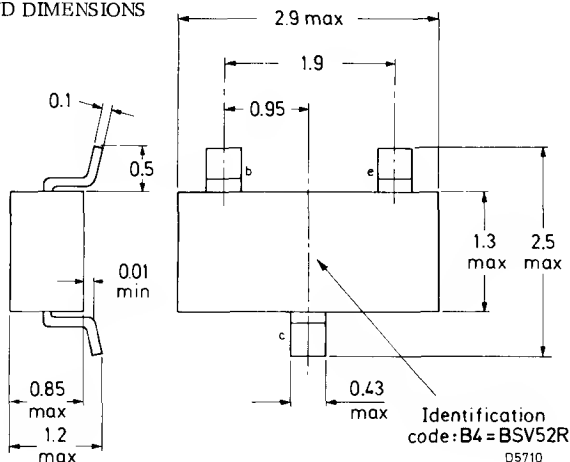
BSV52R

Silicon n-p-n planar epitaxial transistor in a microminiature plastic envelope, intended for high-speed switching in thin and thick film circuits.

QUICK REFERENCE DATA

V_{CBO}	max.	20	V
V_{CES}	max.	20	V
V_{CEO}	max.	12	V
I_{CM}	max.	200	mA
P_{tot}	max. ($T_{amb} \leq 25^{\circ}C$)	200	mW
T_j	max.	150	$^{\circ}C$
h_{FE}	at $I_C = 10mA, V_{CE} = 1V$	40-120	
	$I_C = 50mA, V_{CE} = 1V$	min. 25	
f_T	at $I_C = 10mA, V_{CE} = 10V,$ $f = 100MHz$	min. 400	MHz
		typ. 500	MHz
t_s	max. at $I_C = I_{B(on)} = -I_{B(off)} = 10mA$	13	ns

OUTLINE AND DIMENSIONS



All dimensions in millimetres
Plan view from above

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO}	max.	20	V
V_{CES}	max.	20	V
V_{CEO}	max. ($I_C = 10\text{mA}$)	12	V
V_{EBO}	max.	5.0	V
I_C	max.	100	mA
I_{CM}	max.	200	mA
P_{tot}	max. $T_{amb} \leq 25^\circ\text{C}$, mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	200	mW

Temperature

T_{stg}		-65 to +150	$^\circ\text{C}$
T_j	max.	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $7 \times 5 \times 0.5\text{mm}$	0.62	$^\circ\text{C/mW}$
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$I_E = 0, V_{CB} = 10\text{V}$	-	-	100	nA
	$I_E = 0, V_{CB} = 10\text{V}, T_j = 125^\circ\text{C}$	-	-	5.0	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10\text{mA}, I_B = 0.3\text{mA}$	-	-	300	mV
	$I_C = 10\text{mA}, I_B = 1.0\text{mA}$	-	-	250	mV
	$I_C = 50\text{mA}, I_B = 5.0\text{mA}$	-	-	400	mV
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10\text{mA}, I_B = 1.0\text{mA}$	700	-	850	mV
	$I_C = 50\text{mA}, I_B = 5.0\text{mA}$	-	-	1.2	V
h_{FE}	Static forward current transfer ratio				
	$I_C = 1.0\text{mA}, V_{CE} = 1.0\text{V}$	25	-	-	
	$I_C = 10\text{mA}, V_{CE} = 1.0\text{V}$	40	-	120	
	$I_C = 50\text{mA}, V_{CE} = 1.0\text{V}$	25	-	-	
f_T	Transition frequency				
	$I_C = 10\text{mA}, V_{CE} = 10\text{V}, f = 100\text{MHz}$	400	500	-	MHz

μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BSV52R

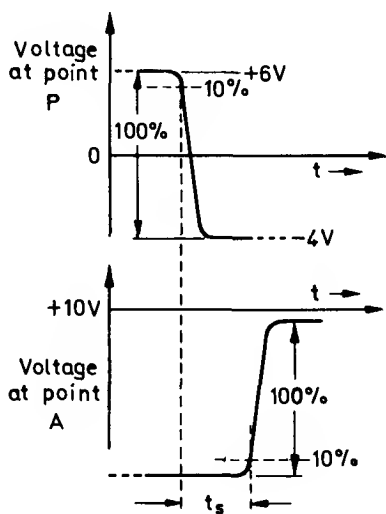
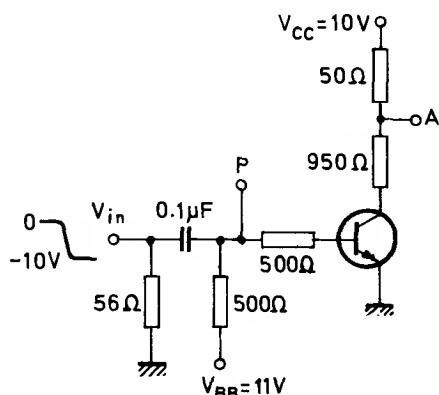
ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
C_{Tc}	Collector capacitance $I_E = I_e = 0, V_{CB} = 5.0V,$ $f = 1.0MHz$	-	-	4.0	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0, V_{EB} = 1.0V,$ $f = 1.0MHz$	-	-	4.5	pF

SWITCHING CHARACTERISTICS

t_s	Storage time ($I_C = I_{B(on)} = -I_{B(off)}$ $= 10mA$)	-	-	13	ns
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Test circuit and waveforms



Pulse generator:

$Z_s = 50\Omega$
 $t_r < 1.0ns$
 $t_p > 300ns$
 $d < 0.02$

Oscilloscope:

$Z_{in} = 50\Omega$
 $t_r < 1.0ns$

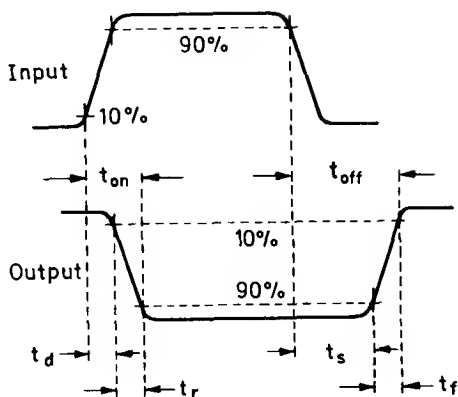
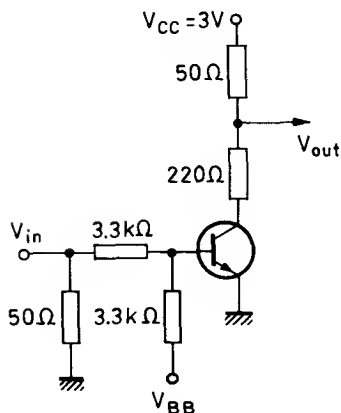
D5725

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SWITCHING CHARACTERISTICS (contd.)

		Min.	Typ.	Max.
t_{on}	Turn-on time when switched from $-V_{BE} = 1.5V$ to $I_C = 10mA$, $I_B = 3mA$, $-V_{BB} = 3V$, $V_{in} = 15V$	-	-	12 ns
t_{off}	Turn-off time when switched from $I_C = 10mA$, $I_B = 3mA$, to cut-off with $-I_{B(off)} = 1.5mA$, $V_{BB} = 12V$, $-V_{in} = 15V$	-	-	18 ns

Test circuit and waveforms



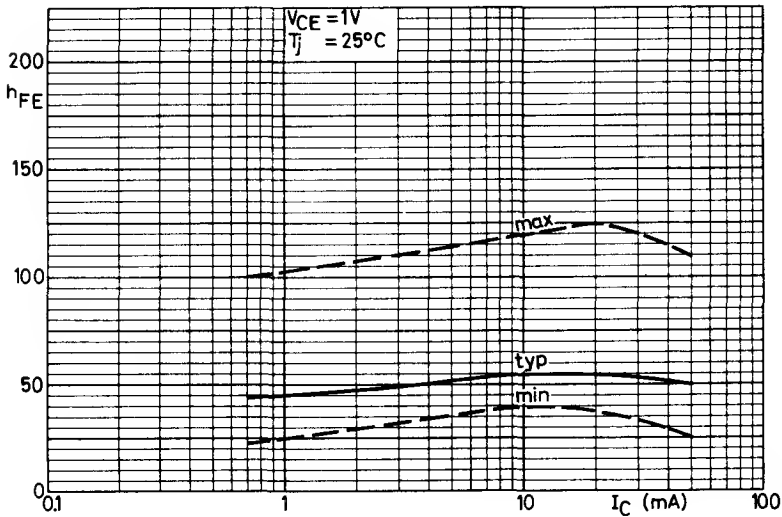
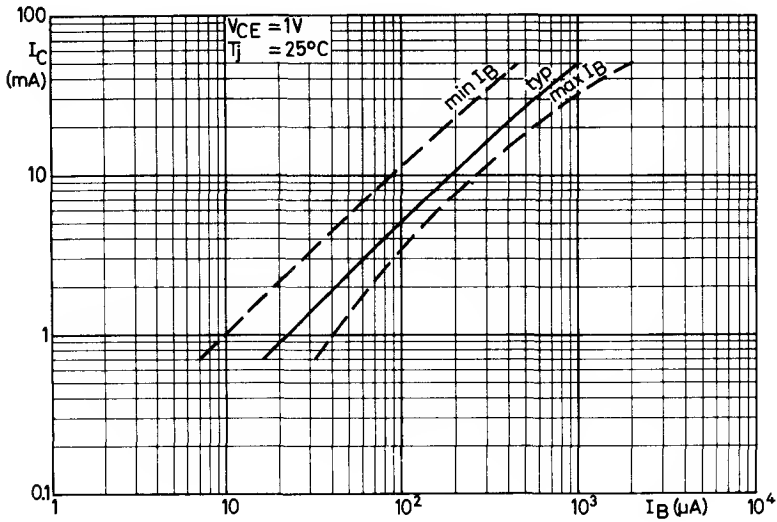
Pulse generator :

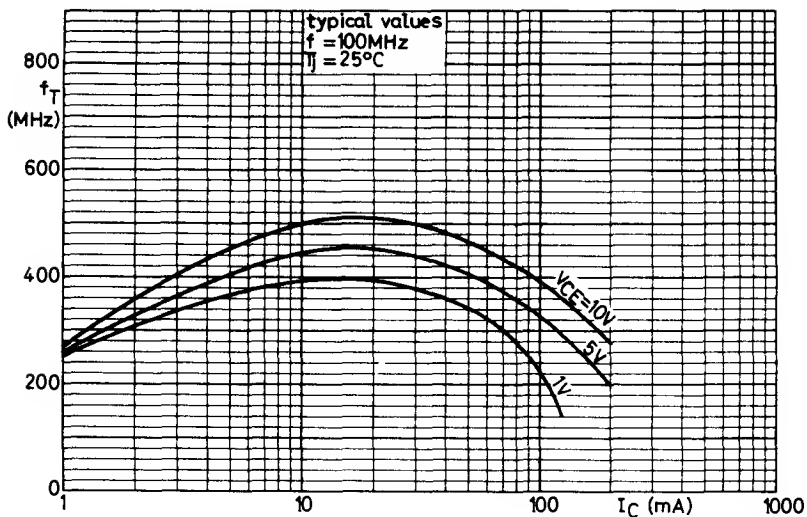
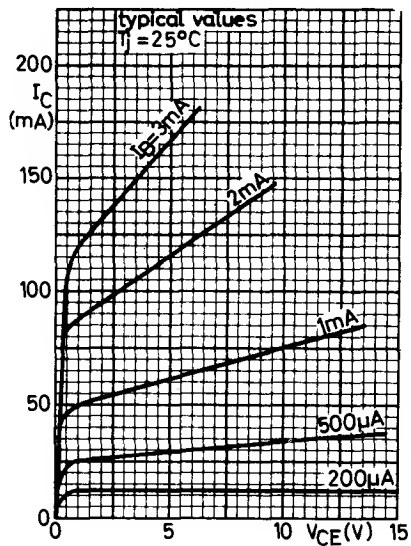
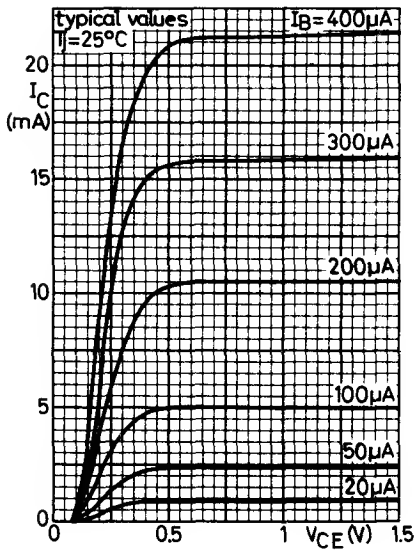
$Z_s = 50\Omega$
 $t_r < 1.0ns$
 $t_p > 300ns$
 $d < 0.02$

Oscilloscope :

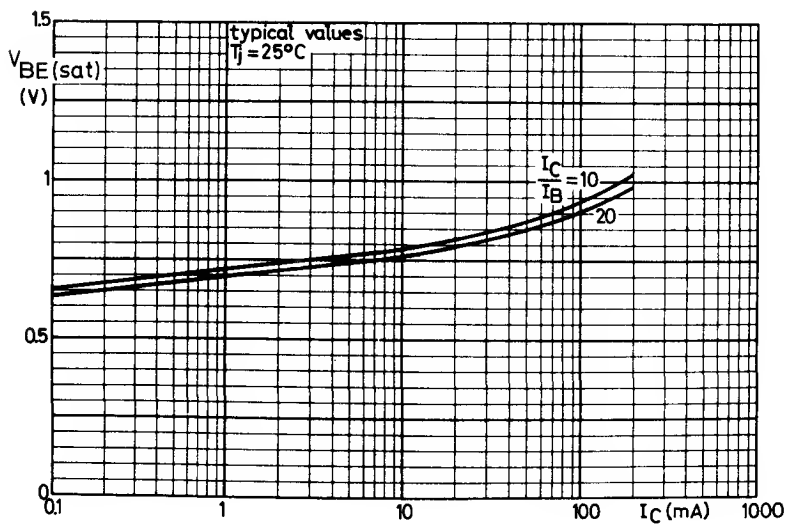
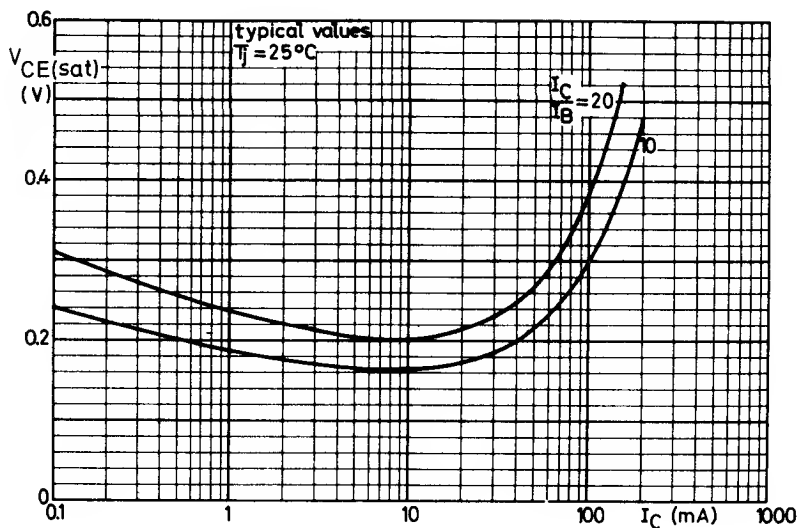
$Z_{in} = 50\Omega$
 $t_r < 1.0ns$

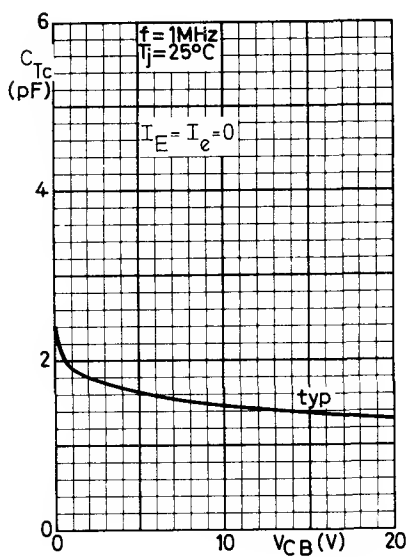
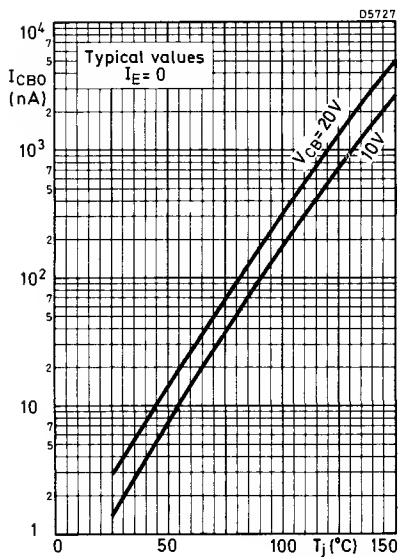
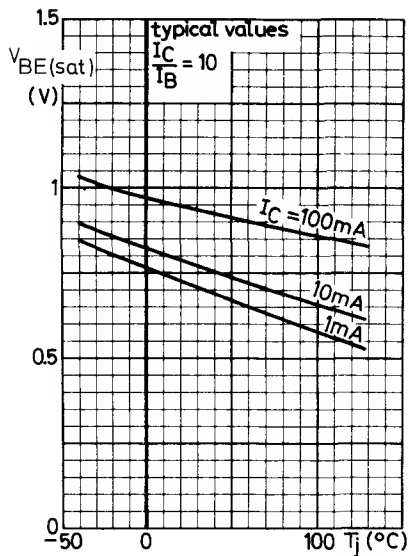
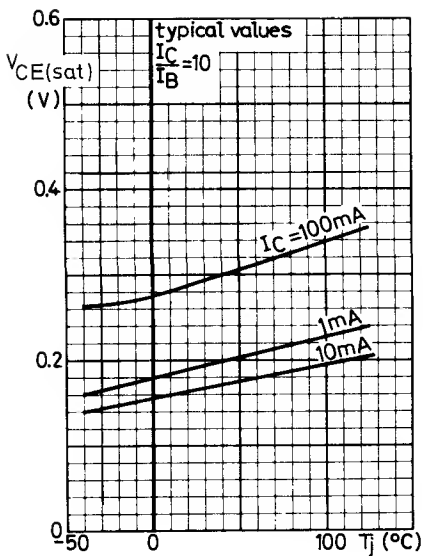
D5726





Mullard





N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BSV64

N-P-N silicon planar epitaxial transistor, with good high current saturation characteristics, primarily intended for use as a print hammer drive.

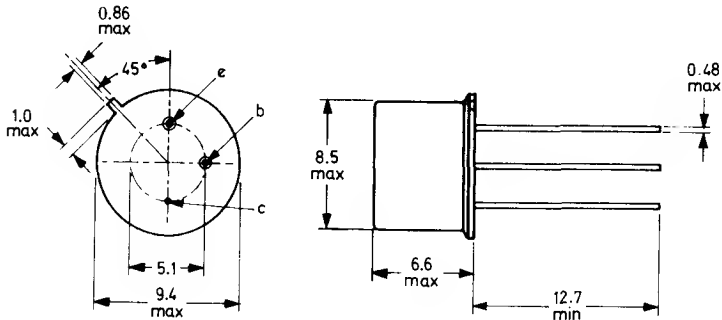
QUICK REFERENCE DATA

V_{CBO} max.	100	V
V_{CEO} max.	60	V
I_{CM} max.	5.0	A
P_{tot} max. ($T_{case} \leq 50^{\circ}C$)	5.0	W
h_{FE} min. ($I_C = 2.0A$, $V_{CE} = 2.0V$)	40	
f_T typ. ($I_C = 0.5A$, $V_{CE} = 5.0V$, $f = 35MHz$, $T_{amb} = 25^{\circ}C$)	100	MHz
t_{off} max. ($I_C = 5.0A$, $I_{B(on)} = -I_{B(off)} = 0.5A$)	1.2	μs

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A

J.E.D.E.C. TO-39



All dimensions in mm

D1574

Collector connected to case

The maximum lead diameter is guaranteed only for 12.7mm.

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	100	V
V_{CER} max. ($R_B \leq 50\Omega$)	80	V
V_{CEO} max.	60	V
V_{EBO} max.	5.0	V
I_{CM} max.	5.0	A
I_C max.	2.0	A
I_B max.	1.0	A
P_{tot} max. $T_{case} \leq 50^\circ C$	5.0	W

Temperature

T_{stg}	-55 to +175	$^\circ C$
T_j max.	+175	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-case)}$ max.	25	degC/W
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ELECTRICAL CHARACTERISTICS (at $T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 60V, I_E = 0$	-	-	10	μA
I_{EBO}	Emitter cut-off current $V_{EB} = 4.0V, I_C = 0$	-	-	10	μA
h_{FE}	Static forward current transfer ratio $I_C = 2.0A, V_{CE} = 2.0V$	40	-	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 5.0A, I_B = 0.5A$	-	-	1.0	V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 5.0A, I_B = 0.5A$	-	-	1.8	V
C_{Tc}	Collector capacitance $V_{CB} = 10V, I_E = I_e = 0, f = 1.0MHz$	-	-	80	pF

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BSV64

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 0.5A$, $V_{CE} = 5.0V$, $f = 35MHz$, $T_{amb} = 25^{\circ}C$	-	100	-	MHz
Saturated switching times					
	$I_C = 5.0A$, $I_{B(on)} = -I_{B(off)} = 0.5A$, $V_{BE(off)} = 2.0V$				
t_{on}	Turn-on time	-	-	0.6	μs
t_{off}	Turn-off time	-	-	1.2	μs

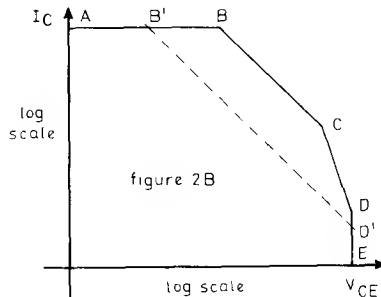
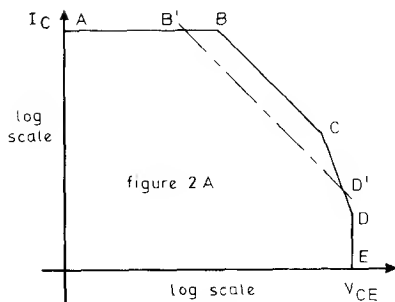
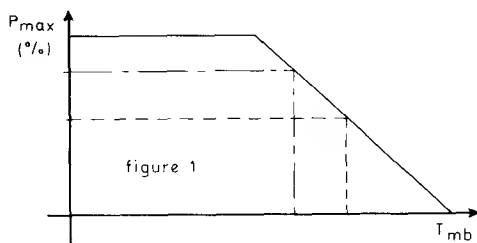
SOLDERING AND WIRING RECOMMENDATIONS

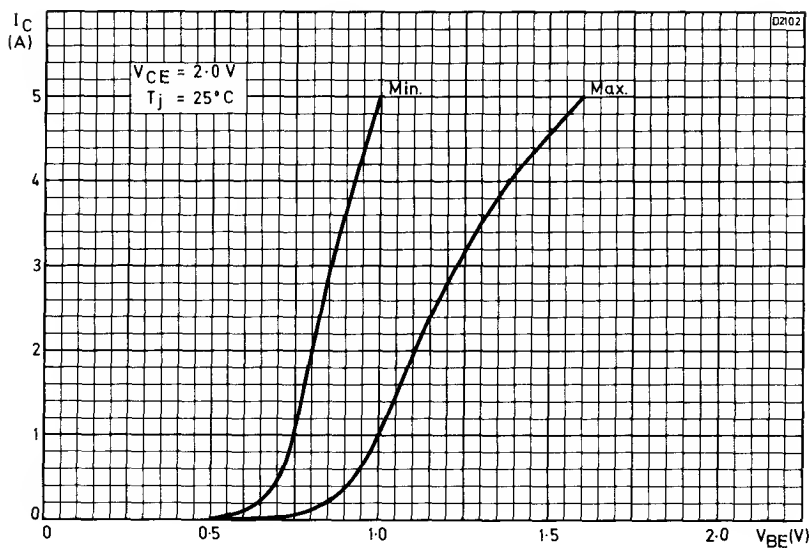
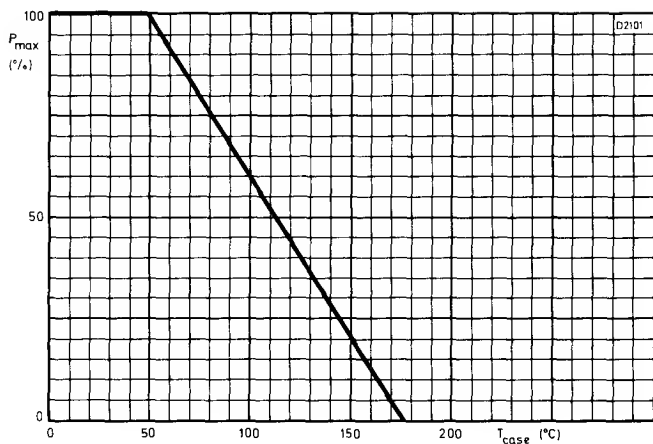
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should, if possible, be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of $245^{\circ}C$ for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above $100^{\circ}C$ before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

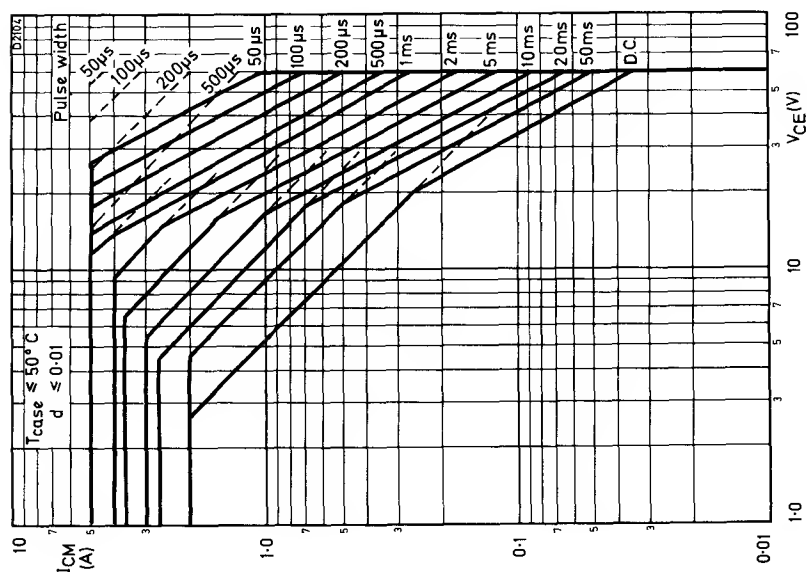
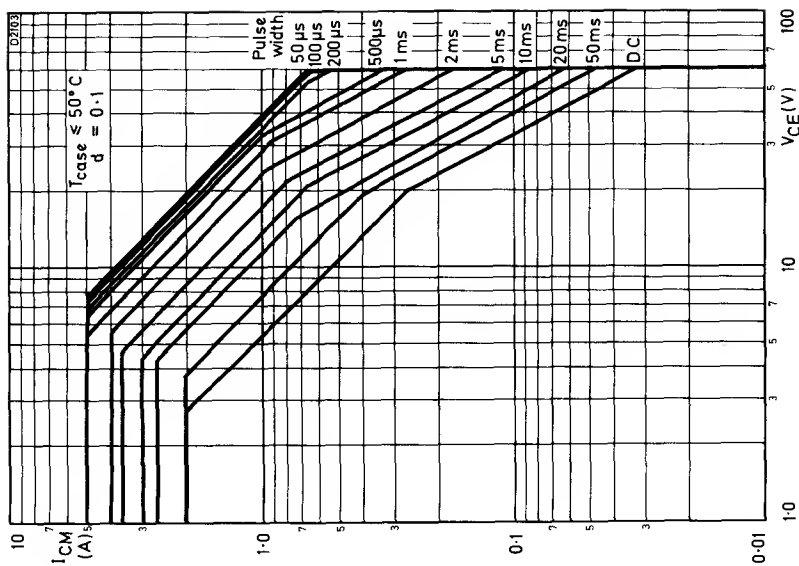
DERATING AGAINST MOUNTING-BASE TEMPERATURE

The maximum permissible power for selected pulse widths and/or mounting-base temperature can be obtained from the graphs on pages 5, 6 and 7, where the P_{\max} value for $T_{mb} \leq 50^{\circ}\text{C}$ is calculated from the line of constant power (i.e. that part of the curve which has a slope of -1), on the relevant I_C versus V_{CE} curve.

For mounting-base temperatures in excess of 50°C , the constant power line BC in figures 2A and 2B is reduced to the % of P_{\max} as read from the % P_{\max} versus T_{mb} graph on page 5. The safe operating area for the higher temperature is defined either by the points A B' D' D E in figure 2A, or by the points A B' D' E in figure 2B. The second-breakdown power line is only modified by the intersection point D' and is not adjusted against temperature in any other way.

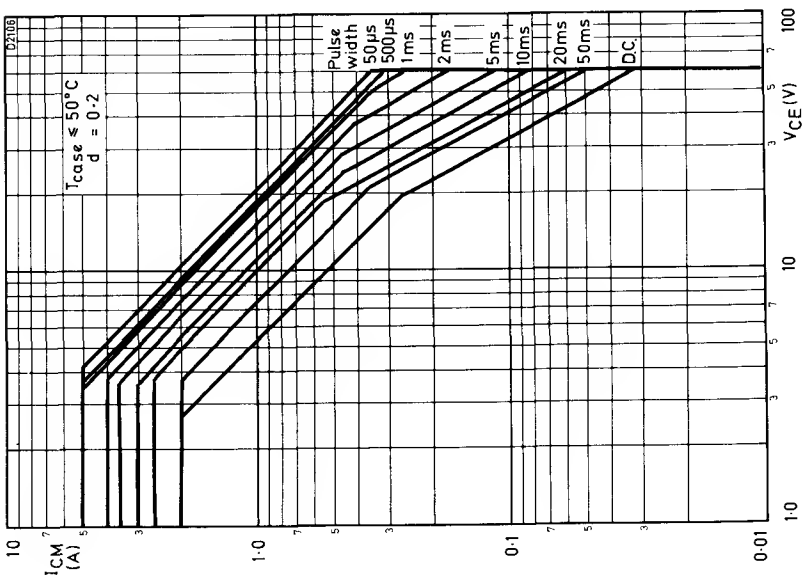
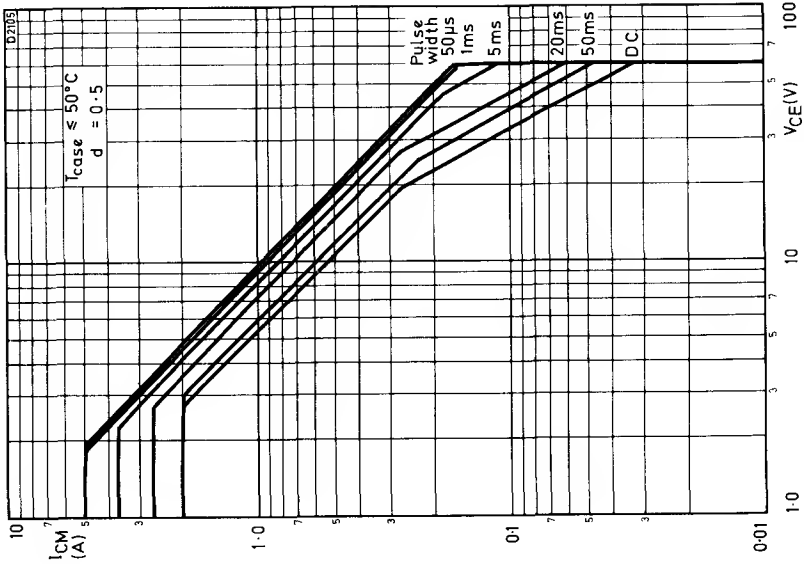




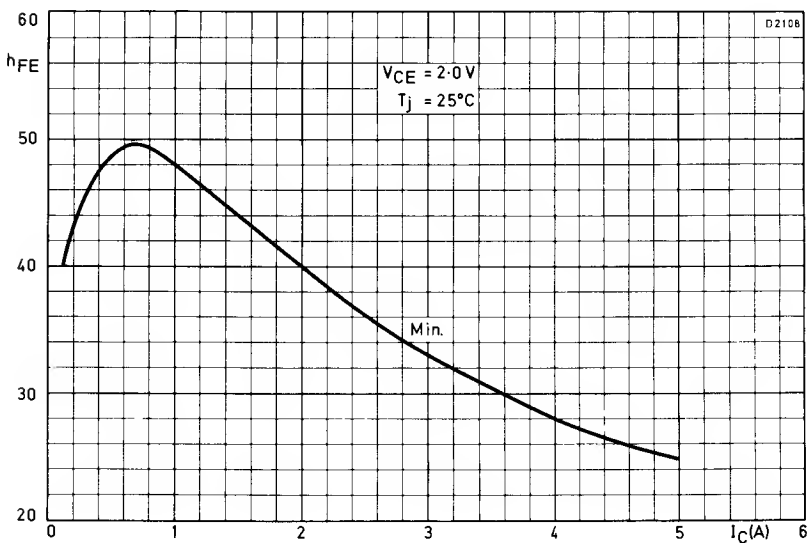
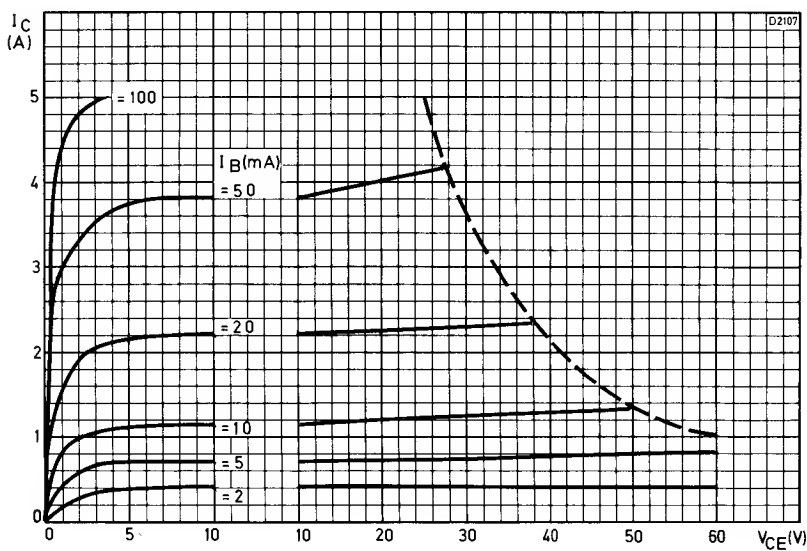


N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BSV64

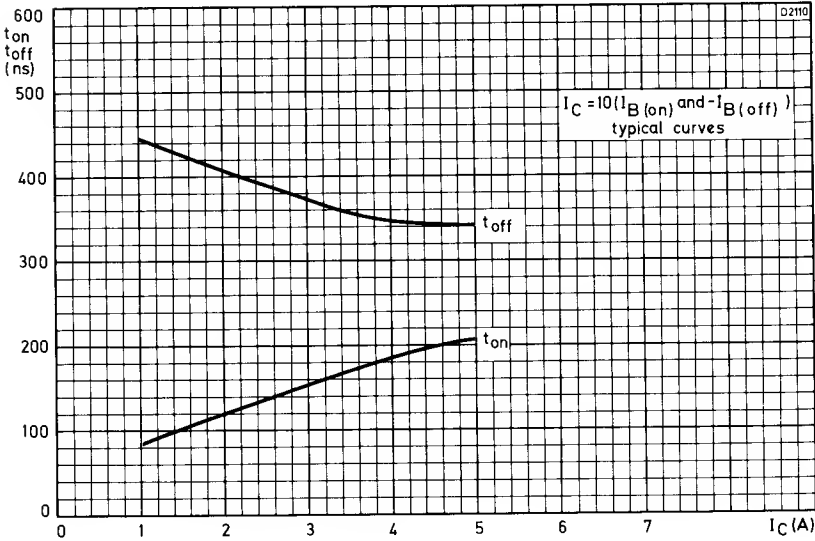
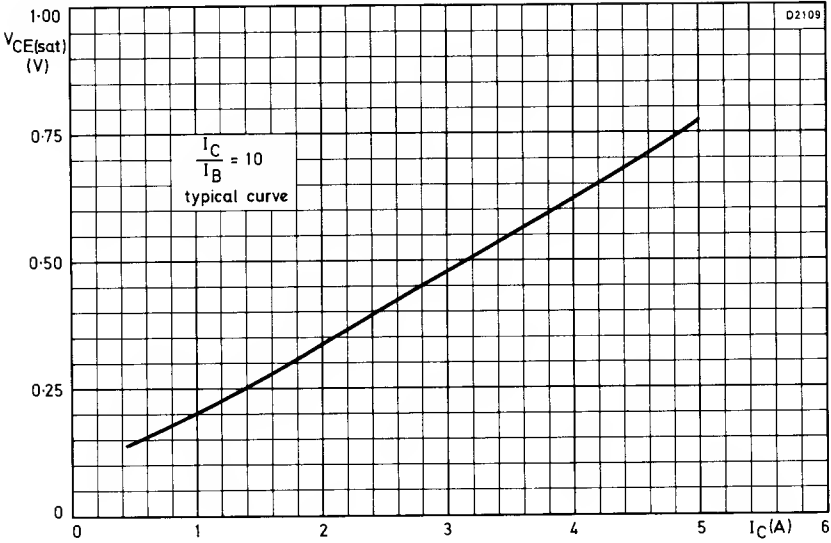


Mullard



N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BSV64



P-N-P SILICON PLANAR EPITAXIAL TRANSISTOR

BSV68

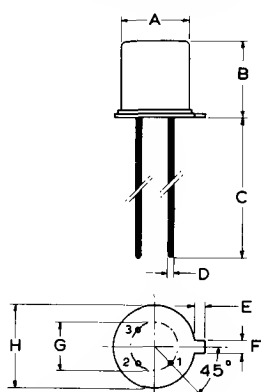
Silicon planar epitaxial transistor intended for anode switching in dynamically driven numerical indicator tubes.

QUICK REFERENCE DATA

$-V_{CER}$ max. ($R_{BE} = 10k\Omega$)	110	V
$-V_{CEO}$ max.	100	V
$-I_{CM}$ max.	100	mA
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	250	mW
T_j max.	150	$^{\circ}C$
h_{FE} min. ($-I_C = 25mA$, $-V_{CE} = 5V$)	30	
f_T typ. ($-I_C = 25mA$, $-V_{CE} = 5V$, $f = 35MHz$)	95	MHz

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18



Millimetres

	Min.	Typ.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	-	0.48
E	-	-	1.17
F	-	-	1.16
G	-	2.54	-
H	-	-	5.8

Viewed from underside

- Connections:
1. Emitter
 2. Base
 3. Collector connected to envelope

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max. ($-I_C = 10\mu A$)	110	V
$-V_{CER}$ max. ($-I_C = 10\mu A$, $R_{BE} = 10k\Omega$)	110*	V
$-V_{CEO}$ max. ($-I_C = 100\mu A$)	100	V
$-V_{EBO}$ max. ($-I_E = 10\mu A$)	6.0	V
$-I_C$ max.	100	mA
$-I_{CM}$ max.	100†	mA
$-I_{BM}$ max.	100	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	250	mW

Temperature

T_{stg}	-65 to +150	$^\circ C$
T_j max.	150	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.5	degC/mW
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
$-I_{CBO}$	Collector-base cut-off current $I_E = 0$, $-V_{CB} = 100V$, $T_j = 70^\circ C$	-	-	10	μA
$-I_{CER}$	Collector-emitter cut-off current $-V_{CE} = 110V$, $R_{BE} = 10k\Omega$	-	-	10	μA
$-I_{EBO}$	Emitter-base cut-off current $I_C = 0$, $-V_{EB} = 6V$	-	-	10	μA

*The transistor may be operated in the breakdown region, provided the collector current does not exceed $10\mu A$ at $T_{amb} = 70^\circ C$.

It can withstand an inductive load of 4mH in series with a resistance of $4k\Omega$, combined with a collector current of 25mA before switching-off.

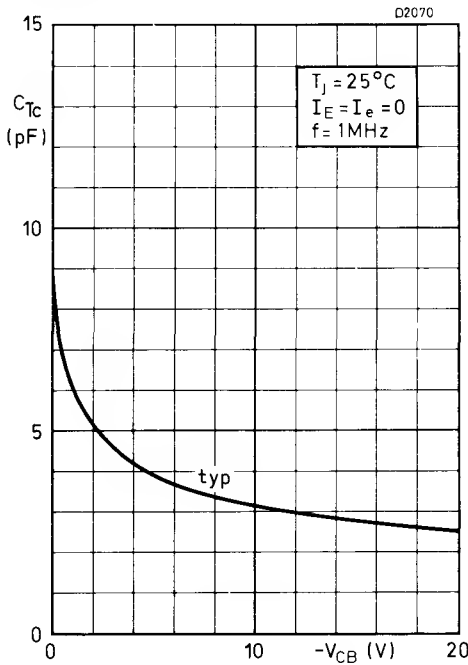
†The transistor can withstand a capacitive load of 100pF, combined with a collector voltage equal to $-V_{CER}$ before switching-on.

P-N-P SILICON PLANAR
EPITAXIAL TRANSISTOR

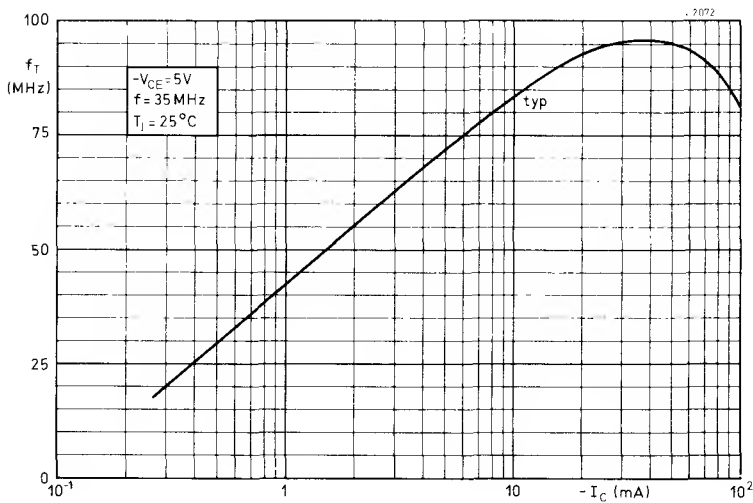
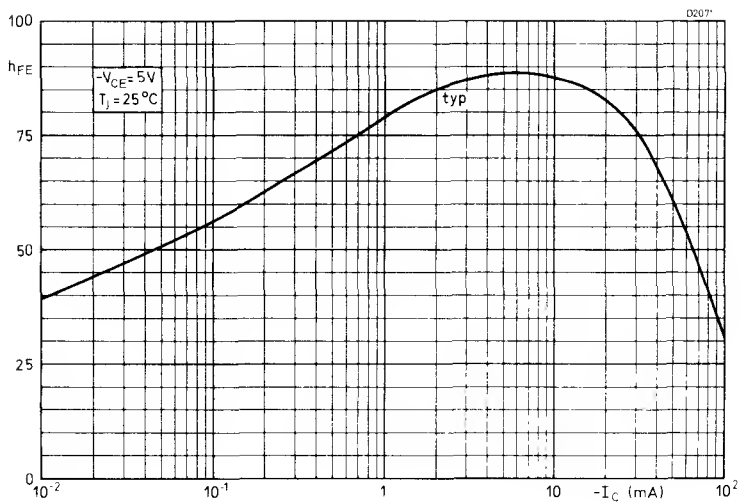
BSV68

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
$-V_{CE(sat)}$	Collector-emitter saturation voltage $-I_C = 25\text{mA}, -I_B = 2.5\text{mA}$	-	-	250	mV
$-V_{BE(sat)}$	Base-emitter saturation voltage $-I_C = 25\text{mA}, -I_B = 2.5\text{mA}$	-	-	900	mV
h_{FE}	Static forward current transfer ratio $-I_C = 10\text{mA}, -V_{CE} = 5\text{V}$ $-I_C = 25\text{mA}, -V_{CE} = 5\text{V}$	30 30	- -	- -	
C_{Tc}	Collector capacitance $I_E = I_e = 0, -V_{CB} = 10\text{V}, f = 1\text{MHz}$	-	-	5.0	pF
f_T	Transition frequency $-I_C = 25\text{mA}, -V_{CE} = 5\text{V},$ $f = 35\text{MHz}$	50	95	-	MHz



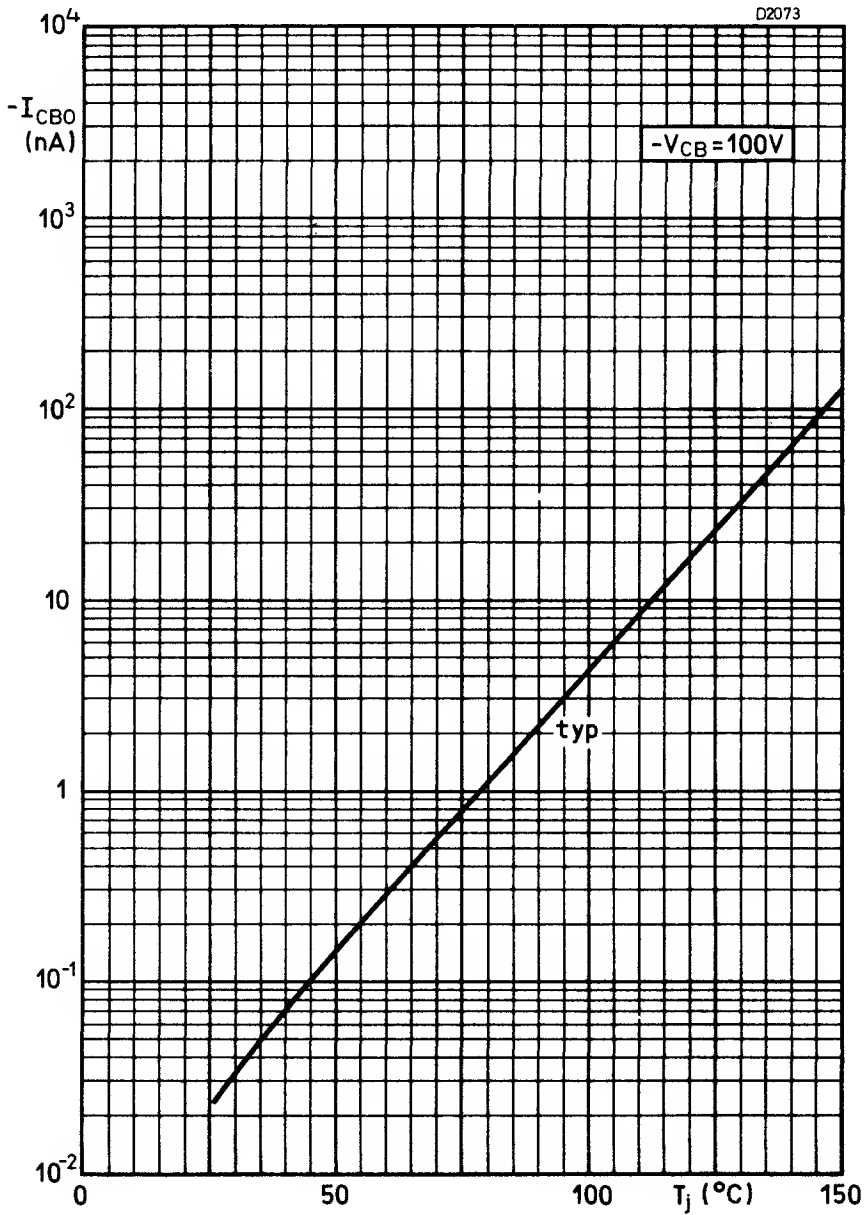
Mullard



N-CH
FIEL

P-N-P SILICON PLANAR
EPITAXIAL TRANSISTOR

BSV68



OUTL



All dim

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Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DS} max.	Drain-source voltage	40	V
V_{DGO} max.	Drain-gate voltage (open source)	40	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	V
I_G max.	Forward gate current	50	mA
P_{tot} max.	Total power dissipation, $T_{amb} \leq 25^{\circ}\text{C}$	350	mW

Temperature

T_{stg}	Storage temperature	-65 to +200	$^{\circ}\text{C}$
T_j max.	Junction temperature	175	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance from junction to ambient in free air	0.43	degC/mW
-----------------	---	------	---------

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}$ unless otherwise stated)

			Min.	Typ.	Max.	
$-I_{GSS}$	Gate cut-off current					
	$-V_{GS} = 20\text{V}$, $V_{DS} = 0$		-	-	0.25	nA
	$-V_{GS} = 20\text{V}$, $V_{DS} = 0$, $T_j = 150^{\circ}\text{C}$		-	-	0.5	μA
I_D	Drain cut-off current					
	$V_{DS} = 15\text{V}$, $-V_{GS} = 12\text{V}$		-	-	0.25	nA
	$V_{DS} = 15\text{V}$, $-V_{GS} = 12\text{V}$, $T_j = 150^{\circ}\text{C}$		-	-	0.5	μA
I_{DSS}	Drain current					
	$V_{DS} = 15\text{V}$, $V_{GS} = 0$	BSV78	50	-	-	mA
		BSV79	20	-	-	mA
		BSV80	10	-	-	mA
$-V_{(P)GS}$	Gate-source cut-off voltage					
	$I_D = 1\text{nA}$, $V_{DS} = 15\text{V}$	BSV78	3.75	-	11	V
		BSV79	2.0	-	7.0	V
		BSV80	1.0	-	5.0	V

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

BSV78
BSV79
BSV80

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
-V _{GS}	Gate-source voltage I _D = 1.5μA, V _{DS} = 15V	BSV78	3.5	-	10	V
		BSV79	1.75	-	6.0	V
		BSV80	0.75	-	4.0	V
V _{DS(on)}	Drain-source 'on' voltage I _D = 20mA, V _{GS} = 0	BSV78	-	-	500	mV
		BSV79	-	-	400	mV
		BSV80	-	-	325	mV
r _{DS(on)}	Drain-source 'on' resistance I _D = 0, V _{GS} = 0, f = 1kHz	BSV78	-	-	25	Ω
		BSV79	-	-	40	Ω
		BSV80	-	-	60	Ω
y-parameters at f = 1MHz (common source)						
-V _{GS} = 10V, V _{DS} = 0						
C _{is}	Input capacitance		-	-	10	pF
-C _{rs}	Feedback capacitance		-	-	5	pF

Switching characteristics (see test circuit on page 4)

Turn-on time when switched from:

$-V_{GSM} = 11V$ to $I_D = 20mA, V_{DD} = 10V$ (BSV78)

$-V_{GSM} = 7V$ to $I_D = 10mA, V_{DD} = 10V$ (BSV79)

$-V_{GSM} = 5V$ to $I_D = 5mA, V_{DD} = 10V$ (BSV80)

			BSV78	BSV79	BSV80	
t_d	Delay time	max.	5.0	10	8.0	ns
t_r	Rise time	max.	5.0	5.0	7.0	ns
t_{on}	Turn-on time	max.	10	15	15	ns

Switching characteristics (contd.)

Turn-off time when switched from:

$$I_D = 20\text{mA to } -V_{GSM} = 11\text{V}, V_{DD} = 10\text{V (BSV78)}$$

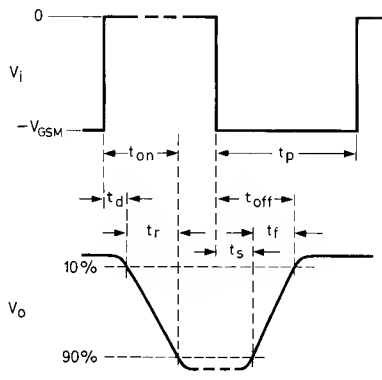
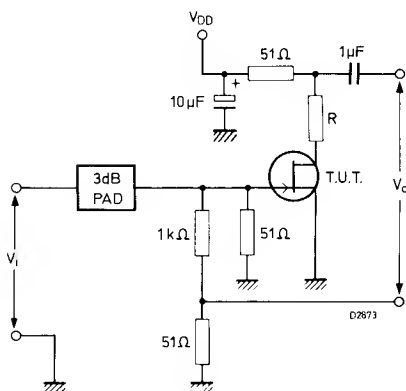
$$I_D = 10\text{mA to } -V_{GSM} = 7\text{V}, V_{DD} = 10\text{V (BSV79)}$$

$$I_D = 5\text{mA to } -V_{GSM} = 5\text{V}, V_{DD} = 10\text{V (BSV80)}$$

		BSV78	BSV79	BSV80	
t_f	Fall time	6.0	10	20	ns
t_s	Storage time	4.0	5.0	5.0	ns
t_{off}	Turn-off time	10	15	25	ns

Test circuit:

Input and output waveforms:



$$R_L = \frac{10 - V_{DS(on)}}{I_{D(on)}} - 51\Omega$$

BSV78	BSV79	BSV80
$R_L = 424$	$R_L = 909$	$R_L = 1885 \Omega$

Pulse generator:

$$R_1 = 50\Omega$$

$$t_r < 0.5\text{ns}$$

$$t_f < 5\text{ns}$$

Oscilloscope:

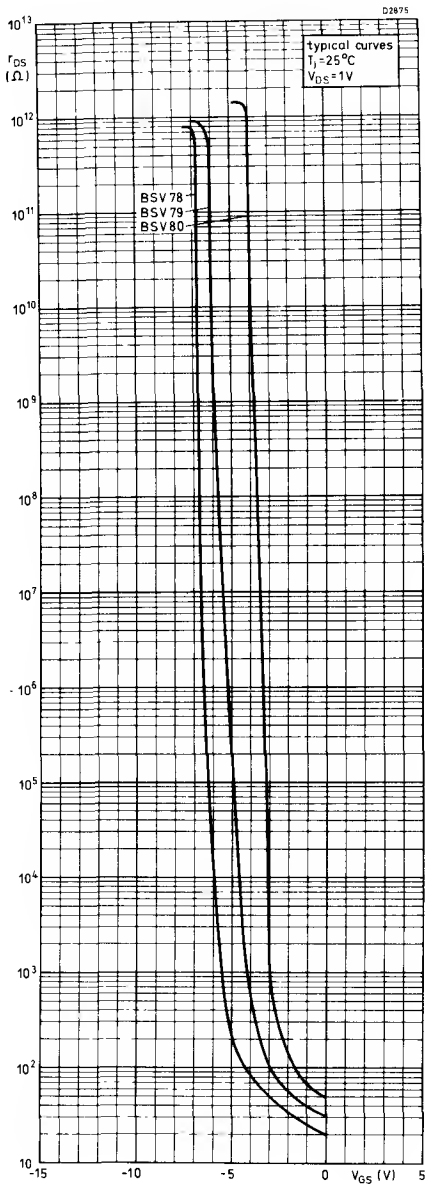
$$R_1 = 50\Omega$$

$$t_r < 1\text{ns}$$

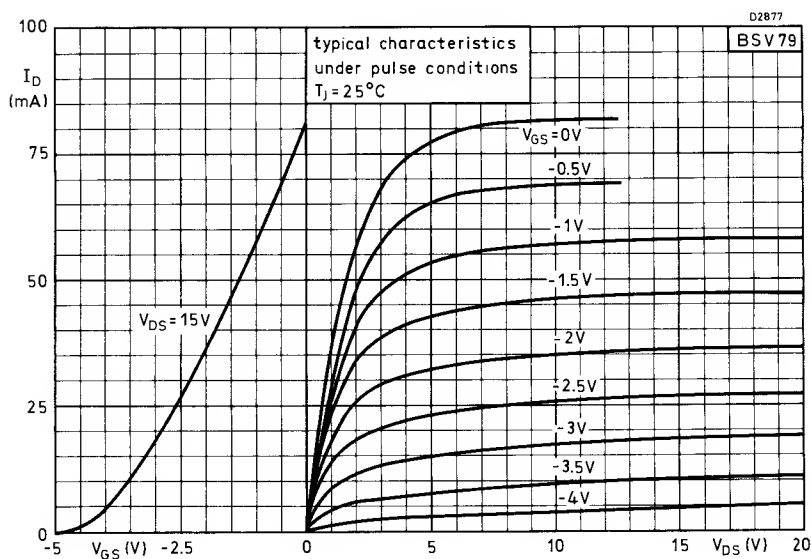
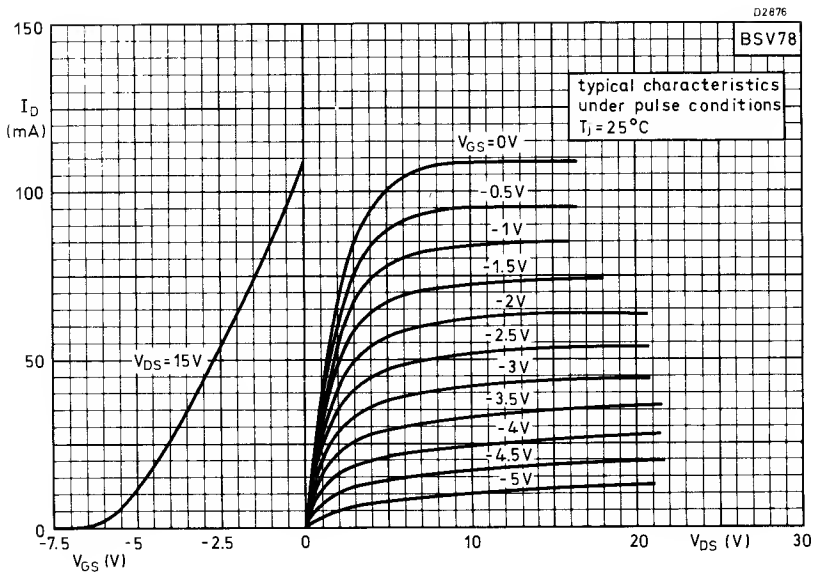
$$t_f < 1\text{ns}$$

N-CHANNEL SILICON
FIELD-EFFECT TRANSISTORS

BSV78
BSV79
BSV80

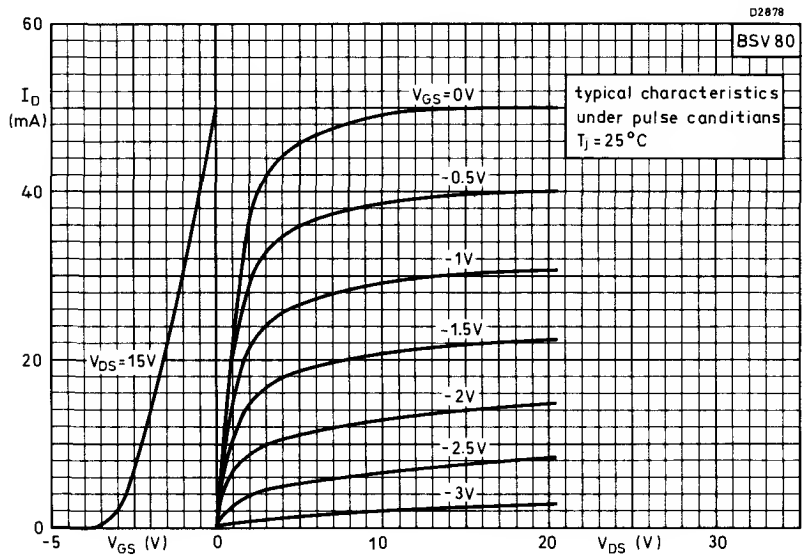


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**N-CHANNEL SILICON
FIELD-EFFECT TRANSISTORS**

**BSV78
BSV79
BSV80**



N-CHANNEL INSULATED GATE
FIELD EFFECT TRANSISTOR

BSV81

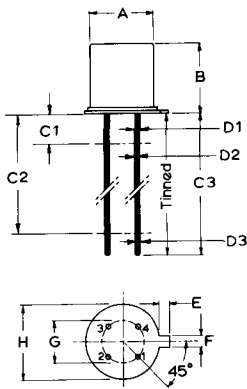
Depletion type, insulated gate, field effect transistor in a TO-72 metal envelope, with the substrate connected to the case. It is intended for chopper and other special switching applications e.g. timing circuits, multiplex circuits etc.
The BSV81 features a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

$r_{DS(on)}$ max. ($V_{DS}=0$, $V_{GS}=5V$, $V_{BS}=0$, $f=1kHz$)	50	Ω
$r_{DS(off)}$ min. ($V_{DS}=10V$, $-V_{GS}=5V$, $V_{BS}=0$)	10	$G\Omega$
$-C_{rs}$ max. ($-V_{GS}=5V$, $V_{DS}=0$, $I_B=0$, $f=1MHz$)	0.5	pF
$-C_{rd}$ max. ($-V_{GD}=5V$, $V_{SD}=0$, $I_B=0$, $f=1MHz$)	1.2	pF

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



Viewed from underside

Millimetres

	Min.	Nom.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections

- 1. Drain
- 2. Source
- 3. Gate
- 4. Substrate connected to envelope

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DB} max.	Drain-substrate voltage	30	V
V_{SB} max.	Source-substrate voltage	30	V
$+V_{GB}$ max.	Gate-substrate voltage (continuous)	10	V
$+V_{G-N}$ max.	Repetitive peak gate voltage (gate to all other terminals) $V_{SB} = V_{DB} = 0$, $f > 100\text{Hz}$	15	V
$+V_{G-N}$ max.	Non-repetitive peak gate voltage (gate to all other terminals) $V_{SB} = V_{DB} = 0$, $t < 10\text{ms}$	50	V
I_{DM} max.	Peak drain current $t_r = 20\text{ms}$, $d = 0.1$	50	mA
I_{SM} max.	Peak source current $t_r = 20\text{ms}$, $d = 0.1$	50	mA
P_{tot} max.	Total power dissipation $T_{amb} \leq 25^\circ\text{C}$	200	mW

Temperature

T_{stg}	Storage temperature	-65 to +125	$^\circ\text{C}$
T_j max.	Junction temperature	125	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance, junction to ambient, in free air	0.5	degC/mW
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Max.	
I_{DSX}	Drain cut-off current, $V_{BS} = 0$ $V_{DS} = 10\text{V}$, $-V_{GS} = 5\text{V}$	-	1.0	nA
	$V_{DS} = 10\text{V}$, $-V_{GS} = 5\text{V}$, $T_j = 125^\circ\text{C}$	-	1.0	μA
I_{SDX}	Source cut-off current, $V_{BD} = 0$ $V_{SD} = 10\text{V}$, $-V_{GD} = 5\text{V}$	-	1.0	nA
	$V_{SD} = 10\text{V}$, $-V_{GD} = 5\text{V}$, $T_j = 125^\circ\text{C}$	-	1.0	μA
$-I_{GSS}$	Gate current, $V_{BS} = 0$ $-V_{GS} = 10\text{V}$, $V_{DS} = 0$	-	10	pA
I_{GSS}	$V_{GS} = 10\text{V}$, $V_{DS} = 0$	-	10	pA
$-I_{GSS}$	$-V_{GS} = 10\text{V}$, $V_{DS} = 0$, $T_j = 125^\circ\text{C}$	-	200	pA
I_{GSS}	$V_{GS} = 10\text{V}$, $V_{DS} = 0$, $T_j = 125^\circ\text{C}$	-	200	pA

N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

BSV81

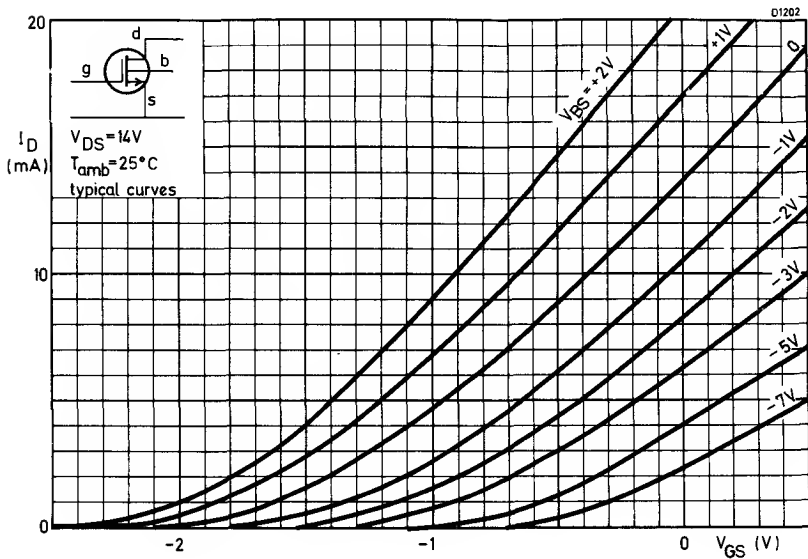
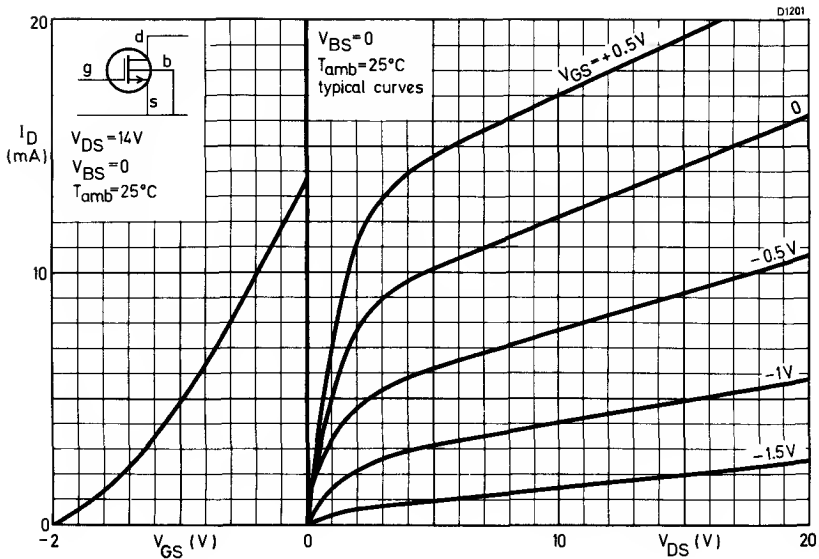
ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Max.	
	Substrate current, $V_{GB}=0$			
$-I_{BDO}$	$-V_{BD}=30V, I_S=0$	-	10	μA
$-I_{BSO}$	$-V_{BS}=30V, I_D=0$	-	10	μA
$r_{DS(on)}$	Drain-source 'on' resistance at $f=1kHz, V_{BS}=0$ $V_{GS}=0, V_{DS}=0$	-	100	Ω
	$V_{GS}=0, V_{DS}=0, T_j=125^\circ C$	-	150	Ω
	$+V_{GS}=5V, V_{DS}=0$	-	50	Ω
$r_{DS(off)}$	Drain-source 'off' resistance $-V_{GS}=5V, V_{DS}=10V, V_{BS}=0$	10	-	$G\Omega$
	Feedback capacitance at $f=1MHz$			
$-C_{rs}$	$-V_{GS}=5V, V_{DS}=0, I_B=0$	-	0.5	pF
$-C_{rd}$	$-V_{GD}=5V, V_{SD}=0, I_B=0$	-	1.2	pF
	Gate to all other terminals capacitance at $f=1MHz$			
C_{g-n}	$-V_{GB}=5V, V_{SB}=V_{DB}=0$	-	5.0	pF

OPERATING NOTE

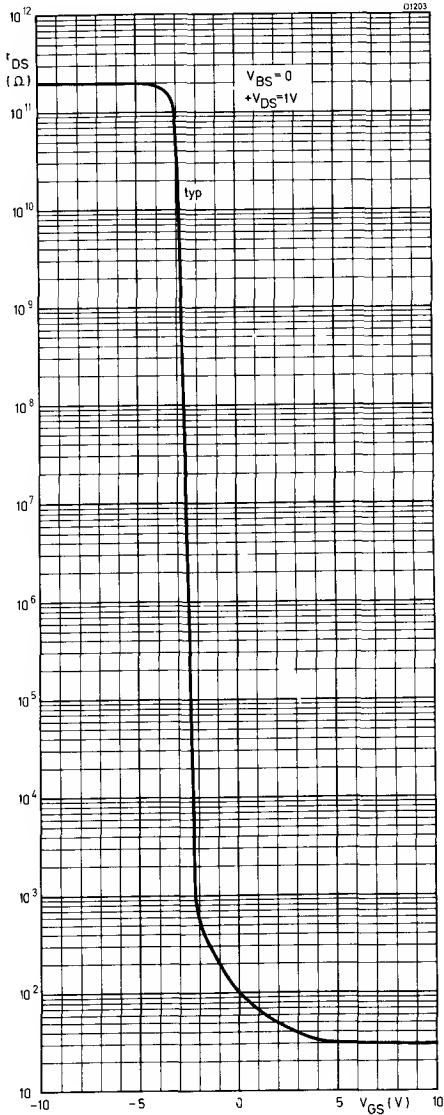
Mounting and handling instructions

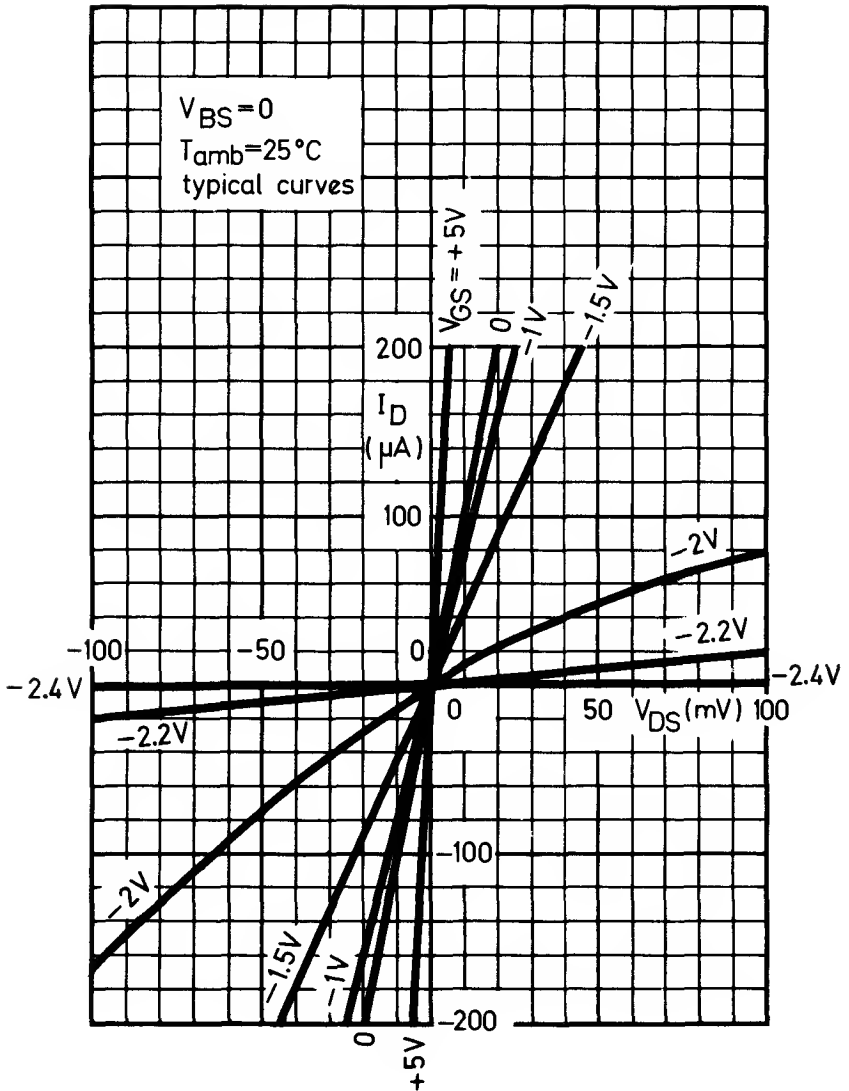
To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conductive rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.



N-CHANNEL INSULATED GATE
FIELD EFFECT TRANSISTOR

BSV81





N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BSW66
BSW67
BSW68

N-P-N silicon planar epitaxial transistors intended for highly inductive load switching.

QUICK REFERENCE DATA

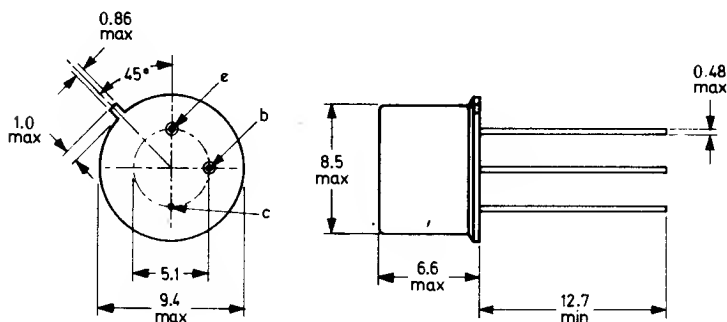
	BSW66	BSW67	BSW68	
V_{CBO} max.	100	120	150	V
V_{CEO} max.	100	120	150	V
I_{CM} max.	2.0			A
P_{tot} max. $T_{case} = 100^{\circ}\text{C}$	2.85			W
$T_{amb} = 45^{\circ}\text{C}$	0.7			W
E max., $L = 150\text{mH}$	5.0			mWs
T_j max.	200			$^{\circ}\text{C}$
h_{FE} min., $V_{CE} = 5\text{V}$, $I_C = 10\text{mA}$	30			
$V_{CE} = 5\text{V}$, $I_C = 500\text{mA}$	30			
$V_{CE(sat)}$ max., $I_C = 500\text{mA}$, $I_B = 50\text{mA}$	400	400	500	mV
f_T typ., $V_{CB} = 20\text{V}$, $-I_E = 100\text{mA}$, $f = 35\text{MHz}$	80			MHz

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-3/SB3-3A
J.E.D.E.C. TO-39

Collector connected to case



All dimensions in mm

D1574

Max. lead diameter is only guaranteed for 12.7mm

Accessories available:- 56218, 56245, 56265

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BSW66	BSW67	BSW68	
V_{CBO} max.	100	120	150	V
V_{CEO} max.	100	120	150	V
V_{EBO} max.	6.0			V
$I_{C(AV)}$ max. ($t_{av} \leq 20ms$)	1.0			A
I_{CM} max.	2.0			A
P_{tot} max. $T_{case} \leq 25^{\circ}C$	5.0			W
$T_{amb} \leq 25^{\circ}C$	0.8			W
E max. (switch-off energy, L = 150mH)	5.0			mWs

Temperature

T_{stg} range	-65 to +200	$^{\circ}C$
T_j max.	200	$^{\circ}C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ In free air	220	degC/W
$R_{th(j-case)}$	35	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}C$ unless otherwise stated)

			Min.	Typ.	Max.	
I _{CBO}	Collector cut-off current					
	V _{CB} = 1/2V _{CBO} max. I _E = 0		-	-	100	nA
	V _{CB} = 1/2V _{CBO} max. I _E = 0,					
	T _j = 150°C		-	-	50	μA
	V _{CB} = V _{CBO} max. I _E = 0		-	-	100	μA
I _{EBO}	Emitter cut-off current					
	V _{EB} = 3.0V, I _C = 0		-	-	100	nA
	V _{EB} = 6.0V, I _C = 0		-	-	100	μA
V _{(BR)CEO}	Collector-emitter breakdown voltage					
	I _C = 100mA, I _B = 0	BSW66	100	-	-	V
		BSW67	120	-	-	V
		BSW68	150	-	-	V

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

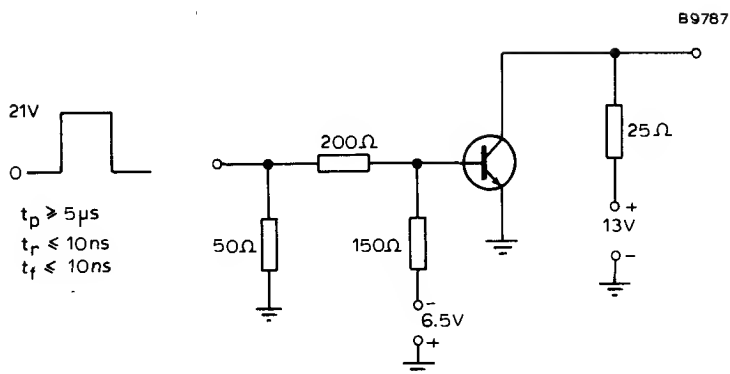
BSW66
BSW67
BSW68

ELECTRICAL CHARACTERISTICS (contd.)

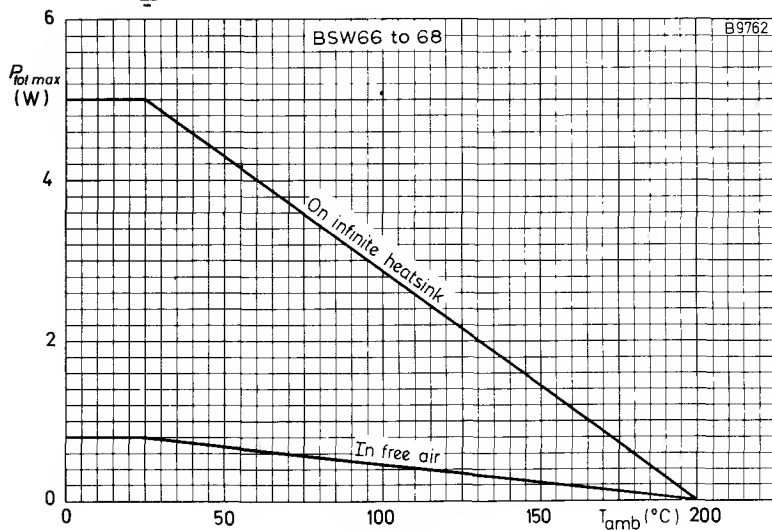
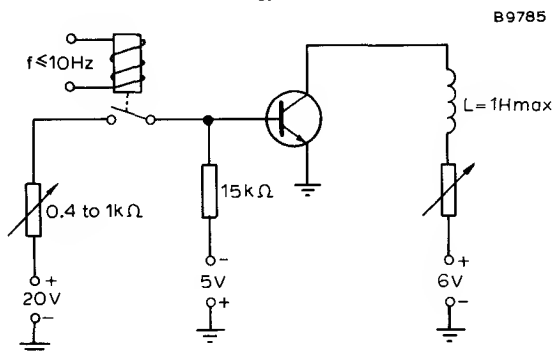
		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 100\text{mA}$, $I_B = 10\text{mA}$	-	-	150	mV
	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$				
	BSW66	-	-	400	mV
	BSW67	-	-	400	mV
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 100\text{mA}$, $I_B = 10\text{mA}$	-	-	0.9	V
	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$	-	-	1.1	V
h_{FE}	Static forward current transfer ratio				
	$I_C = 10\text{mA}$, $V_{CE} = 5.0\text{V}$	30	-	-	
	$I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$	40	-	-	
	$I_C = 500\text{mA}$, $V_{CE} = 5.0\text{V}$	30	-	-	
	$I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$	15	-	-	
f_T	Transition frequency				
	$-I_E = 100\text{mA}$, $V_{CB} = 20\text{V}$, $f = 35\text{MHz}$	-	80	-	MHz
C_{Tc}	Collector capacitance				
	$V_{CB} = 10\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	-	35	pF
C_{Te}	Emitter capacitance				
	$V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0\text{MHz}$	-	-	650	pF
Switching characteristics (see test circuits on page 4)					
t_{on}	Turn-on time				
	$I_C = 500\text{mA}$, $I_{Bon} = 50\text{mA}$, $-V_{BEoff} = 4\text{V}$	-	0.5	-	μs
t_{off}	Turn-off time				
	$I_C = 500\text{mA}$, $I_{Bon} = -I_{Boff} = 50\text{mA}$	-	1.0	-	μs

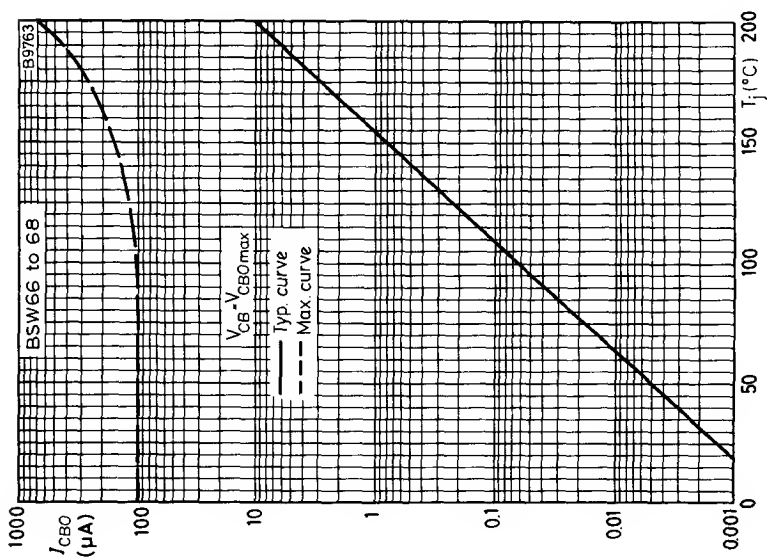
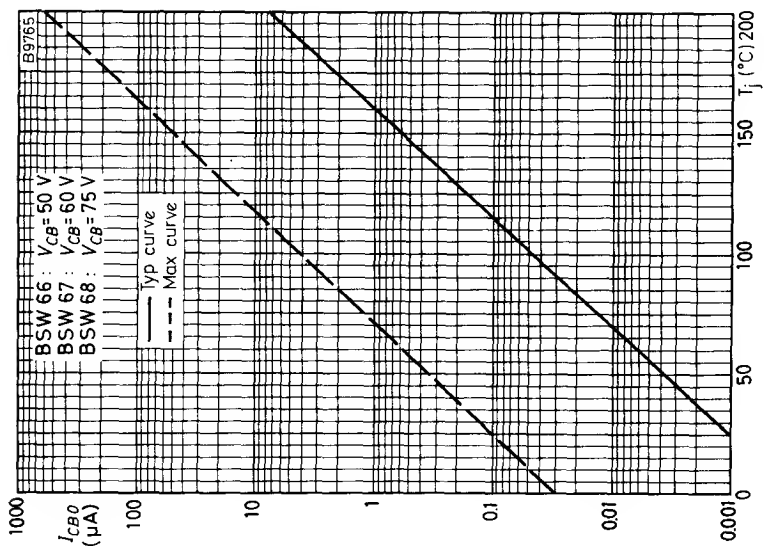
ELECTRICAL CHARACTERISTICS (cont'd)

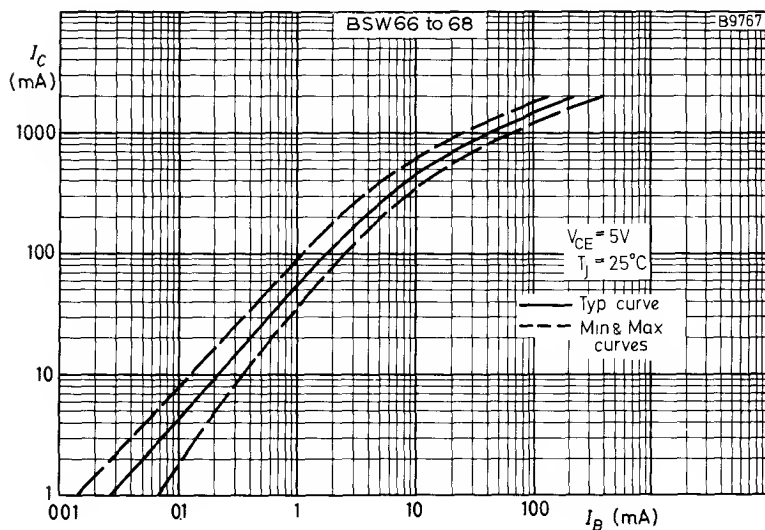
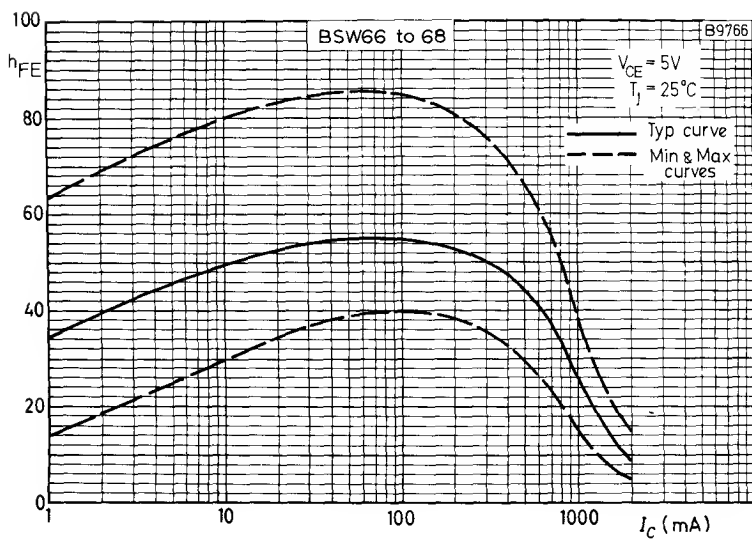
Test circuit for switching characteristics



Test circuit for switch-off energy

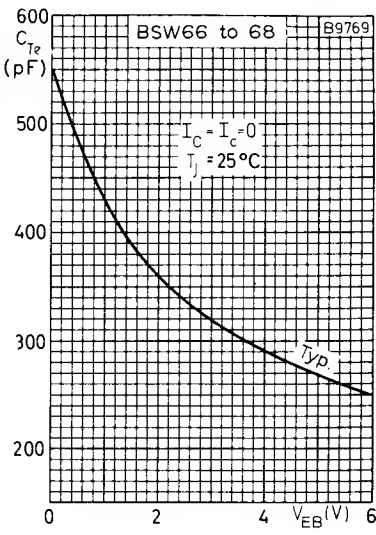
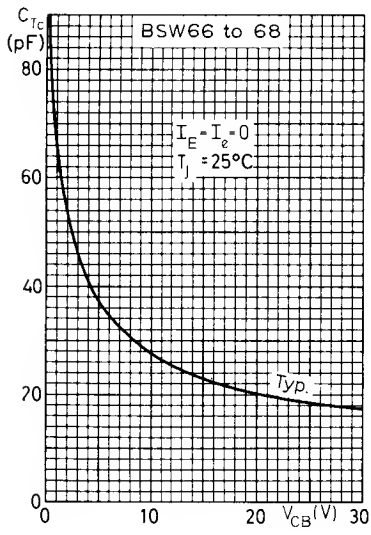
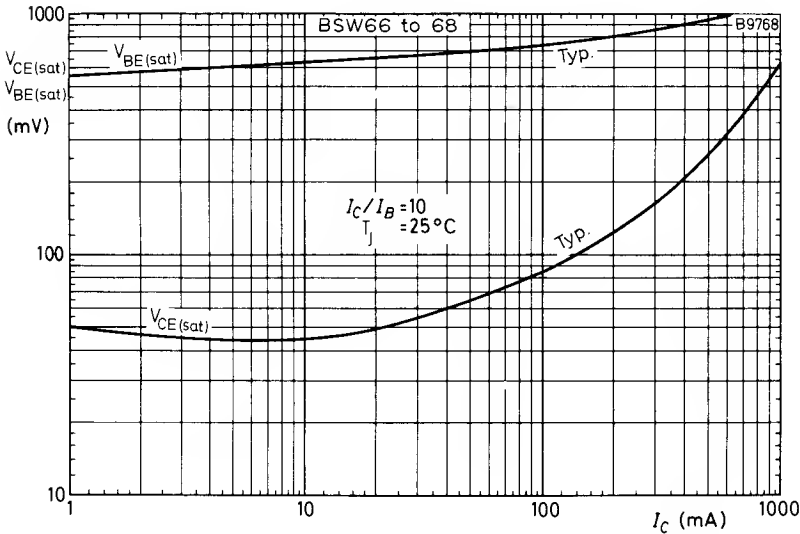


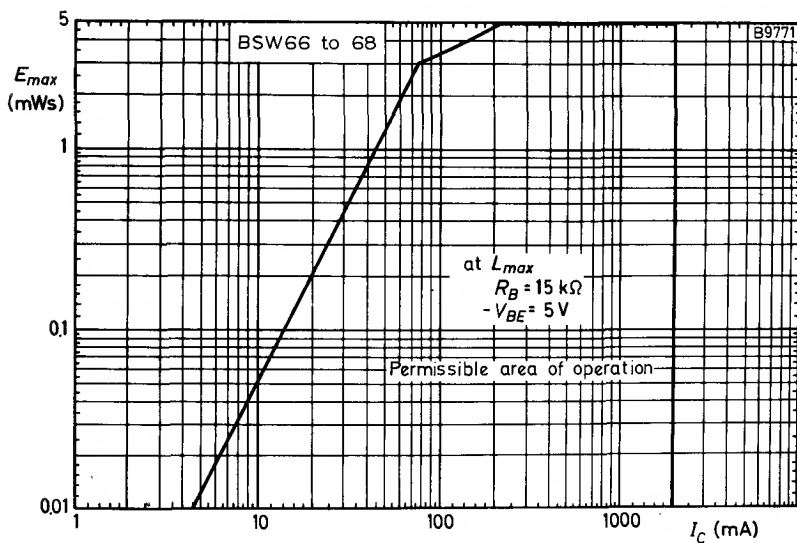
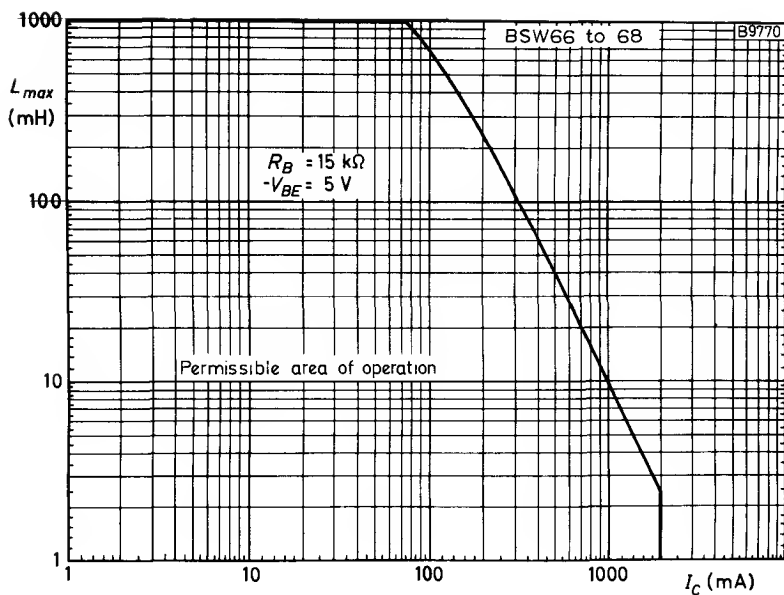




N-P-N SILICON PLANAR
EPITAXIAL TRANSISTORS

BSW66
BSW67
BSW68





SILICON N-P-N PLANAR EPITAXIAL TRANSISTORS

BSX19 BSX20

The BSX19 and BSX20 are n-p-n silicon planar epitaxial transistors, primarily intended for high-speed saturated switching and high frequency amplifier applications. TO-18 construction, collector connected to envelope.

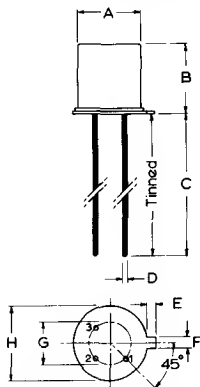
Unless otherwise shown data is applicable to both types

QUICK REFERENCE DATA			
	BSX19	BSX20	
V_{CBO} max. ($I_E = 0$)	40	V	
V_{CES} max. ($V_{BE} = 0$)	40	V	
V_{CEO} max. ($I_B = 0$)	15	V	
I_{CM} max.	500	mA	
P_{tot} max. ($T_{amb} = 25^{\circ}C$)	360	mW	
T_j max.	200	$^{\circ}C$	
h_{FE} ($I_C = 10mA$, $V_{CE} = 1.0V$)	20-60	40-120	
($I_C = 100mA$, $V_{CE} = 2.0V$)	>10	>20	
f_T min. ($I_C = 10mA$, $V_{CE} = 10V$)	400	500	Mc/s
t_s max. ($I_C = I_B = -I_{BM} = 10mA$)	10	13	ns

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-18

V.A.S.C.A. SO-12A/SB3-6A



Millimetres

	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.33
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections 1. Emitter

2. Base

3. Collector connected to envelope

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max. ($I_E = 0$)	40	V
V_{CES} max. ($V_{BE} = 0$)	40	V
V_{CEO} max. ($I_B = 0$, $I_C = 10\text{mA}$)	15	V
V_{EBO} max. ($I_C = 0$)	4.5	V
I_{CM} max. ($t = 10\mu\text{s}$)	500	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)	360	mW

Temperature

T_{stg} min.	-65	$^\circ\text{C}$
T_{stg} max.	200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Θ_{j-amb}	0.48 deg C/mW
Θ_{j-case}	0.15 deg C/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 20\text{V}$, $I_E = 0$	-	-	400*	nA
	$V_{CB} = 20\text{V}$, $I_E = 0$, $T_j = 150^\circ\text{C}$	-	-	30	μA
I_{CES}	Collector-emitter cut-off current				
	$V_{CE} = 15\text{V}$, $V_{BE} = 0$, $T_j = 55^\circ\text{C}$	-	-	0.4	μA
	$V_{CE} = 40\text{V}$, $V_{BE} = 0$	-	-	1.0	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 4.5\text{V}$, $I_C = 0$	-	-	10	μA
I_{BEX}	Base-emitter cut-off current				
	$V_{CE} = 15\text{V}$, $V_{BE} = -3.0\text{V}$, $T_j = 55^\circ\text{C}$	-	-	-0.6	μA
I_{CEX}	Collector-emitter cut-off current				
	$V_{CE} = 15\text{V}$, $V_{BE} = -3.0\text{V}$, $T_j = 55^\circ\text{C}$	-	-	0.6	μA

SILICON N-P-N PLANAR EPITAXIAL TRANSISTORS

BSX19 BSX20

			Min.	Typ.	Max.	
I_B	Base current					
	$I_E = -10\text{mA}$, $V_{CB} = 0$	BSX19	167*	-	500*	μA
		BSX20	83*	-	250*	μA
$V_{CEO(\text{sust})}$	Collector-emitter sustaining voltage					
	$I_C = 10\text{mA}$, $I_B = 0$		15*	-	-	V
$V_{CER(\text{sust})}$	$I_C = 10\text{mA}$, $R_{BE} = 10\Omega$		20	-	-	V
$V_{CE(\text{sat})}$	Collector-emitter saturation voltage					
	$I_C = 10\text{mA}$, $I_B = 1.0\text{mA}$		-	-	0.25*	V
	$I_C = 10\text{mA}$, $I_B = 0.6\text{mA}$	BSX19	-	-	0.3	V
	$I_C = 10\text{mA}$, $I_B = 0.3\text{mA}$	BSX20	-	-	0.3	V
	$I_C = 100\text{mA}$, $I_B = 10\text{mA}$		-	-	0.60	V
$V_{BE(\text{sat})}$	Base-emitter saturation voltage					
	$I_C = 10\text{mA}$, $I_B = 1.0\text{mA}$		0.70*	-	0.85*	V
	$I_C = 100\text{mA}$, $I_B = 10\text{mA}$		-	-	1.5	V
V_{BE}	Base-emitter voltage					
	$V_{CE} = 20\text{V}$, $I_C = 30\mu\text{A}$, $T_j = 100^\circ\text{C}$		0.35	-	-	V
h_{FE}	Static forward current transfer ratio					
	$I_C = 10\text{mA}$, $V_{CE} = 1.0\text{V}$	BSX19	20	-	60	
		BSX20	40	-	120	
	$I_C = 10\text{mA}$, $V_{CE} = 1.0\text{V}$,	BSX19	10	-	-	
	$T_j = -55^\circ\text{C}$	BSX20	20	-	-	
	$I_C = 100\text{mA}$, $V_{CE} = 2.0\text{V}$	BSX19	10	-	-	
		BSX20	20	-	-	
f_T	Transition frequency					
	$I_C = 10\text{mA}$, $V_{CE} = 10\text{V}$	BSX19	400	500	-	Mc/s
		BSX20	500	600	-	Mc/s

*These are the characteristics which are recommended for acceptance testing purposes.

Min. Typ. Max.

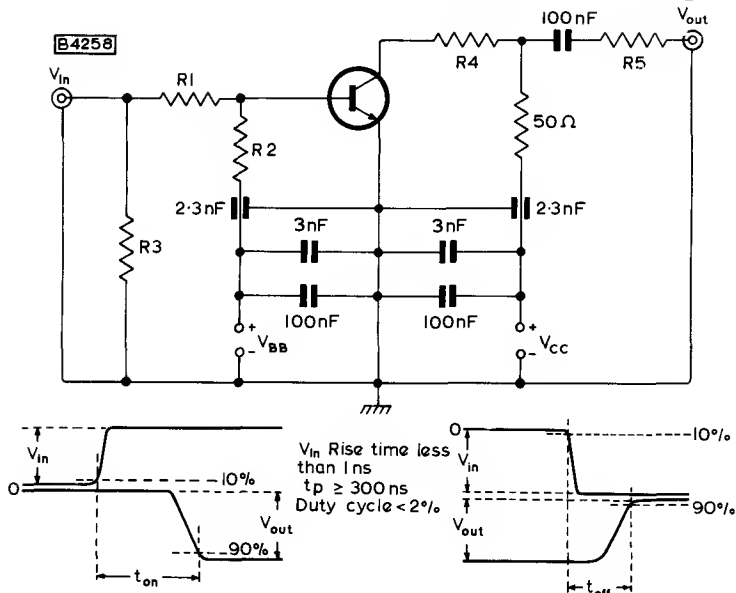
c_{tc} Collector capacitance
 $V_{CB} = 5.0V, I_E = I_c = 0,$
 $f = 1.0Mc/s$ - - 4.0 pF

c_{te} Emitter capacitance
 $V_{EB} = 1.0V, I_C = I_c = 0,$
 $f = 1.0Mc/s$ - - 4.5 pF

Switching characteristics

t_{on} Turn-on time (see Fig.1)
 $I_C = 10mA, I_B = 3.0mA$
 from $V_{BE} = -1.5V$ - - 12 ns
 $I_C = 100mA, I_B = 40mA$
 from $V_{BE} = -2.25V$ - - 7.0 ns

t_{off} Turn-off time (see Fig.1)
 $I_C = 10mA, I_B = 3.0mA,$
 $I_{BM} = -1.5mA$ BSX19 - - 15 ns
 BSX20 - - 18 ns
 $I_C = 100mA, I_B = 40mA,$
 $I_{BM} = -20mA$ BSX19 - - 18 ns
 BSX20 - - 21 ns



Mullard

SILICON N-P-N PLANAR
EPITAXIAL TRANSISTORS

BSX19
BSX20

Circuit conditions:

I_C (mA)	I_B (mA)	$-I_{BM}$ (mA)	V_{CC} (V)	$R_1 = R_2$ (k Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (k Ω)
10	3.0	1.5	3.0	3.3	50	220	0
100	40	20	6.0	0.33	56	0	1.0

t_{on}			t_{off}	
V_{BB} (V)	V_{BE} (V)	V_{in} (V)	V_{BB} (V)	V_{in} (V)
-3.0	-1.5	15	12	-15
-4.5	-2.25	20	15.3	-20

Note: $-I_{BM}$ is the reverse current that can flow during switching-off.
The indicated $-I_{BM}$ is determined and limited by the applied cut-off
voltage and series resistance.

		Min.	Typ.	Max.	
t_s	Storage time (see fig.2)				
	$I_C = I_B = -I_{BM} = 10\text{mA}$	BSX19	-	5.0	10 ns
		BSX20	-	6.0	13 ns

Storage time test circuit

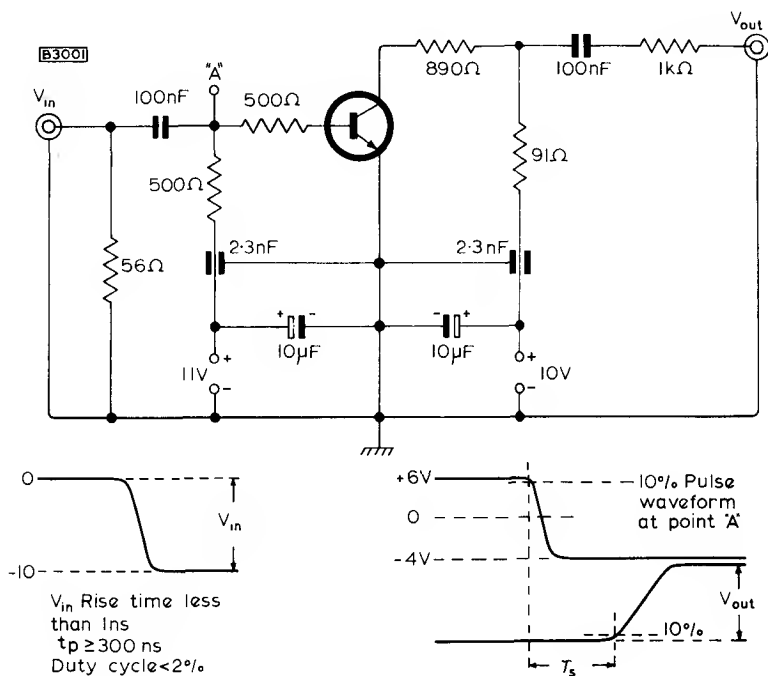
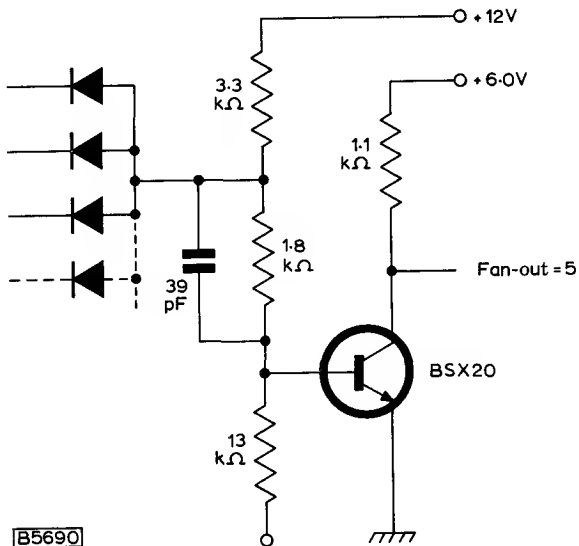


Fig. 2

TYPICAL CIRCUIT USING BSX20

NAND gate (Diode-transistor logic)

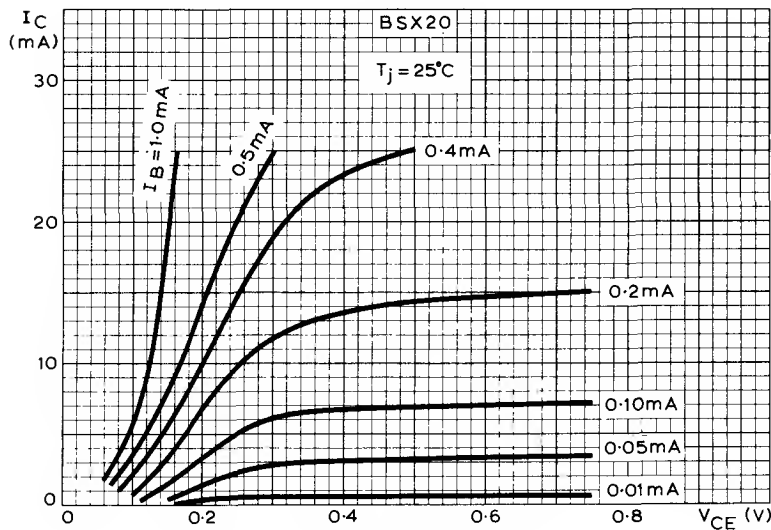
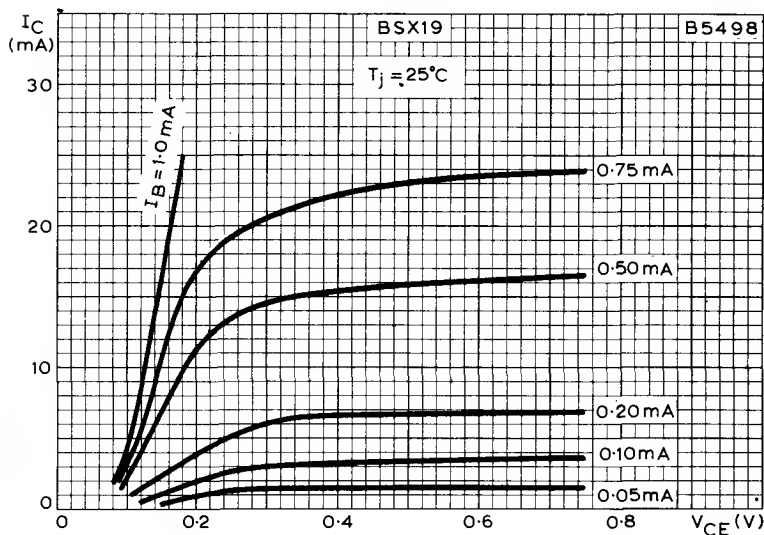


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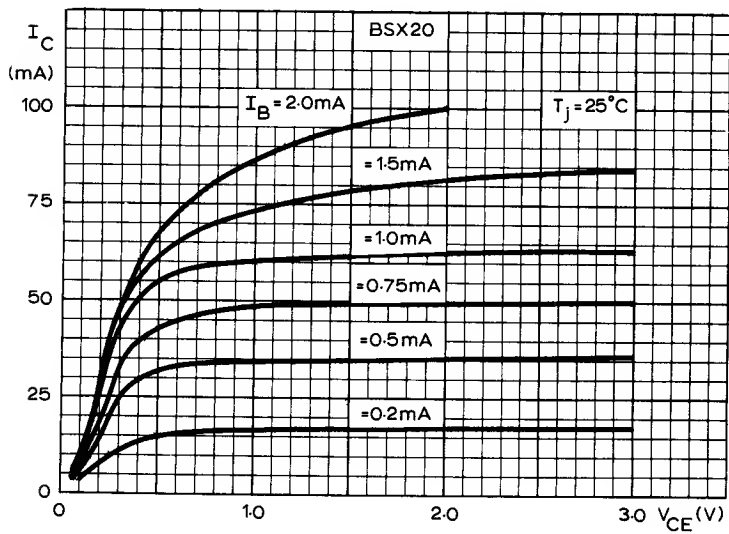
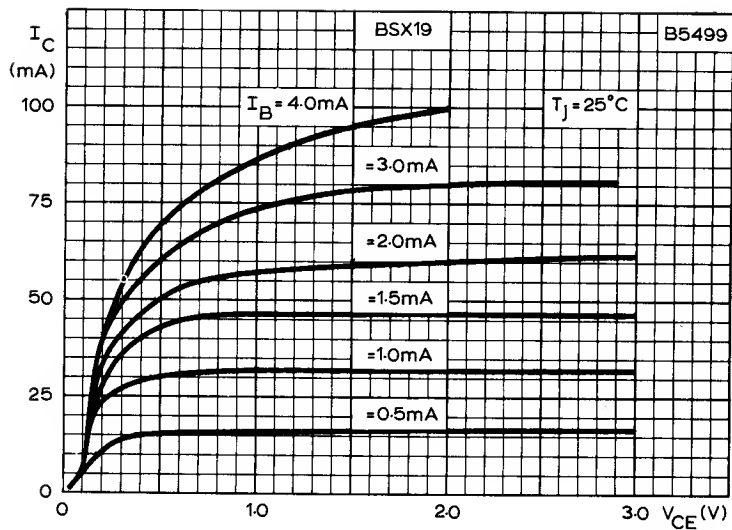
Typical delay time per stage $t_d = 15\text{ns}$, when 'fan-in' = 5

NOTE

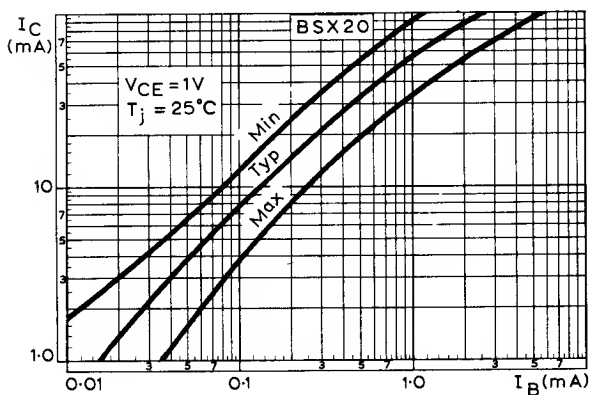
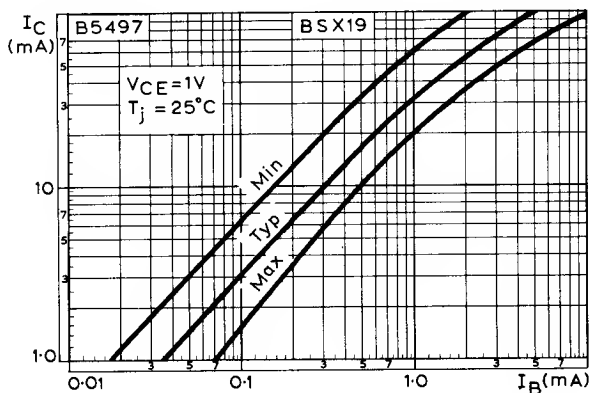
Fan-out=5 means that the circuit may be loaded by a maximum of five circuits, each presenting a load identical to that of one input branch of the input circuit itself.



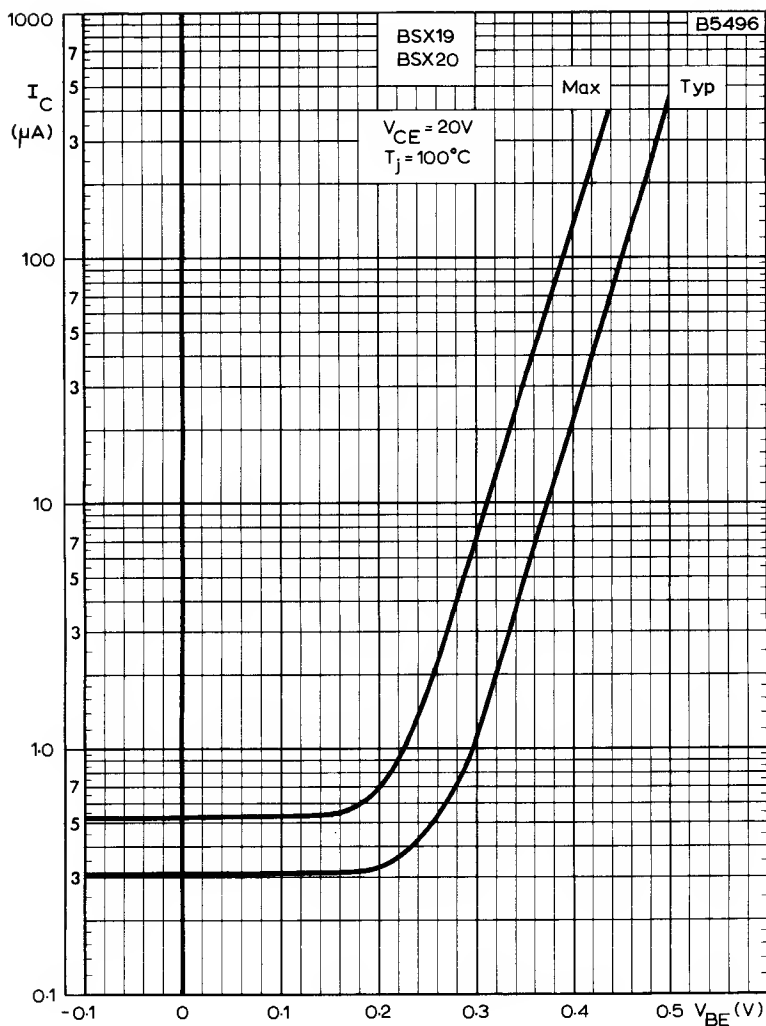
TYPICAL OUTPUT CHARACTERISTICS. $T_j = 25^\circ\text{C}$



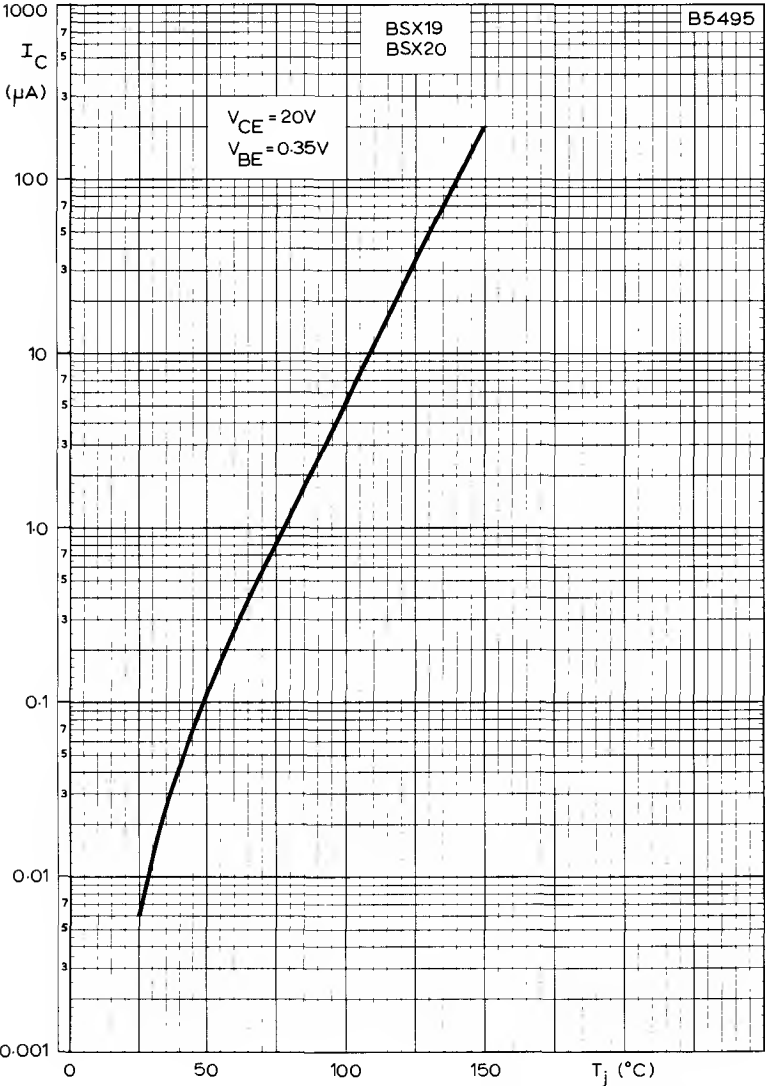
TYPICAL OUTPUT CHARACTERISTICS. $T_J = 25^\circ\text{C}$



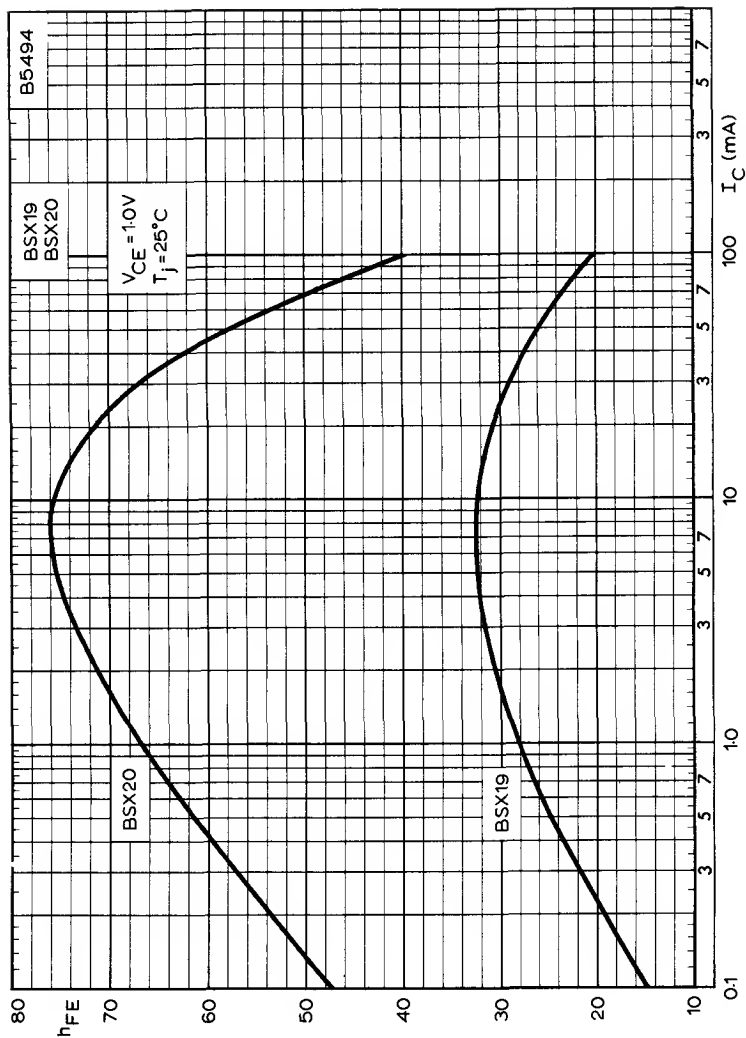
COLLECTOR CURRENT PLOTTED AGAINST BASE CURRENT



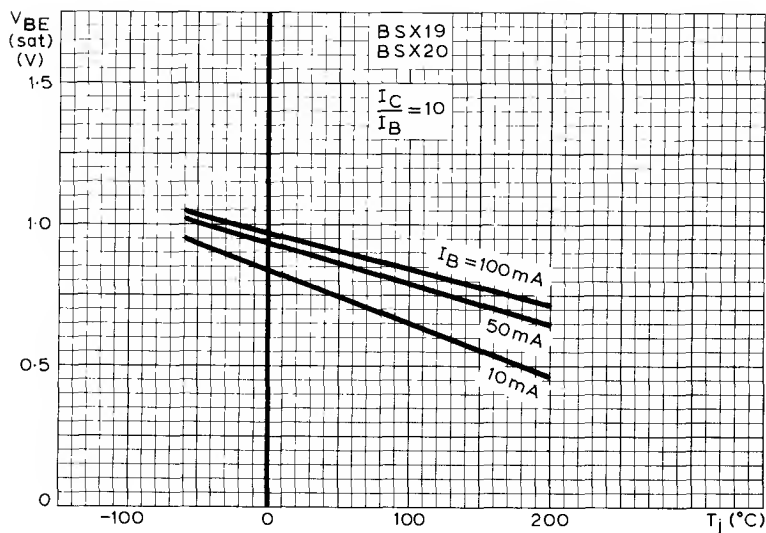
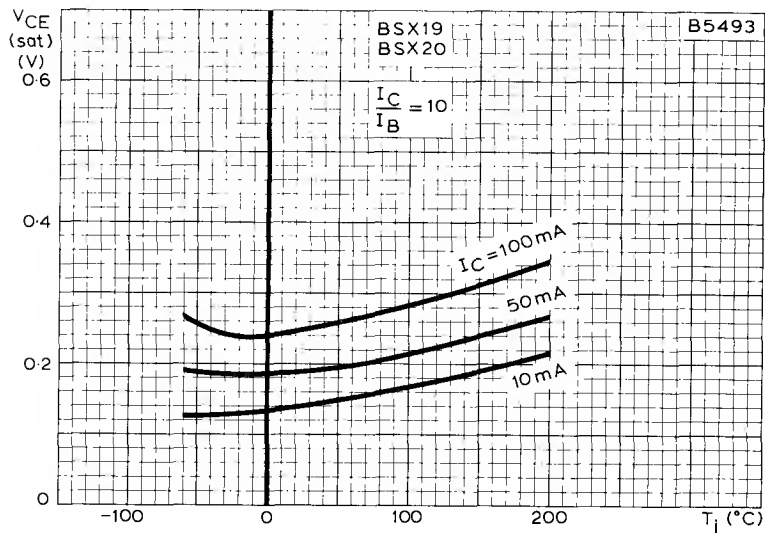
COLLECTOR CURRENT PLOTTED AGAINST BASE-EMITTER VOLTAGE



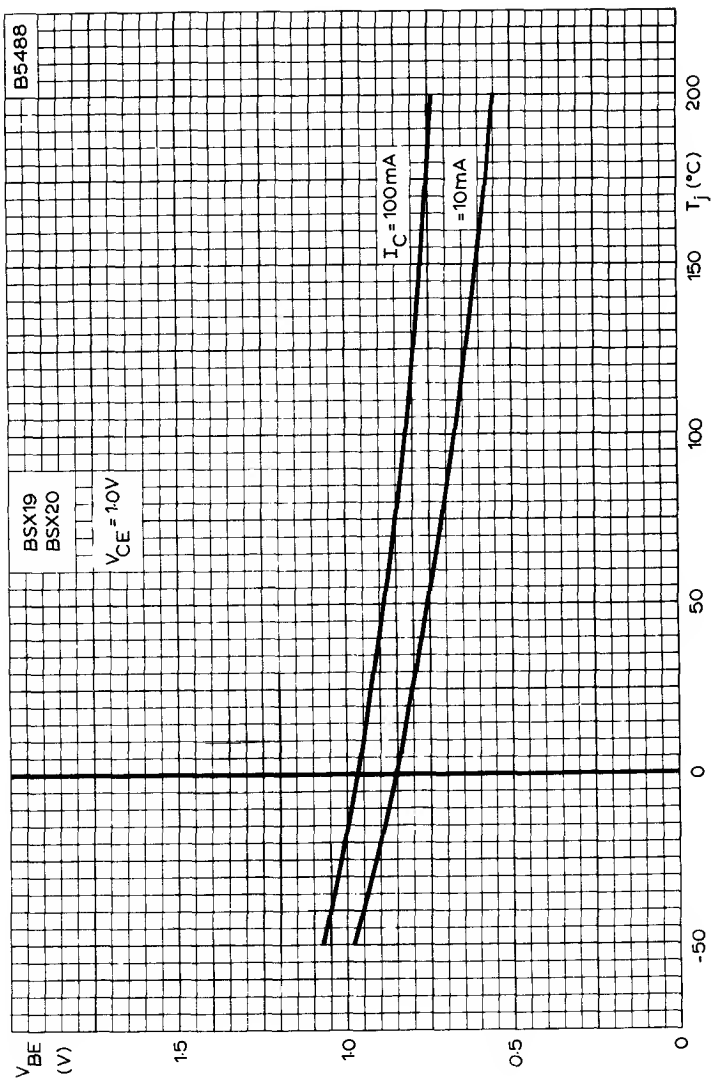
TYPICAL COLLECTOR CURRENT PLOTTED AGAINST JUNCTION
TEMPERATURE



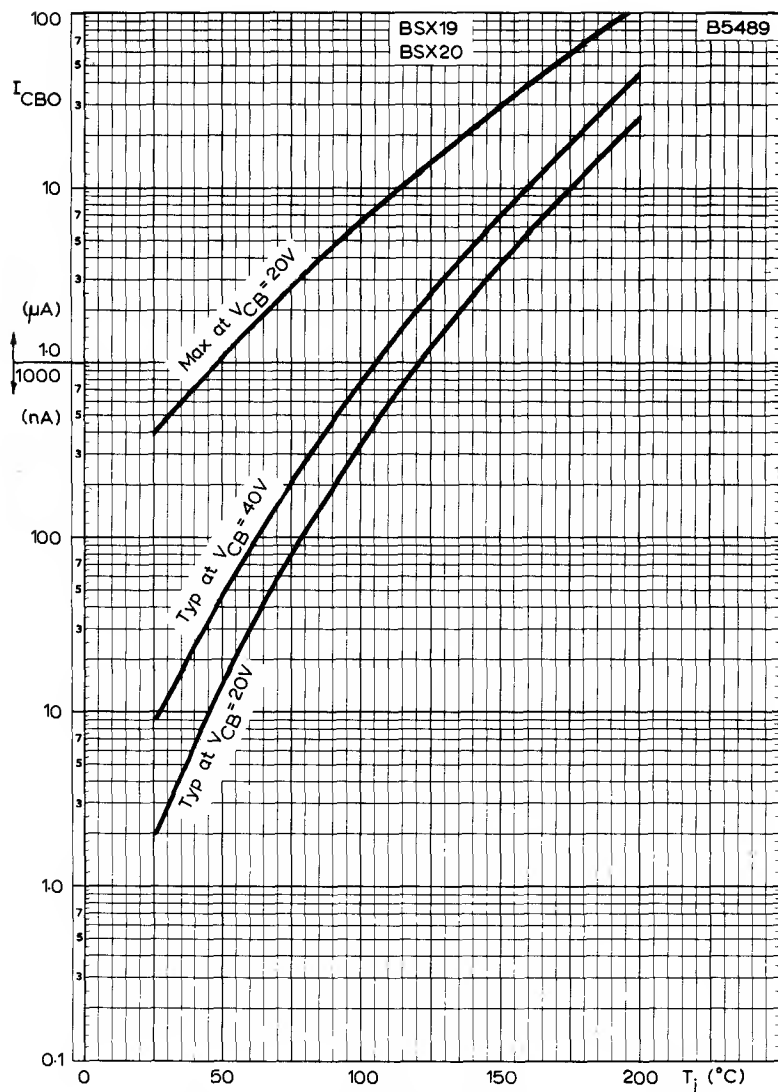
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED
AGAINST COLLECTOR CURRENT



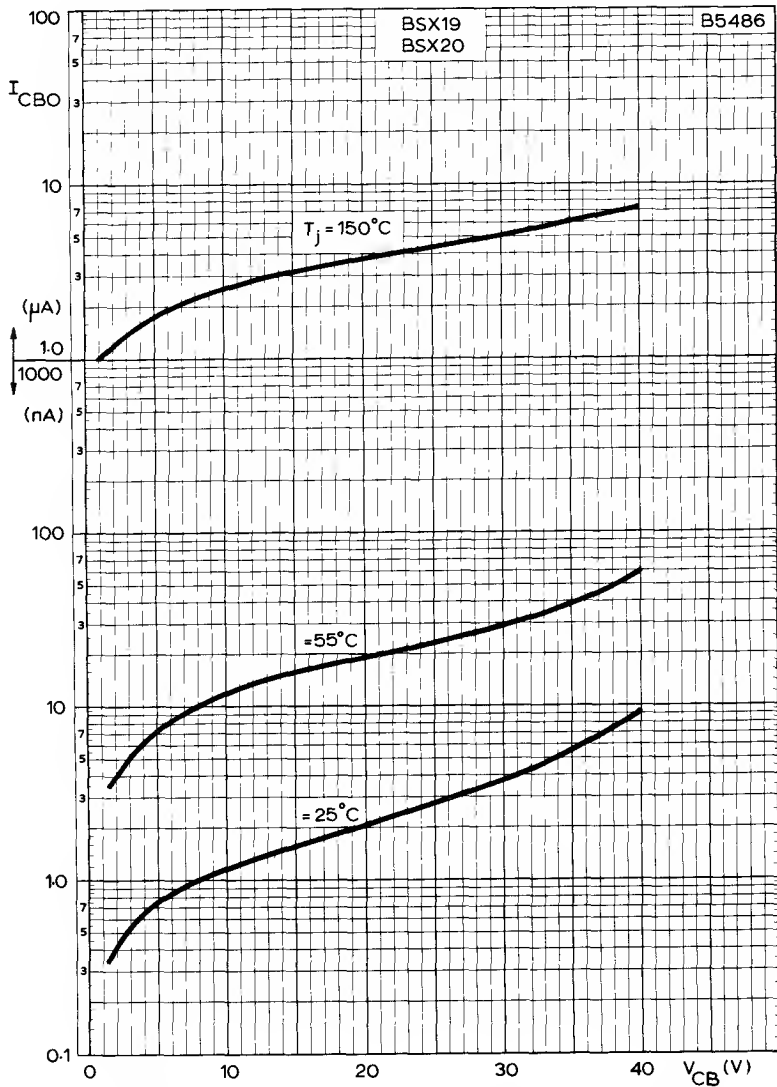
**TYPICAL COLLECTOR-EMITTER SATURATION AND BASE-EMITTER
SATURATION VOLTAGES PLOTTED AGAINST JUNCTION TEMPERATURE.**



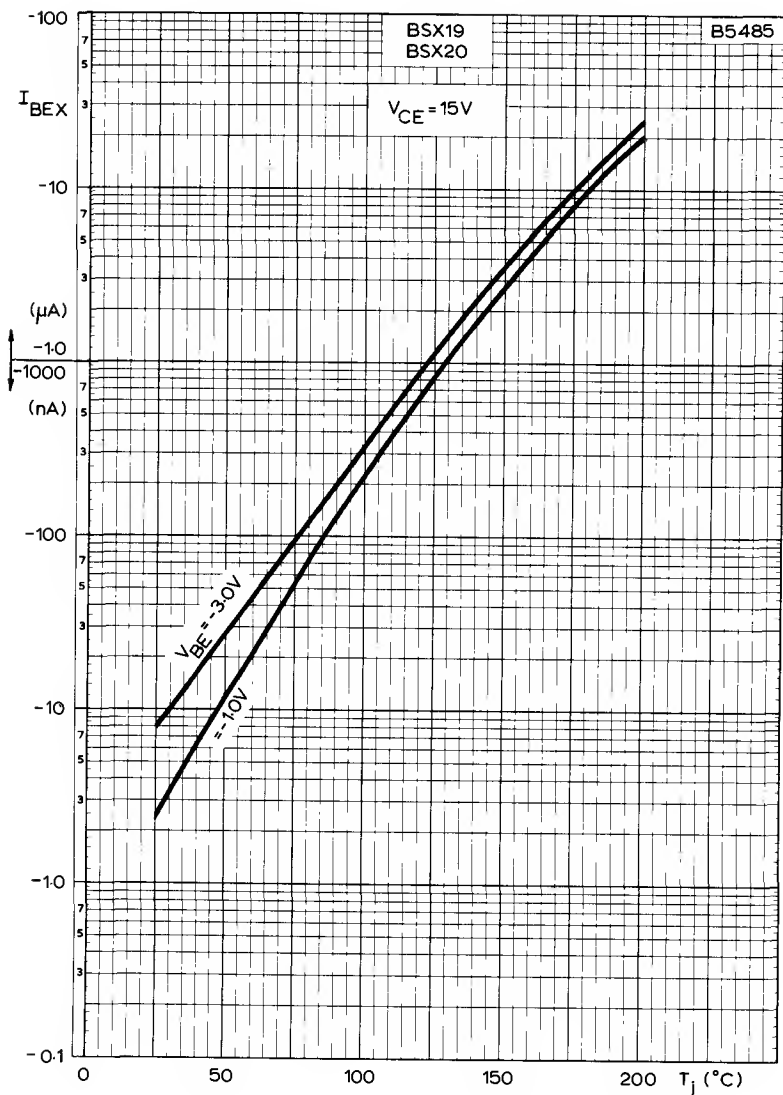
TYPICAL BASE-EMITTER VOLTAGE PLOTTED AGAINST JUNCTION TEMPERATURE



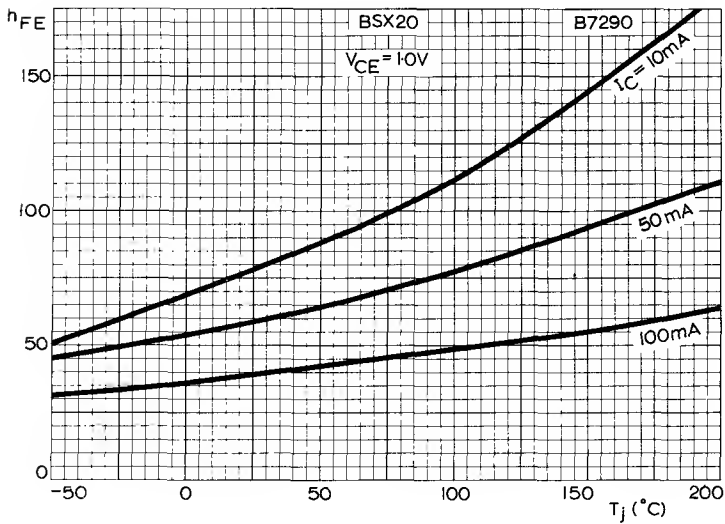
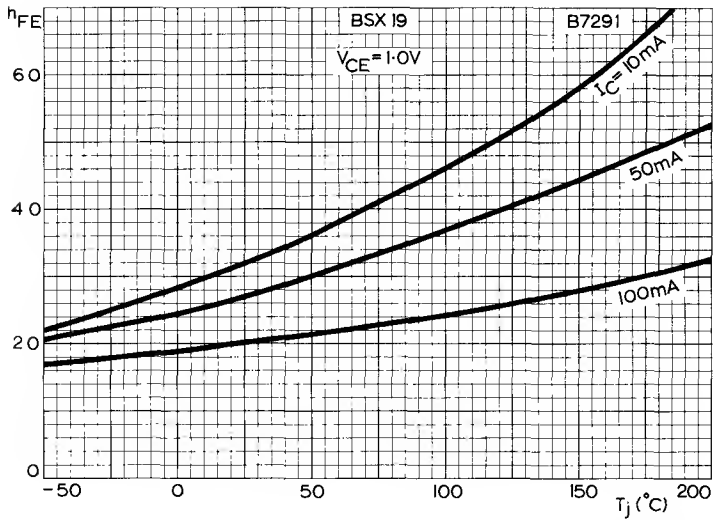
COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST JUNCTION
TEMPERATURE



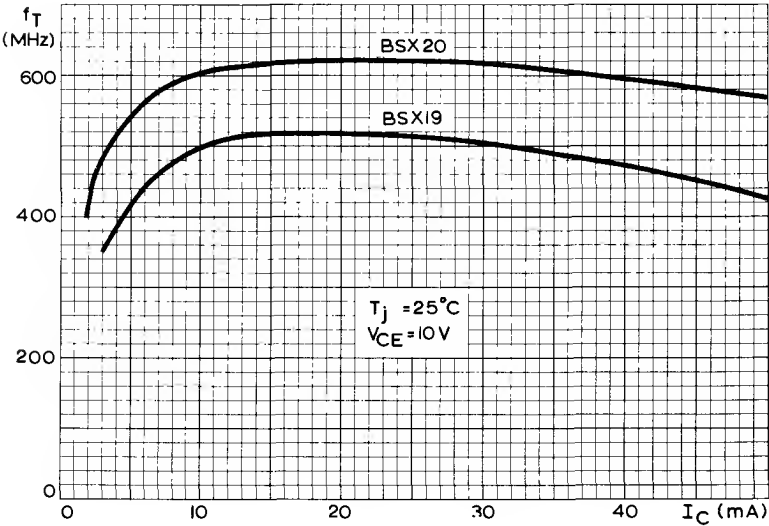
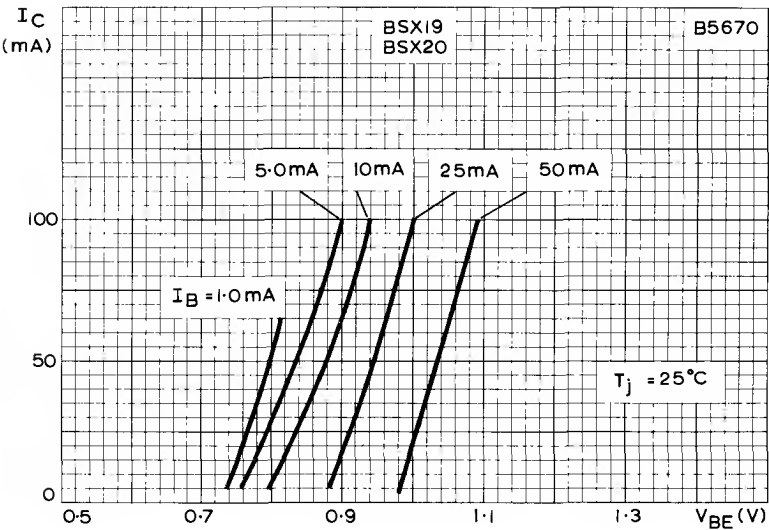
TYPICAL COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST
COLLECTOR-BASE VOLTAGE



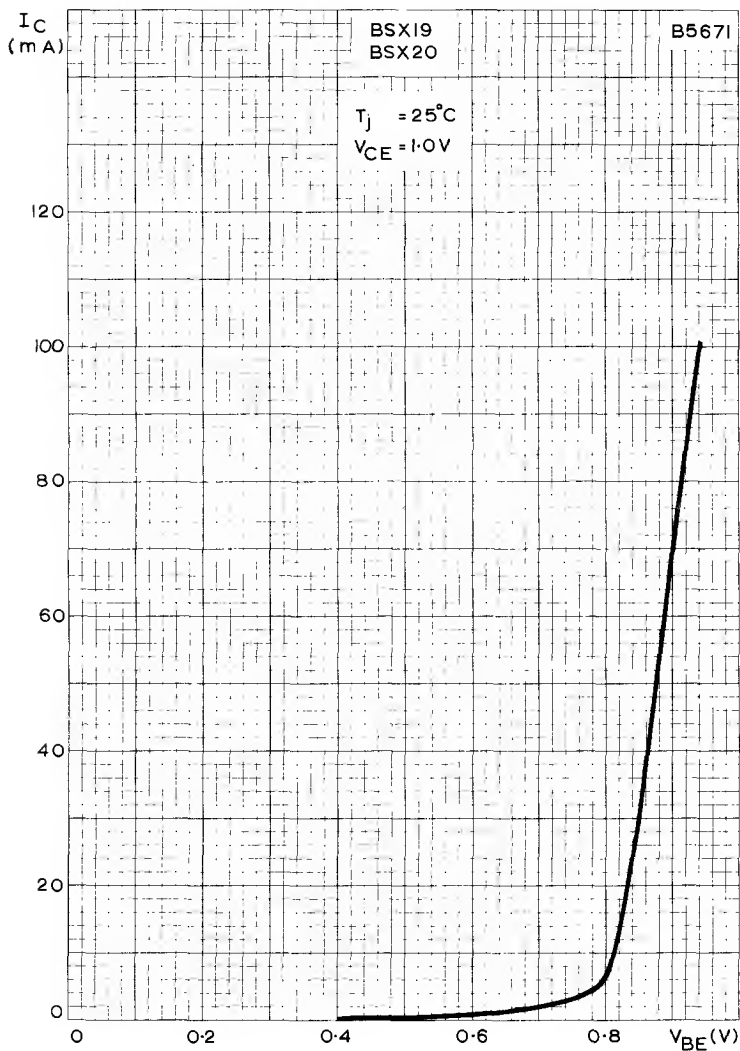
TYPICAL BASE-EMITTER CUT-OFF CURRENT PLOTTED AGAINST
JUNCTION TEMPERATURE



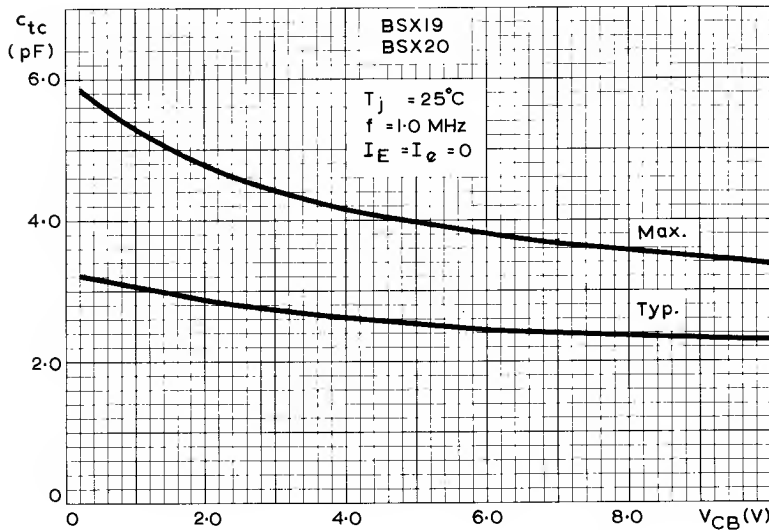
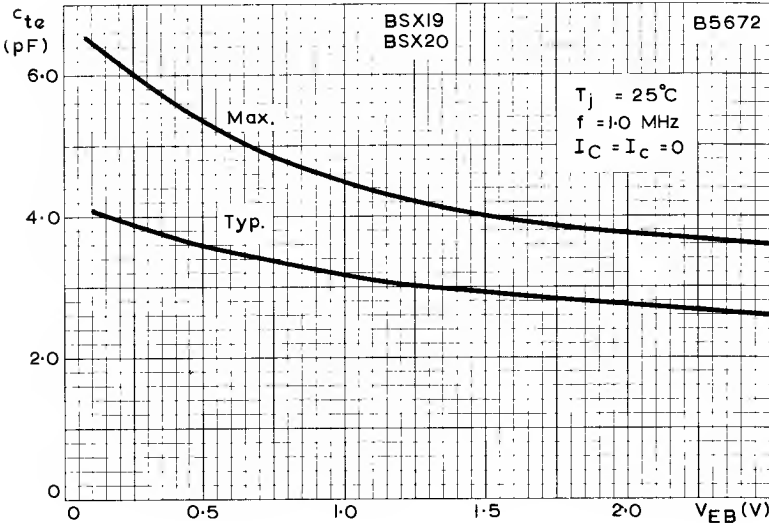
TYPICAL VARIATION OF STATIC FORWARD CURRENT
TRANSFER RATIO WITH JUNCTION TEMPERATURE



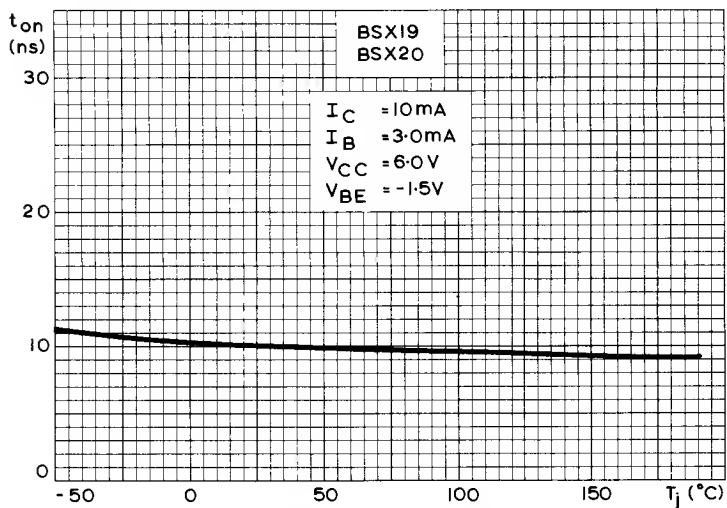
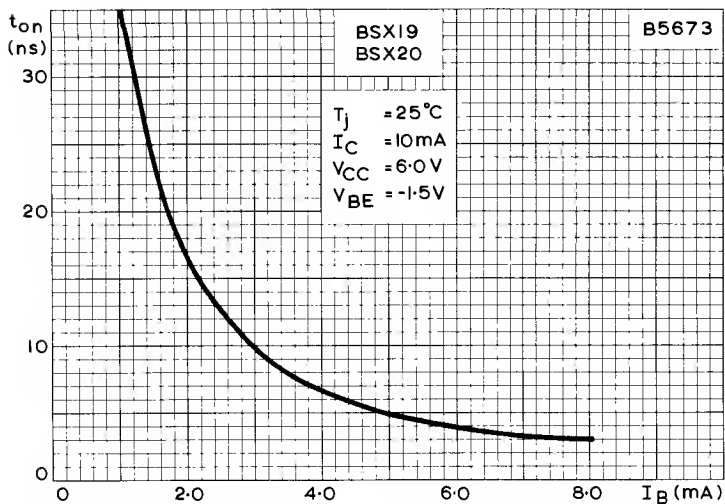
TYPICAL COLLECTOR CURRENT PLOTTED AGAINST BASE -
EMITTER VOLTAGE
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR
CURRENT



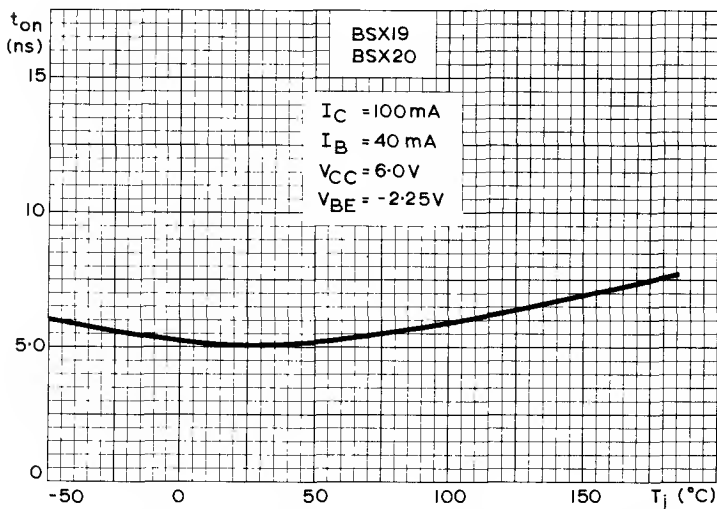
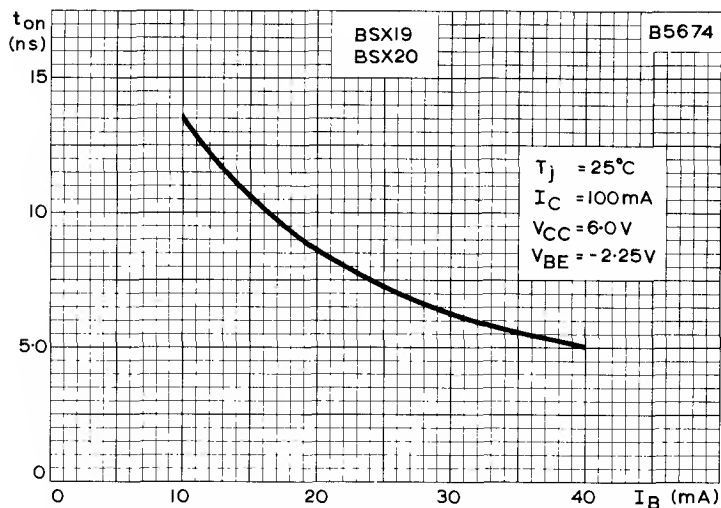
TYPICAL COLLECTOR CURRENT PLOTTED AGAINST BASE-EMITTER
VOLTAGE



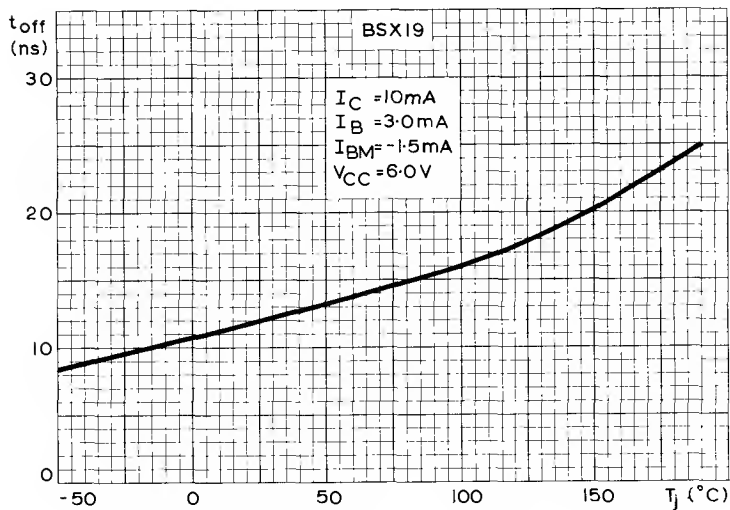
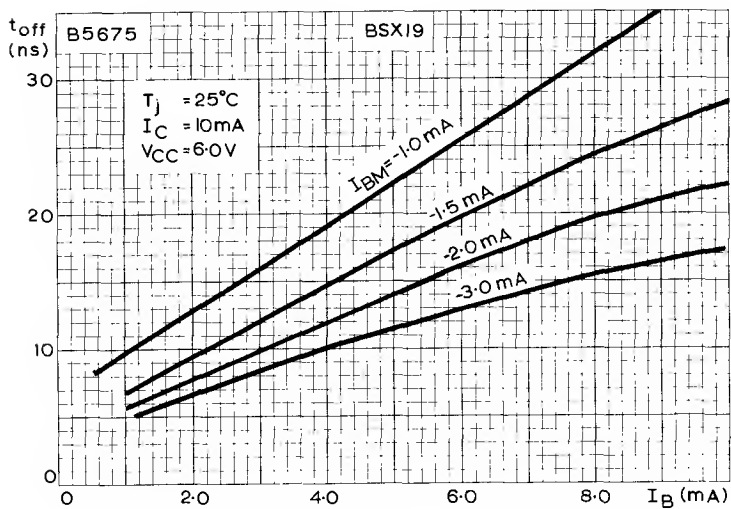
EMITTER CAPACITANCE PLOTTED AGAINST EMITTER-BASE
VOLTAGE
COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE
VOLTAGE



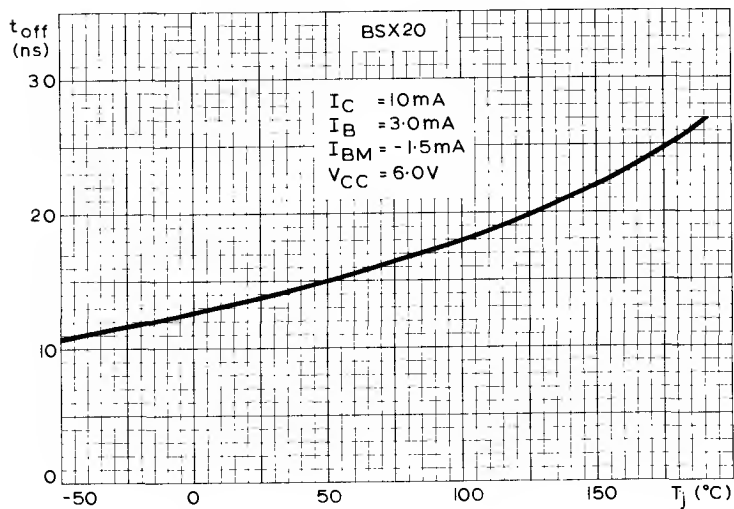
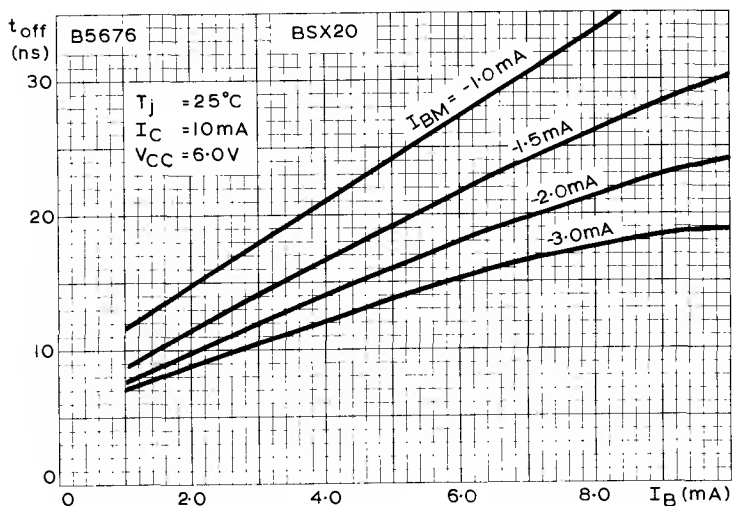
TYPICAL TURN-ON TIME PLOTTED AGAINST BASE CURRENT
 TYPICAL TURN-ON TIME PLOTTED AGAINST JUNCTION TEMPERATURE



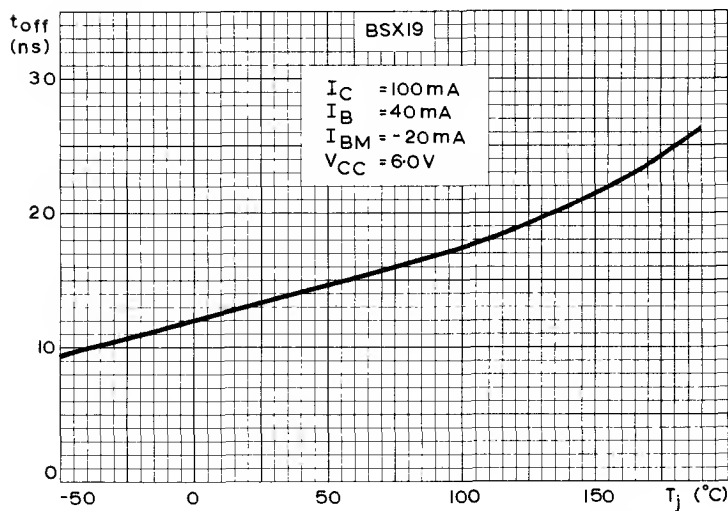
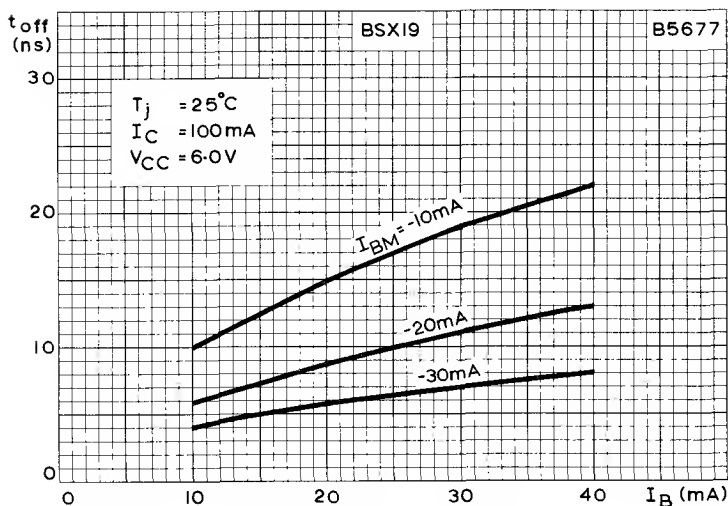
TYPICAL TURN-ON TIME PLOTTED AGAINST BASE CURRENT
 TYPICAL TURN-ON TIME PLOTTED AGAINST JUNCTION TEMPERATURE



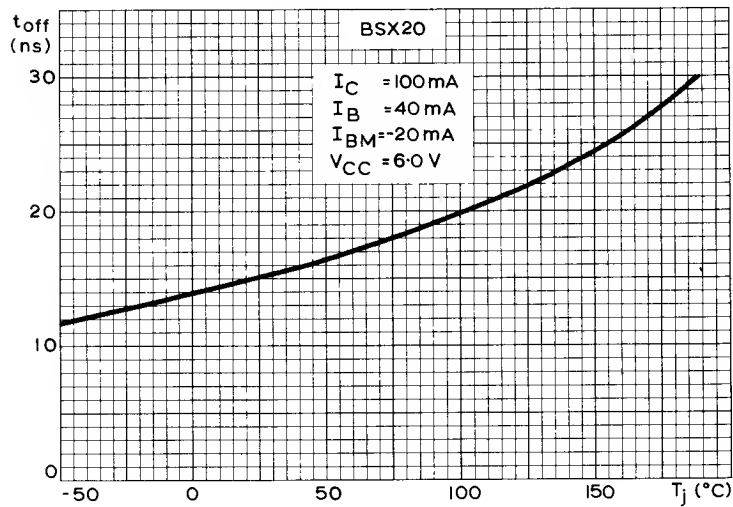
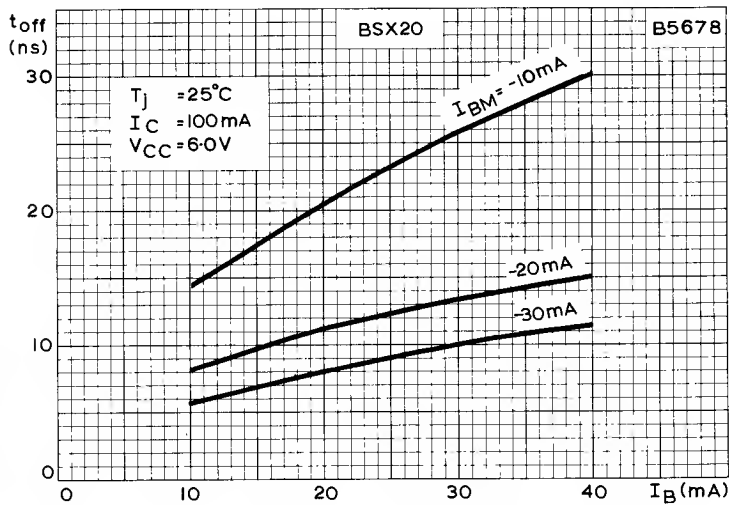
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
 TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



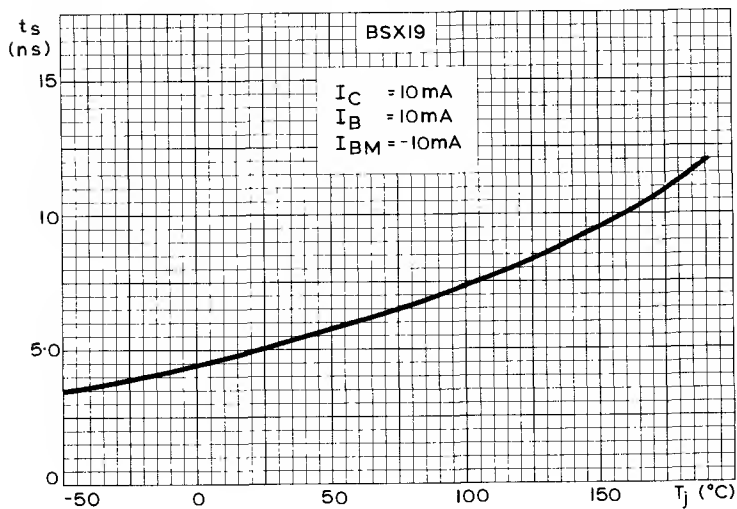
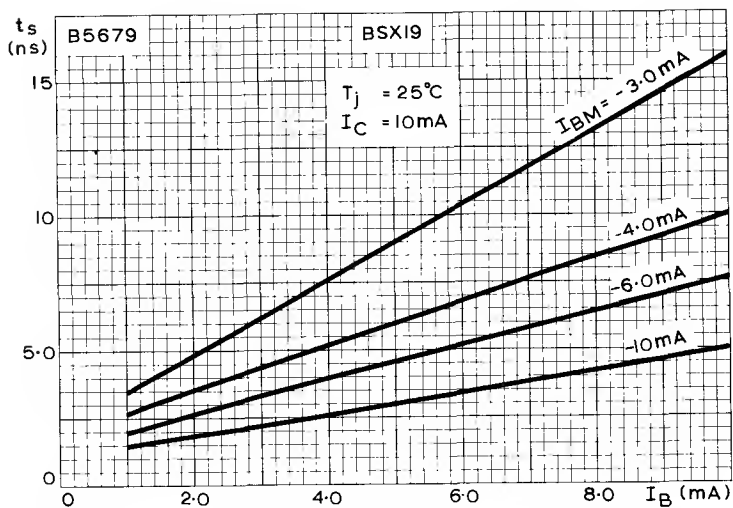
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
 TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



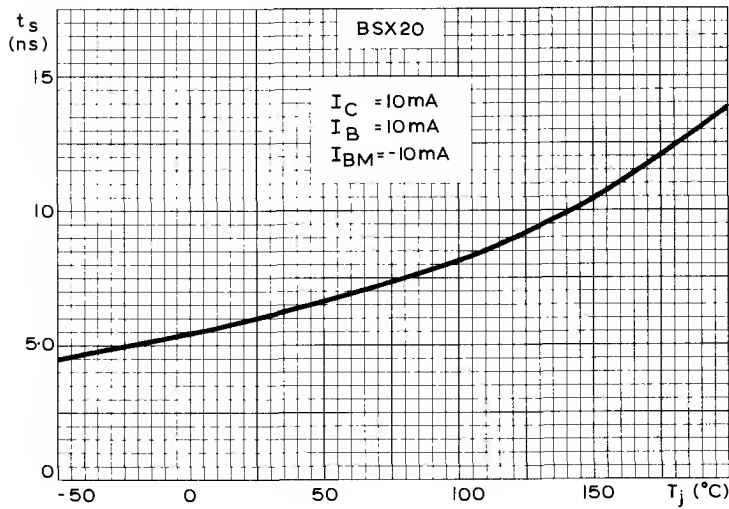
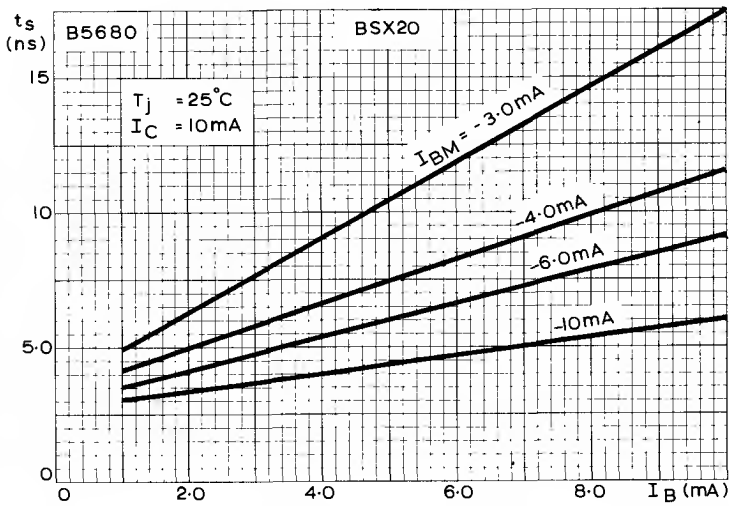
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
 TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL STORAGE TIME PLOTTED AGAINST BASE CURRENT
 TYPICAL STORAGE TIME PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL STORAGE TIME PLOTTED AGAINST BASE CURRENT
TYPICAL STORAGE TIME PLOTTED AGAINST JUNCTION TEMPERATURE

N-P-N SILICON PLANAR TRANSISTOR

BSX21

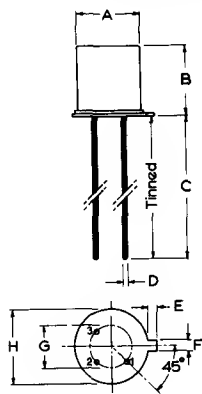
N-P-N silicon planar transistor for use in general industrial applications and as a driver with numerical indicator tubes. TO-18 construction with collector connected to the envelope.

QUICK REFERENCE DATA

V_{CB} max. ($I_E = 0$)	+120	V
V_{CEO} max.	+80	V
I_{CM} max.	50	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)	300	mW
T_j max.	175	$^\circ\text{C}$
h_{FE} min. ($I_C = 4.0\text{mA}$, $V_{CE} = +3.0\text{V}$)	20	
f_T min. ($I_C = 4.0\text{mA}$, $V_{CE} = +10\text{V}$)	60	MHz

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18



Millimetres

	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	-	0.48
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

- Connections
1. Emitter
 2. Base
 3. Collector connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\dagger V_{CBO}$ max. ($I_E = 0$)	+120	V
$\dagger V_{CEO}$ max. ($I_B = 0$)	+80	V
V_{EBO} max. ($I_C = 0$)	+5.0	V
$\ddagger I_{CM}$ max.	50	mA
$* I_{C(AV)}$ max.	50	mA
I_{EM} max.	50	mA
$* I_{E(AV)}$ max.	50	mA
P_{tot} max. ($T_{amb} = 25^\circ C$)	300	mW

Temperature

T_{stg} min.	-65	$^\circ C$
T_{stg} max.	175	$^\circ C$
T_j max.	175	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	0.5	degC/mW
$R_{th(j-case)}$	0.15	degC/mW

*Averaged over any 20ms period.

\dagger The BSX21 may be operated in the breakdown region up to $V_{CE} = +160V$, provided that $P_{tot} \leq 100mW$ at $T_{amb} \leq 85^\circ C$.

\ddagger The transistor can withstand a capacitive load of 500pF, with V_{CE} max. = 150V during switch-on.

N-P-N SILICON PLANAR TRANSISTOR

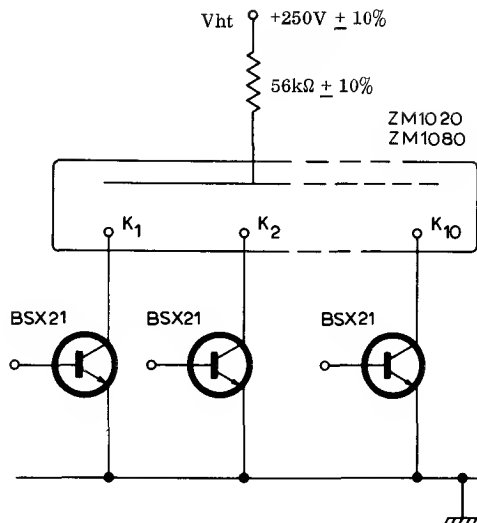
BSX21

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{\text{CB}} = +50\text{V}, I_{\text{E}} = 0$	-	0.5	-	μA
	$V_{\text{CB}} = +120\text{V}, I_{\text{E}} = 0$	-	-	40	μA
I_{EBO}	Emitter cut-off current				
	$V_{\text{EB}} = +3.0\text{V}, I_{\text{C}} = 0$	-	0.1	-	μA
$V_{\text{CE(sat)}}$	Collector-emitter saturation voltage				
	$I_{\text{C}} = 1.0\text{mA}, I_{\text{B}} = 100\mu\text{A}$	-	+250	-	mV
	$I_{\text{C}} = 10\text{mA}, I_{\text{B}} = 1.0\text{mA}$	-	+1.8	-	V
$V_{\text{BE(sat)}}$	Base-emitter saturation voltage				
	$I_{\text{C}} = 1.0\text{mA}, I_{\text{B}} = 100\mu\text{A}$	-	+670	-	mV
	$I_{\text{C}} = 10\text{mA}, I_{\text{B}} = 1.0\text{mA}$	-	+900	-	mV
$V_{\text{CE(sust)}}$	Collector-emitter sustaining voltage				
	$I_{\text{C}} = 4.0\text{mA}, I_{\text{B}} = 0$	+80	-	-	V
V_{BE}	Base-emitter voltage				
	$I_{\text{C}} = 4.0\text{mA}, V_{\text{CE}} = +3.0\text{V}$	-	+700	+900	mV
h_{FE}	Static forward current transfer ratio				
	$I_{\text{C}} = 1.0\text{mA}, V_{\text{CE}} = +3.0\text{V}$	-	25	-	
	$I_{\text{C}} = 4.0\text{mA}, V_{\text{CE}} = +3.0\text{V}$	20	40	-	
	$I_{\text{C}} = 10\text{mA}, V_{\text{CE}} = +3.0\text{V}$	-	32	-	
	$I_{\text{C}} = 20\text{mA}, V_{\text{CE}} = +3.0\text{V}$	-	7	-	
C_{Tc}	Collector capacitance				
	$I_{\text{E}} = I_{\text{e}} = 0, V_{\text{CB}} = +10\text{V},$ $f = 1.0\text{MHz}$	-	3.6	-	pF
C_{Te}	Emitter capacitance				
	$I_{\text{C}} = I_{\text{c}} = 0, V_{\text{EB}} = +1.0\text{V}$ $f = 1.0\text{MHz}$	-	8.5	-	pF
f_{T}	Transition frequency				
	$I_{\text{C}} = 4.0\text{mA}, V_{\text{CE}} = +10\text{V}$	60	120	-	MHz

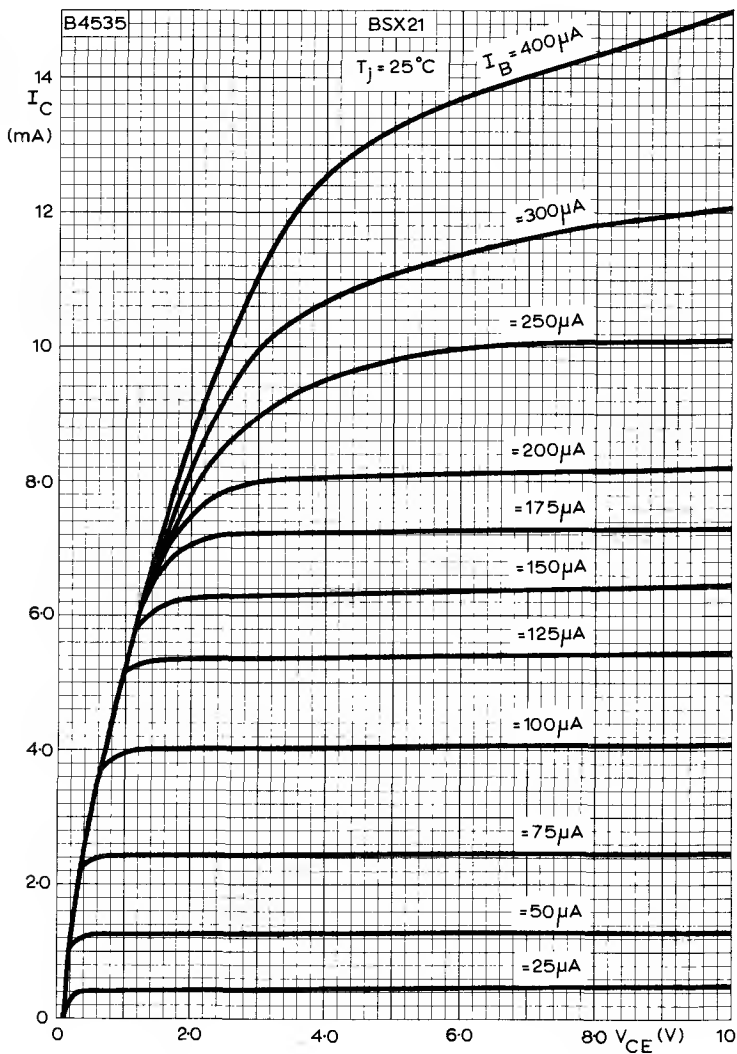
Mullard

TYPICAL CIRCUIT

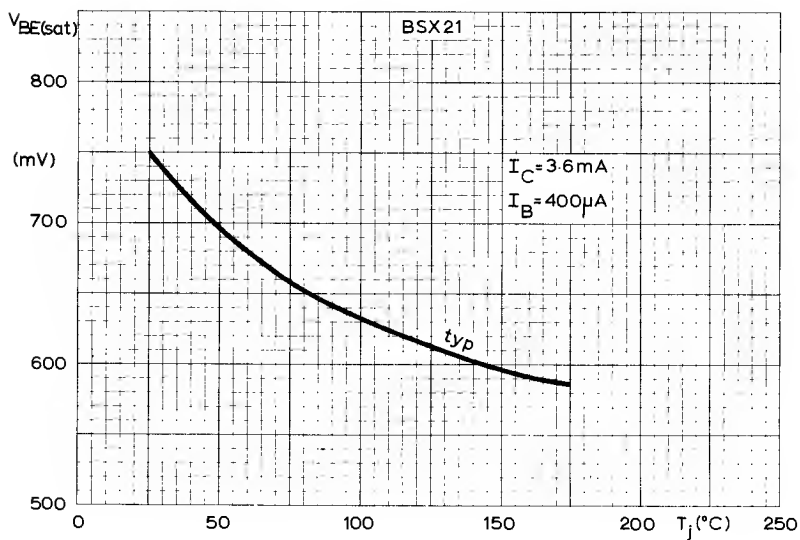
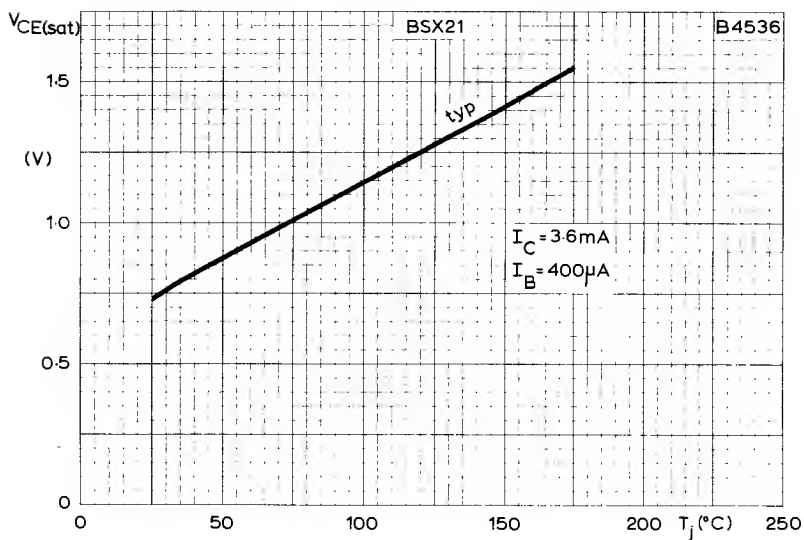


SOLDERING AND WIRING RECOMMENDATIONS

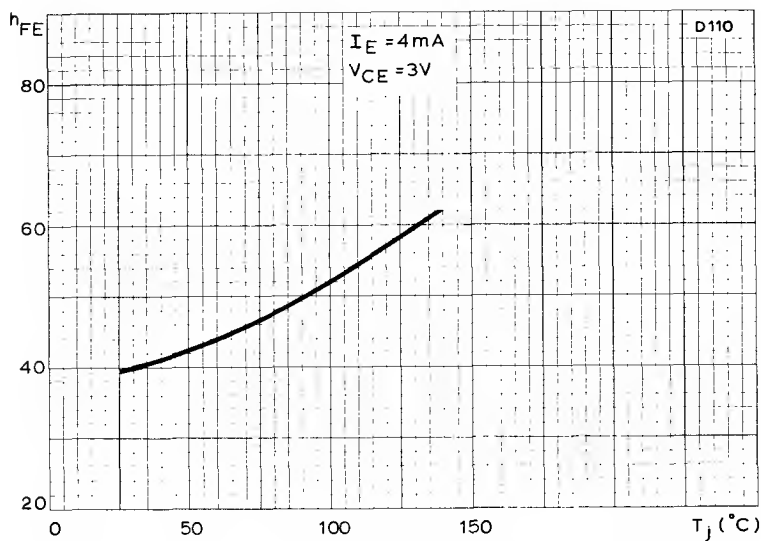
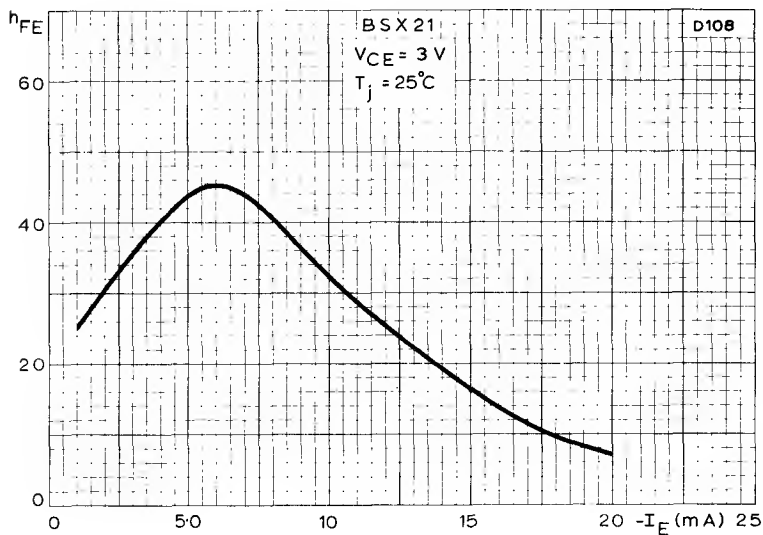
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.



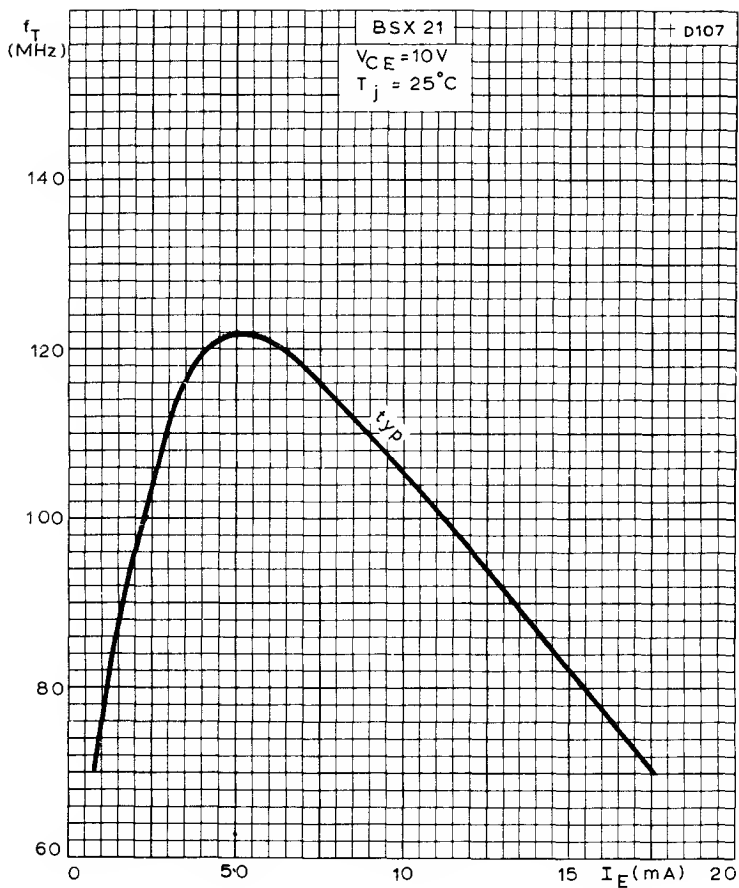
TYPICAL OUTPUT CHARACTERISTIC



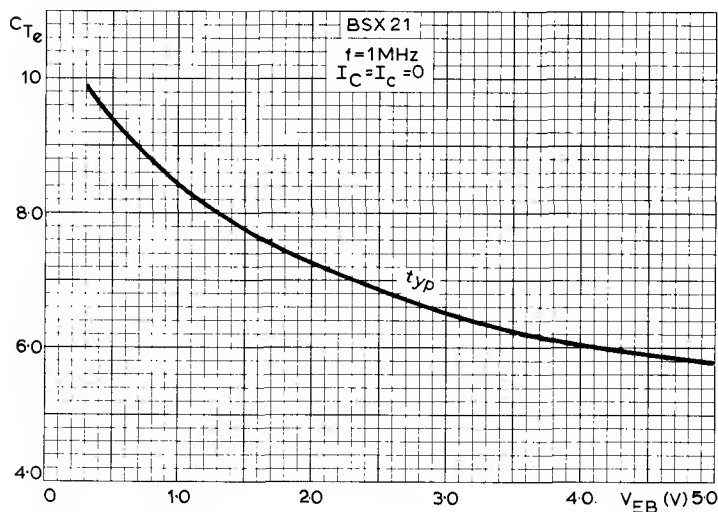
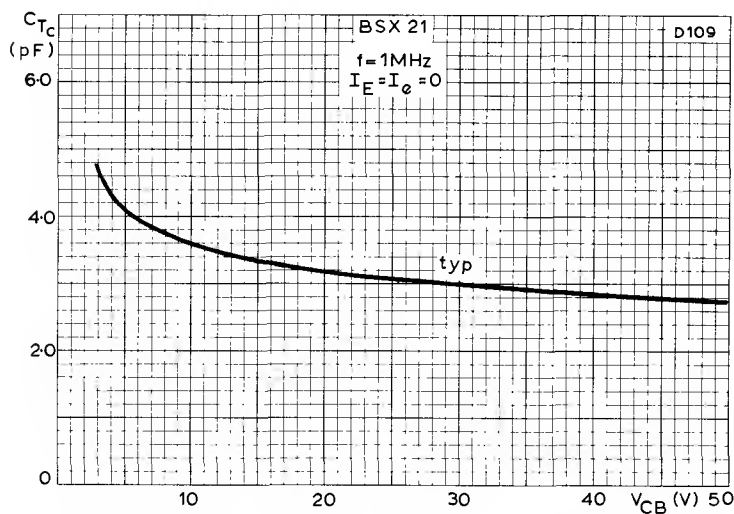
TYPICAL VARIATION OF COLLECTOR-EMITTER AND BASE-EMITTER SATURATION VOLTAGES WITH JUNCTION TEMPERATURE



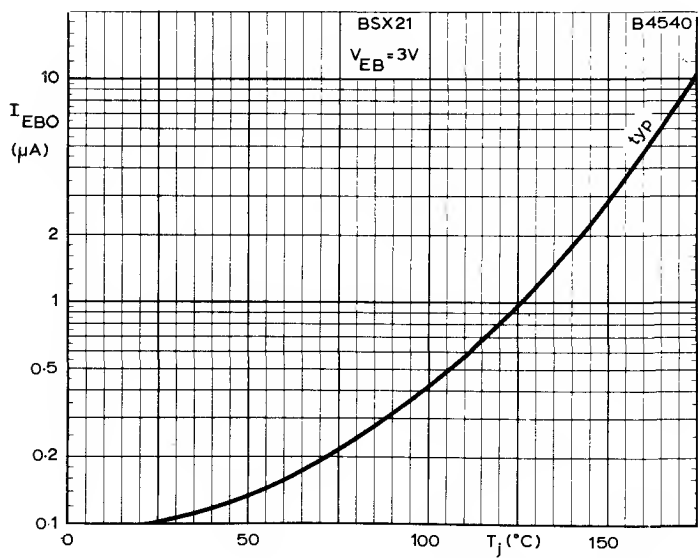
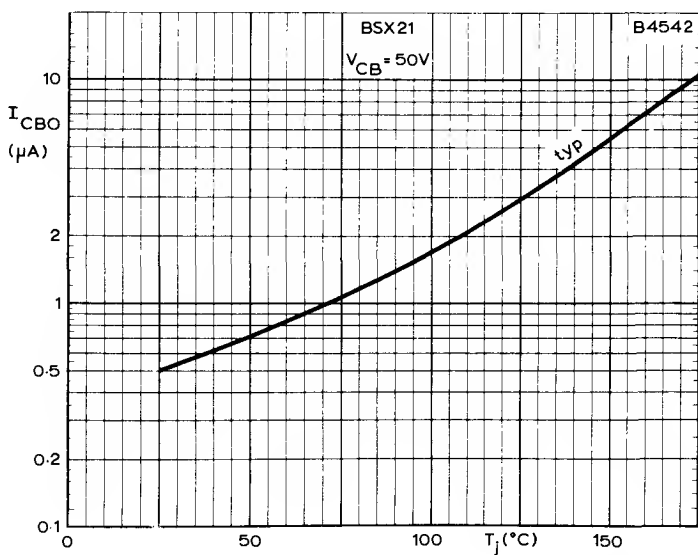
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH EMITTER CURRENT AND JUNCTION TEMPERATURE



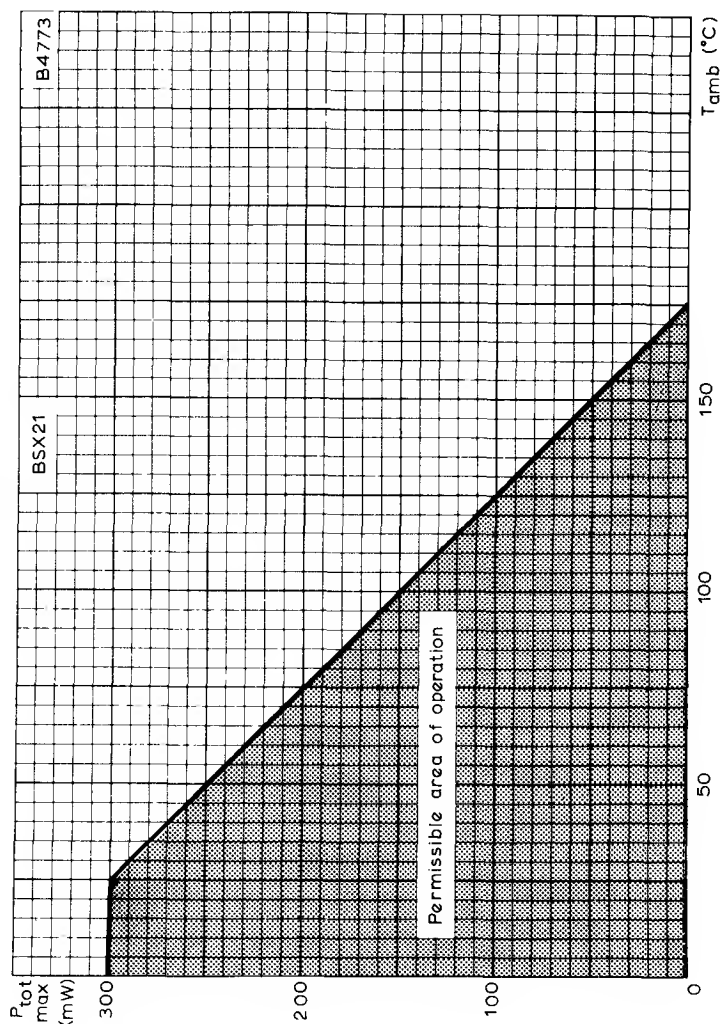
TRANSITION FREQUENCY PLOTTED AGAINST EMITTER CURRENT



COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE
VOLTAGE AND EMITTER CAPACITANCE PLOTTED AGAINST
EMITTER-BASE VOLTAGE



TYPICAL VARIATION OF COLLECTOR-BASE AND EMITTER-BASE CUT-OFF CURRENTS WITH JUNCTION TEMPERATURE



MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

BSX59
BSX60
BSX61

Silicon planar epitaxial n-p-n transistors intended for use in very high speed core driving applications

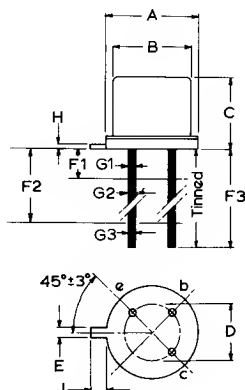
QUICK REFERENCE DATA

	BSX59	BSX60	BSX61	
V_{CBO} max.	70	70	70	V
V_{CEO} max.	45	30	45	V
I_C max.	1.0	1.0	1.0	A
P_{tot} max. ($T_{amb} = 25^{\circ}C$)	800	800	800	mW
T_j max.	200	200	200	$^{\circ}C$
h_{FE} ($I_C = 500mA$, $V_{CE} = 1.0V$)	25min.	30-90	25min.	
$V_{CE(sat)}$ max. ($I_C = 500mA$, $I_B = 50mA$)	0.5	0.5	0.7	V
t_{on} max. ($I_C = 500mA$, $I_{Bon} = 50mA$, $-V_{BEoff} = 2.0V$)	35	40	50	ns
t_{off} max. ($I_C = 500mA$, $I_{Bon} = -I_{Boff} = 50mA$)	60	70	100	ns

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



Millimetres

	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.2	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

The collector is connected
to the envelope

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.		70	V
V_{CEO} max.	BSX59	45	V
	BSX60	30	V
	BSX61	45	V
V_{EBO} max.		5.0	V
I_C max.		1.0	A
I_B max.		0.2	A
P_{tot} max. ($T_{amb} = 25^{\circ}\text{C}$)		800	mW

Temperature

T_{stg} min.	-65	$^{\circ}\text{C}$
T_{stg} max.	200	$^{\circ}\text{C}$
T_j max.	200	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Θ_{j-amb} (in free air)	0.22	degC/mW
Θ_{j-mb}	0.035	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

			Min.	Typ.	Max.	
I _{CBO}	Collector cut-off current					
	V _{CB} =40V, I _E =0		-	50	500	nA
	V _{CB} =40V, I _E =0, T _j =150 ^o C		-	100	300	μA
I _{EBO}	Emitter cut-off current					
	V _{EB} =4.0V, I _C =0	BSX59,60	-	50	300	nA
		BSX61	-	50	500	nA
	V _{EB} =4.0V, I _C =0, T _j =150 ^o C		-	5.0	50	μA
I _{CEX}	Currents with reverse biased emitter junction					
	V _{CE} =40V, -V _{BE} =4.0V	BSX59,60	-	50	500	nA
		BSX61	-	50	1000	nA
	V _{CE} =40V, -V _{BE} =4.0V, T _j =150 ^o C					
		BSX59,60	-	100	300	μA
		BSX61	-	100	500	μA
-I _{BEX}	V _{CE} =40V, -V _{BE} =4.0V	BSX59,60	-	50	500	nA
		BSX61	-	50	1000	nA
	V _{CE} =40V, -V _{BE} =4.0V, T _j =150 ^o C					
		BSX59,60	-	100	300	μA
		BSX61	-	100	500	μA

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SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

BSX59
BSX60
BSX61

ELECTRICAL CHARACTERISTICS (cont'd)

			Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage					
	$I_C = 10\mu A, I_E = 0$	BSX59	70	120	-	V
		BSX60	70	110	-	V
		BSX61	70	100	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage					
	$I_C = 100\mu A, V_{BE} = 0$	BSX59	60	110	-	V
		BSX60, 61	60	100	-	V
$V_{(BR)CEO}$	$I_C = 10mA, I_B = 0$	BSX59, 61	45	55	-	V
		BSX60	30	50	-	V
$V_{(BR)CEX}$	$-V_{BB} = 3.5V, R_B = 70\Omega$	BSX59, 61				See note 1
$V_{CE(sat)}$	Collector-emitter saturation voltage					
	$I_C = 150mA, I_B = 15mA$	BSX59	-	0.24	0.3	V
		BSX60	-	0.21	0.3	V
		BSX61	-	0.18	0.5	V
	$I_C = 500mA, I_B = 50mA$	BSX59	-	0.44	0.5	V
		BSX60	-	0.42	0.5	V
		BSX61	-	0.4	0.7	V
	$I_C = 1.0A, I_B = 100mA$	BSX59	-	0.58	1.0	V
		BSX60	-	0.56	1.0	V
		BSX61	-	0.56	1.3	V
$V_{BE(sat)}$	Base-emitter saturation voltage					
	$I_C = 150mA, I_B = 15mA$		-	0.8	1.0	V
	$I_C = 500mA, I_B = 50mA$	BSX59	0.85	1.0	1.2	V
		BSX60	0.7	1.0	1.3	V
		BSX61	0.77	1.0	1.3	V
	$I_C = 1.0A, I_B = 100mA$		-	1.2	1.8	V
h_{FE}	Static forward current transfer ratio					
	$I_C = 150mA, V_{CE} = 1.0V$	BSX59	30	70	-	
		BSX60	30	100	-	
		BSX61	30	110	-	

NOTE

1. No breakdown may occur when the transistor is switched from $I_C = 1.0A$ to $V_{CE} = 60V$ with $-I_{Boff} = 50mA$.

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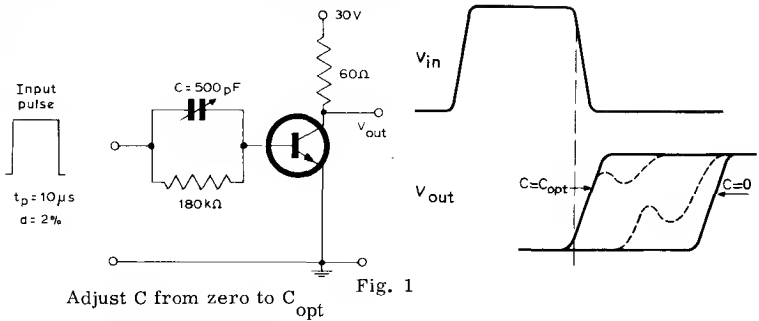
ELECTRICAL CHARACTERISTICS (cont'd)

			Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio					
	$I_C = 500\text{mA}$, $V_{CE} = 1.0\text{V}$	BSX59, 61	25	-	-	
		BSX60	30	-	90	
	$I_C = 1.0\text{A}$, $V_{CE} = 5.0\text{V}$	BSX59	20	40	-	
		BSX60	25	50	-	
		BSX61	20	55	-	
h_{fe}	Small signal forward current transfer ratio					
	$I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 100\text{MHz}$		2.5	4.75	-	
C_{ibo}	Input capacitance $-V_{BE} = 0.5\text{V}$, $I_C = 0$, $f = 1.0\text{MHz}$		-	36	50	pF
C_{obo}	Output capacitance $V_{CB} = 10\text{V}$, $I_E = 0$, $f = 1.0\text{MHz}$		-	5.75	10	pF
Q_s	Recovered charge (see fig.1)					
	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$, $V_{CC} = 30\text{V}$		-	3.8	5.0	nC
t_{on}	Turn-on time (see fig.2)					
	$I_C = 500\text{mA}$, $I_{Bon} = 50\text{mA}$, $-V_{BEoff} = 2.0\text{V}$, $V_{CC} = 50\text{V}$		-	17	35	ns
	$V_{CC} = 30\text{V}$		-	17	40	ns
	$V_{CC} = 50\text{V}$		-	18	50	ns
t_{off}	Turn-off time (see fig.2)					
	$I_C = 500\text{mA}$, $I_{Bon} = -I_{Boff} = 50\text{mA}$, $V_{CC} = 50\text{V}$		-	45	60	ns
	$V_{CC} = 30\text{V}$		-	58	70	ns
	$V_{CC} = 50\text{V}$		-	70	100	ns

SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

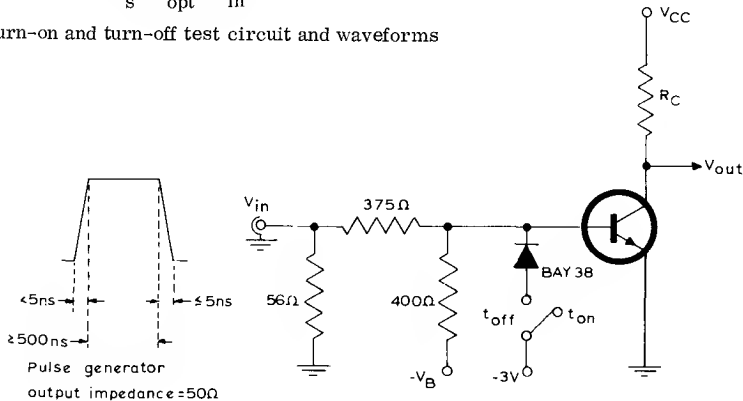
BSX59
BSX60
BSX61

Recovered charge test circuit and waveforms

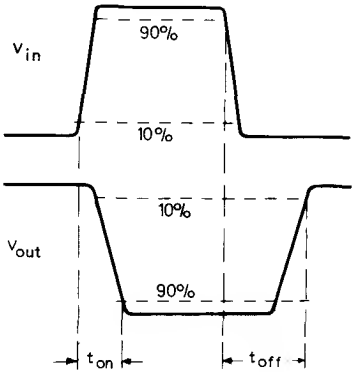


$$Q_s = C_{opt} \times V_{in}$$

Turn-on and turn-off test circuit and waveforms

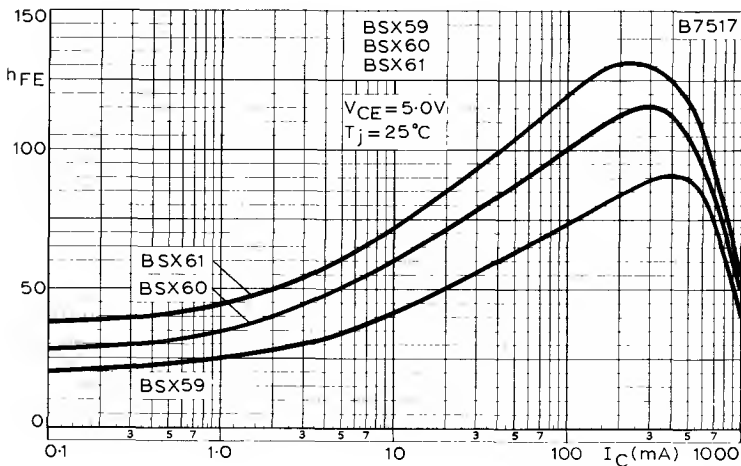
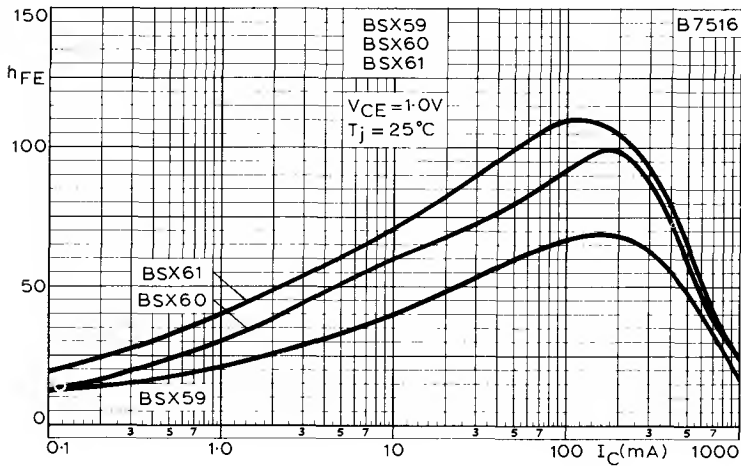


Measurement	V_{CC}	BSX59	BSX60	V
		BSX61		
R_C	50	30		V
	100	60		Ω
t_{on}	$-V_B$	4.0		V
	V_{in}	24.75		V
t_{off}	$-V_B$	16.7		V
	V_{in}	37.5		V



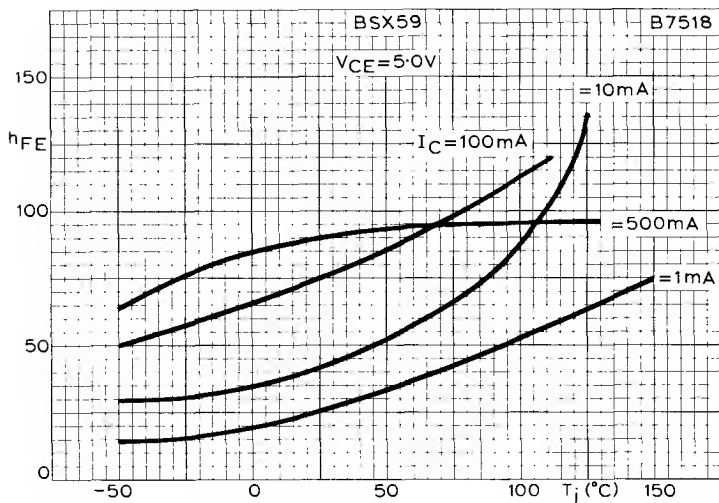
SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

BSX59
BSX60
BSX61

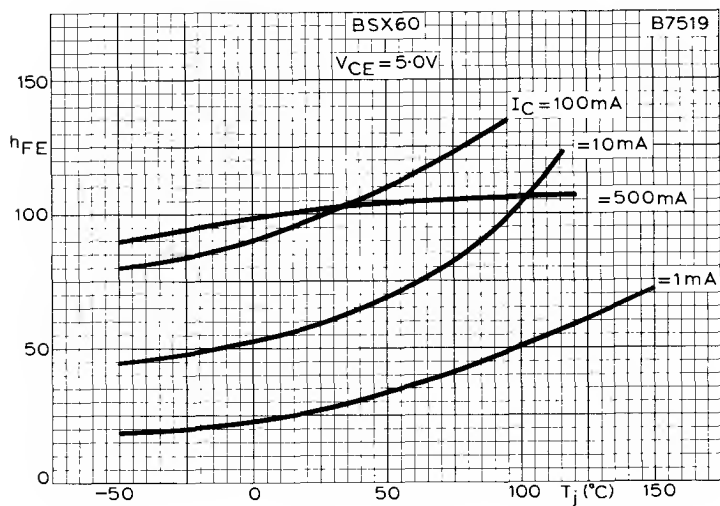


TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH COLLECTOR CURRENT AT $V_{CE} = 1.0$ and $5.0V$ RESPECTIVELY

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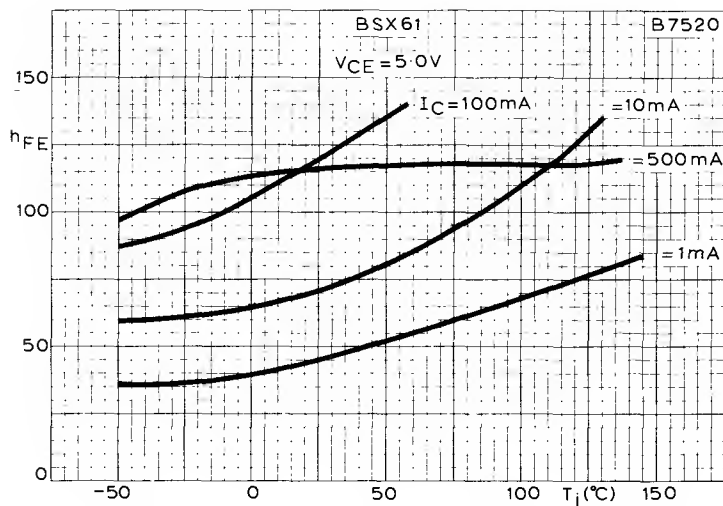
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH JUNCTION TEMPERATURE ; BSX59



TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH JUNCTION TEMPERATURE ; BSX60

SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

**BSX59
BSX60
BSX61**

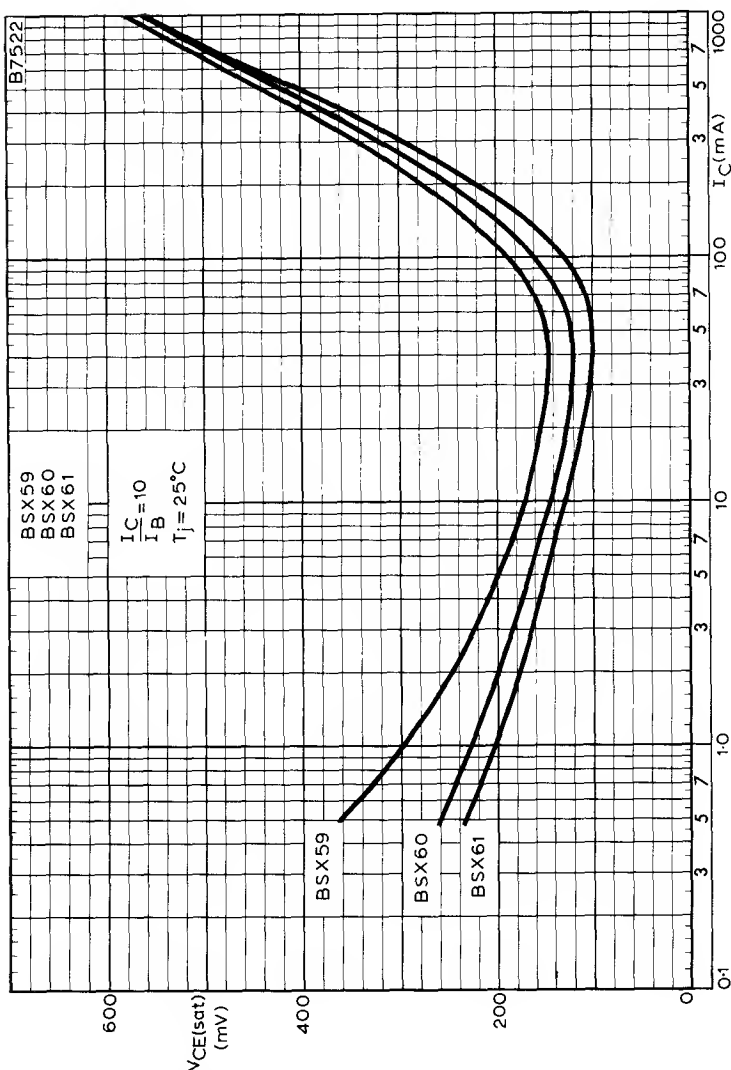


TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO
WITH JUNCTION TEMPERATURE; BSX61



TYPICAL VARIATION OF SMALL SIGNAL FORWARD CURRENT
TRANSFER RATIO WITH COLLECTOR CURRENT

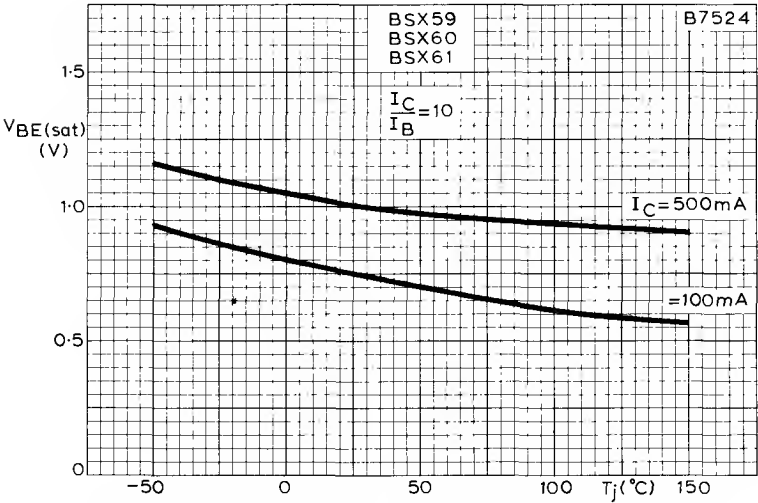
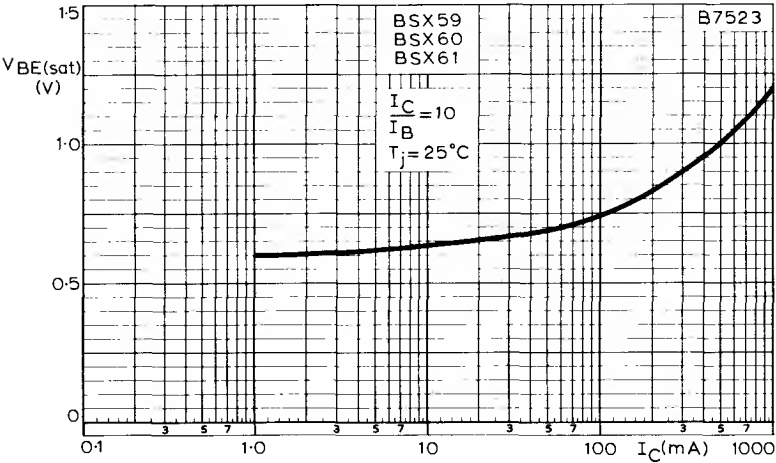
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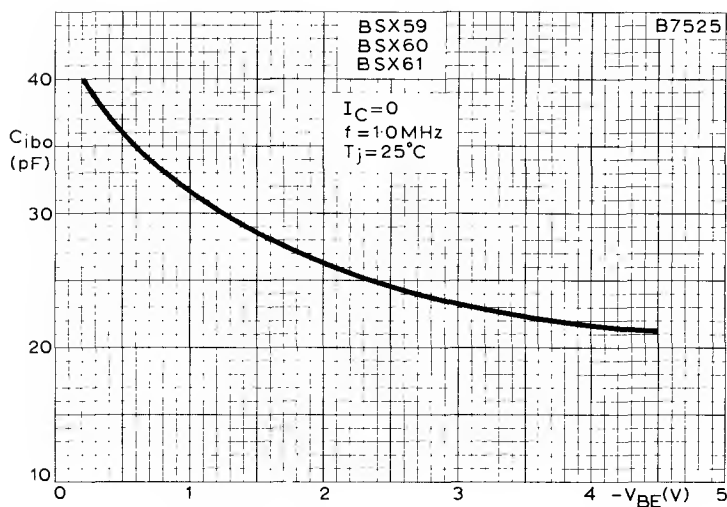
TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION
VOLTAGE WITH COLLECTOR CURRENT

SILICON PLANAR EPITAXIAL
N-P-N TRANSISTORS

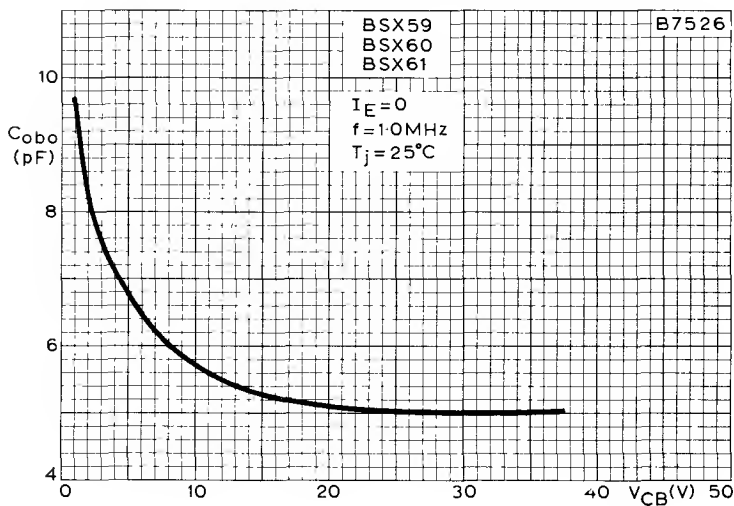
BSX59
BSX60
BSX61



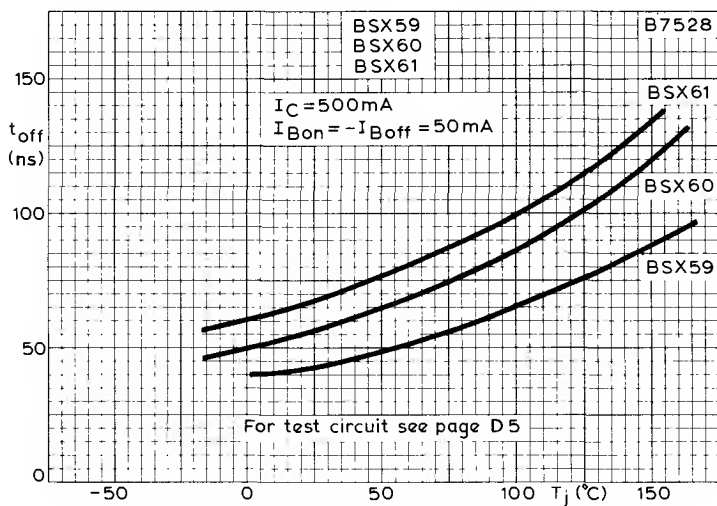
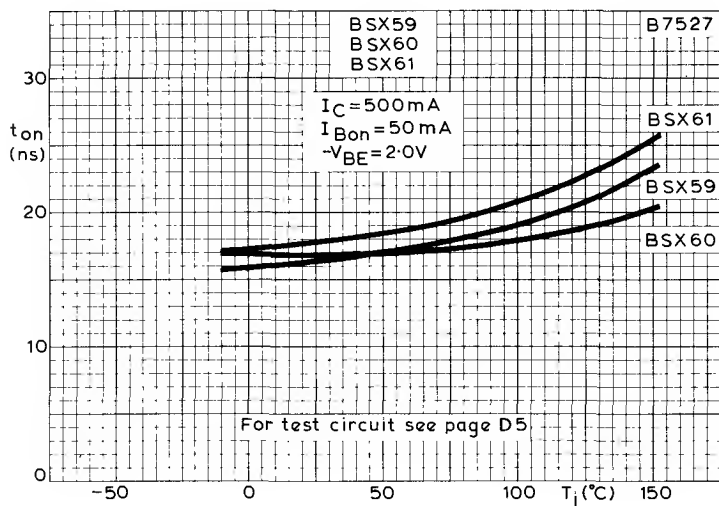
TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE
WITH COLLECTOR CURRENT AND JUNCTION TEMPERATURE
RESPECTIVELY



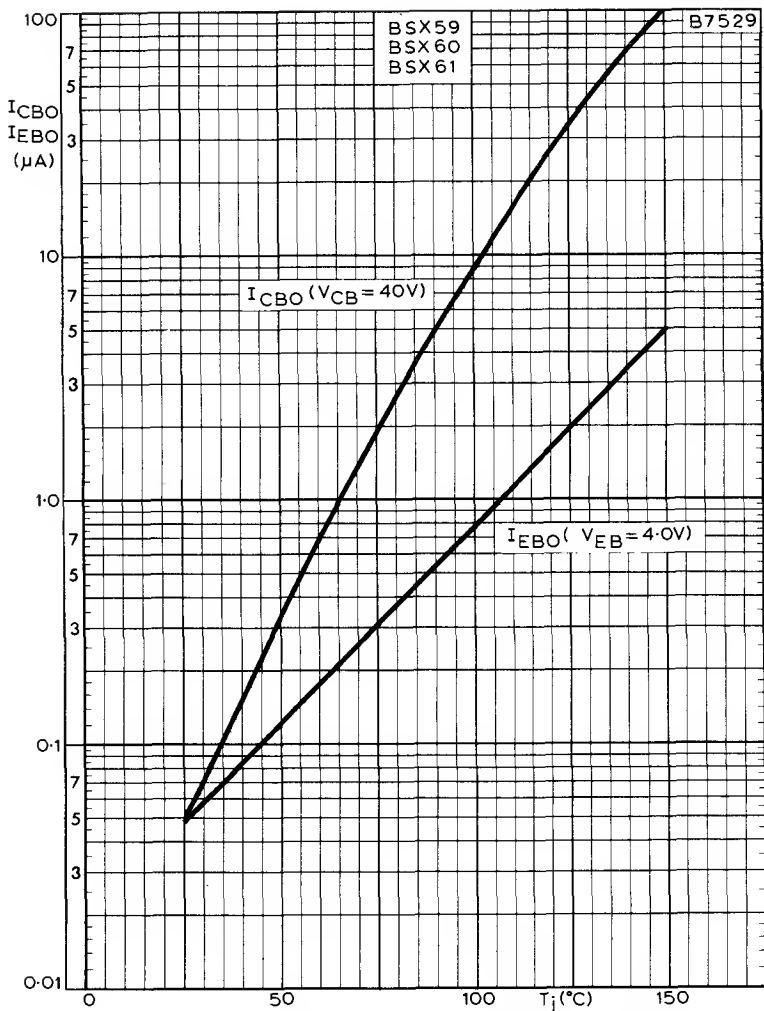
TYPICAL VARIATION OF INPUT CAPACITANCE WITH
BASE-EMITTER VOLTAGE



TYPICAL VARIATION OF OUTPUT CAPACITANCE WITH
COLLECTOR-BASE VOLTAGE



TYPICAL VARIATION OF TURN-ON AND TURN-OFF TIME
WITH JUNCTION TEMPERATURE



TYPICAL VARIATION OF COLLECTOR AND EMITTER CUT-OFF
CURRENT WITH JUNCTION TEMPERATURE

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BSY95A

Silicon planar epitaxial n-p-n transistor for general purpose low level switching applications.

QUICK REFERENCE DATA

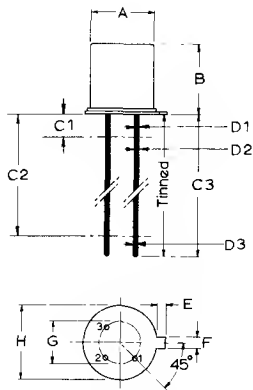
V_{CBO} max.	20	V
V_{CEO} max.	15	V
I_{CM} max.	200	mA
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	300	mW
h_{FE} ($I_C = 10mA$)	50-200	
f_T min. ($I_C = 10mA$, $V_{CE} = 9.0V$, $f = 100MHz$)	200	MHz
t_s max.	50	ns

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-18

B.S. 3934 SO-12A/SB3-6A

	Millimetres		
	Min.	Typ.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84



Viewed from underside

Connections 1. Emitter 3. Collector connected to envelope
2. Base

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	20	V
V_{CEO} max.	15	V
V_{EBO} max.	5.0	V
$*I_{C(AV)}$ max.	100	mA
I_{CM} max.	200	mA
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	300	mW

*Averaged over any 20ms period.

Temperature

T_{stg} min.	-65	$^{\circ}C$
T_{stg} max.	175	$^{\circ}C$
T_j max. (operating)	175	$^{\circ}C$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.5	degC/mW
-----------------	-----	---------

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$ unless otherwise stated)

		Min.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 16V, I_E = 0$	-	50	nA
$V_{BR(CBO)}$	Collector-base breakdown voltage $I_C = 1.0\mu A$	20	-	V
I_{EBO}	Emitter cut-off current $V_{EB} = 1.5V, I_C = 0$	-	25	nA
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 10\mu A$	5.0	-	V
I_{CEO}	Collector-emitter cut-off current $V_{CE} = 12V, I_B = 0$	-	250	nA
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_C = 10mA^{**}$	15	-	V
f_T	Transition frequency $I_C = 10mA, V_{CE} = 9.0V,$ $f = 100MHz$	200	-	MHz

** Pulsed: Pulse width = 300 μs , duty cycle < 2%.

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BSY95A

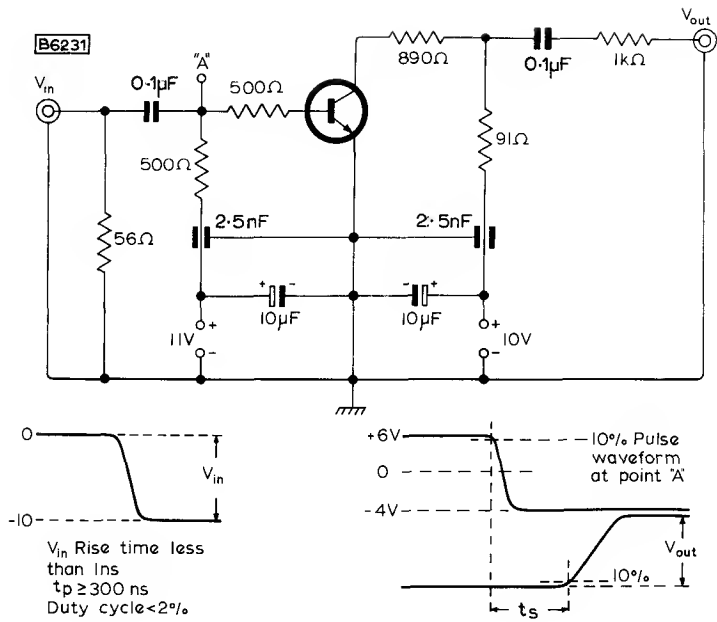
		Min.	Max.	
h_{FE}	Common emitter forward current transfer ratio $I_C = 1.0\text{mA}$, $V_{CE} = 0.35\text{V}$	30	-	
	$I_C = 10\text{mA}$, $V_{CE} = 0.35\text{V}$	50	200	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 10\text{mA}$, $I_B = 0.2\text{mA}$	-	0.35	V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 10\text{mA}$, $I_B = 0.2\text{mA}$	0.67	0.87	V
C_{ob}	Collector-base capacitance $V_{CB} = 9.0\text{V}$, $I_E = 0$ $f = 1.0\text{MHz}$	-	6.0	pF
t_s	Storage time $I_C = 10\text{mA}$ See test circuit on page 4	-	50	ns

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

Mullard

STORAGE TIME TEST CIRCUIT



Input and output waveforms

HIGH VOLTAGE N-P-N SILICON POWER TRANSISTOR

BU126

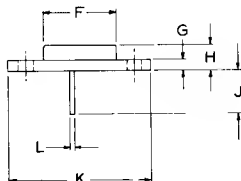
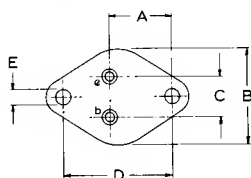
High voltage n-p-n silicon power transistor intended for use in the switched mode power supply of television receivers.

QUICK REFERENCE DATA

V_{CESM} max. ($V_{BE} = 0$)	750	V
V_{CEXM} max. ($-V_{BE} = 1.5V$)	750	V
I_{CM} max. (peak value)	6	A
P_{tot} max. ($T_{mb} \leq 50^{\circ}C$)	30	W
$V_{CE(sat)}$ max. ($I_C = 2.5A$, $I_B = 0.25A$)	10	V
t_f typ. ($I_{CM} = 2.5A$, $I_{B(end)} = 0.25A$)	0.15	μs

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-5A/SB2-2
J. E. D. E. C. TO-3



Millimetres

	Min.	Nom.	Max.
A	-	16.9	-
B	-	-	26.6
C	-	10.9	-
D	-	30.1	-
E	4.0	-	4.2
F	-	-	20.3
G	-	3.15	-
H	-	-	9.5
J	11	-	13
K	-	-	39.5
L	-	1.0	-

Collector electrically connected
to the envelope

ACCESSORIES

56201 consisting of: - 56201A (insulating bushes) and 56201B (mica washer)
56214 lead washer

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CESM}	max. ($V_{BE} = 0$) (peak value)	750	V
V_{CEXM}	max. ($-V_{BE} = 1.5V$) (peak value)	750	V
V_{CEO}	max. (open base)	300	V
I_C	max. (d. c.)	3	A
I_{CM}	max. (peak value)	6	A
$-I_{CM}$	max. (peak value)	3	A
I_B	max. (d. c.)	2	A
I_{BM}	max. (peak value)	2	A
$-I_{B(AV)}$	max. (d. c. or averaged over any 20ms period)	100	mA
$-I_{BM}$	max. (peak value, turn-off current)	1.5	A
P_{tot}	max. ($T_{mb} \leq 50^\circ C$)	30	W

Temperature

T_{stg}	range	-65 to +125	$^\circ C$
T_j	max.	+125	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$		2.5	$^\circ C/W$
$R_{th(mb-hs)}$	with mica washer and lead washer	0.75	$^\circ C/W$
$R_{th(mb-hs)}$	with lead washer only	0.5	$^\circ C/W$

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.
I_{CES}	Collector cut-off current † $V_{CE} = 750V$; $V_{BE} = 0$	-	-	0.5 mA
	$V_{CE} = 750V$; $V_{BE} = 0$, $T_j = 125^\circ C$	-	-	2 mA
I_{EBO}	Emitter cut-off current $I_C = 0$; $V_{EB} = 6V$	-	-	5 mA
h_{FE}	Large signal forward current transfer ratio $I_C = 1A$; $V_{CE} = 5V$	15	-	60
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 2.5A$; $I_B = 0.25A$	-	-	10 V
	$I_C = 4A$; $I_B = 1A$	-	-	5 V

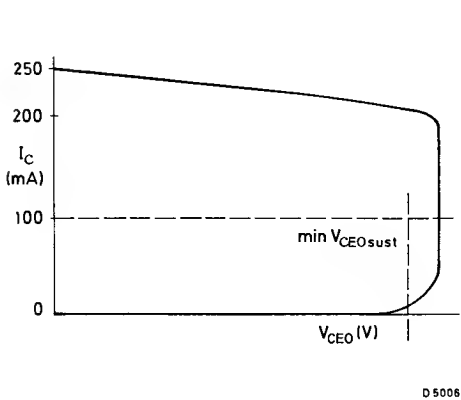
†Measured with a half sinewave voltage (curve tracer).

HIGH VOLTAGE N-P-N SILICON POWER TRANSISTOR

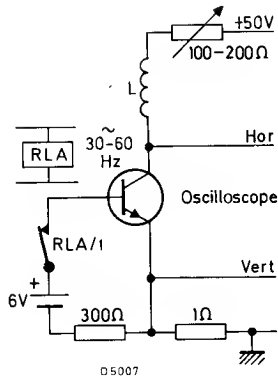
BU126

ELECTRICAL CHARACTERISTIC (contd.)

		Min.	Typ.	Max.
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 2.5A, I_B = 0.25A$	-	-	1.5 V
$V_{CEO(sust)}$	Collector-emitter sustaining voltage $I_B = 0; I_C = 100mA; L = 25mH$	300	-	V



Oscilloscope display for $V_{CEO\text{ sust}}$

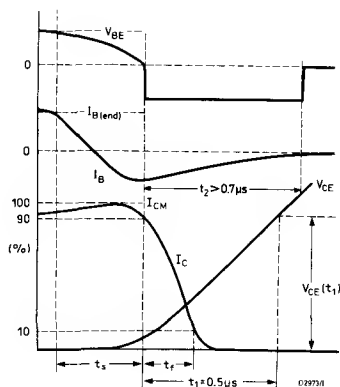
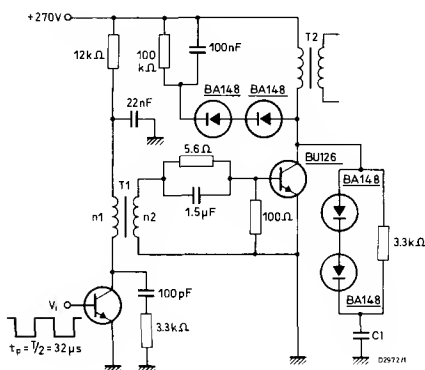


Test circuit for $V_{CEO\text{ sust}}$

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.
f_T	Transition frequency $I_C = 0.2A$, $V_{CE} = 10V$, $f = 1MHz$	-	8	- MHz
C_{Tc}	Collector capacitance $I_E = I_c = 0$, $V_{CB} = 10V$, $f = 1MHz$	-	85	- pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 2V$, $f = 1kHz$	-	1.4	- nF
Turn-off time $I_{CM} = 2.5A$, $I_{B(end)} = 0.25A$				
t_s	Storage time	-	1.2	- μs
t_f	Fall time	-	0.15	- μs

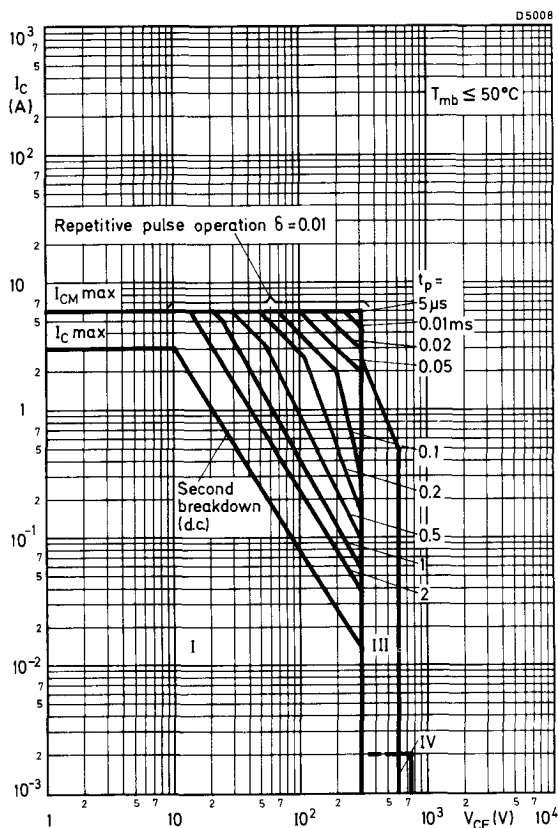
Practical turn-off circuit



		Min.	Typ.	Max.
$V_{CE}(t_1)$	Allowable value of V_{CE} after $0.5\mu s$	-	-	500 V
T1	Core EI 25 n1 = 350 turns, 100mH n2 = 32 turns Leakage inductance at secondary $3\mu H$			

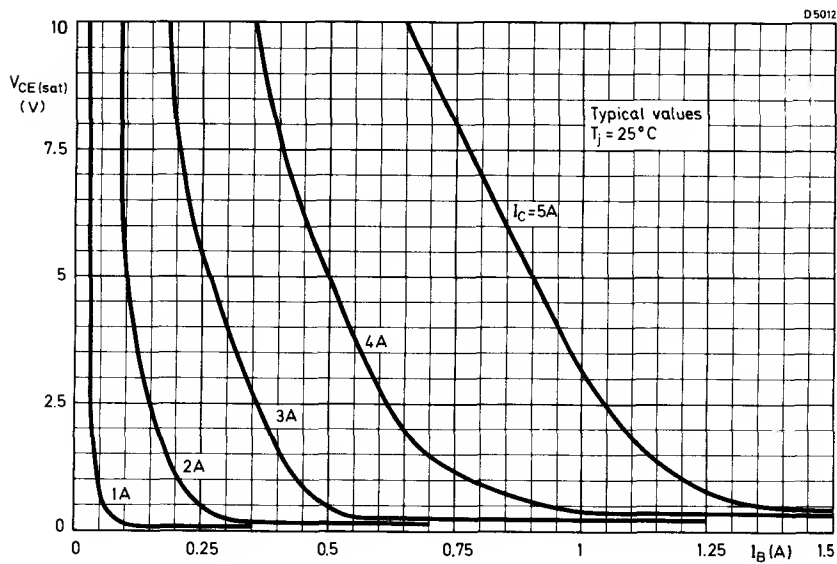
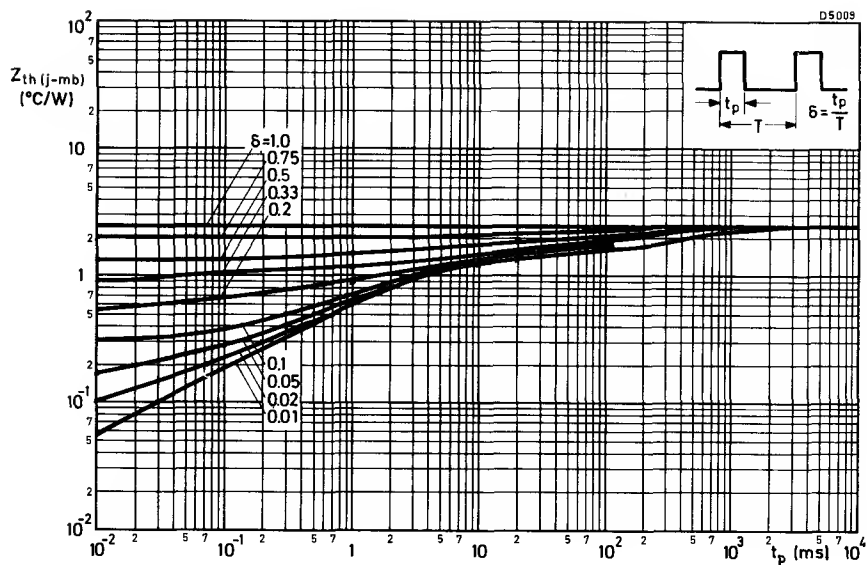
The value of C_1 depends on the stray capacitance of T_2 and on the capacitive loading of the secondary (typical value for C_1 is $1.5nF$).

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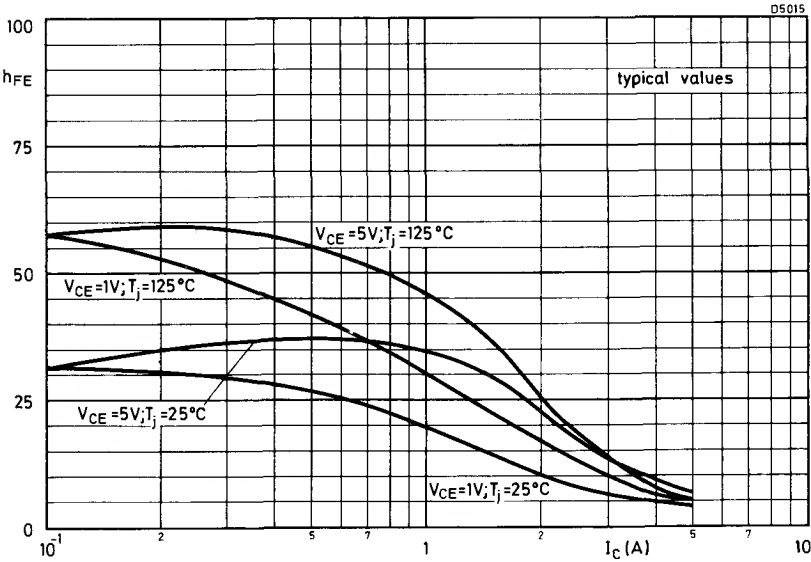
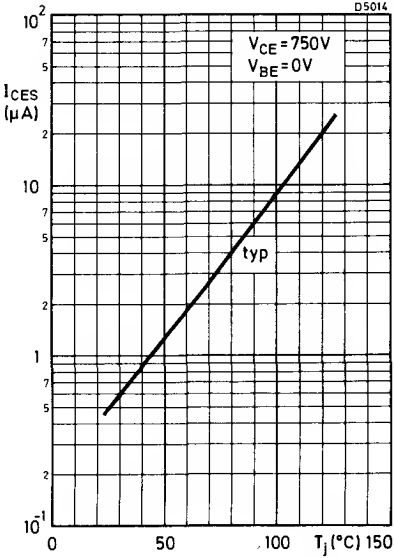
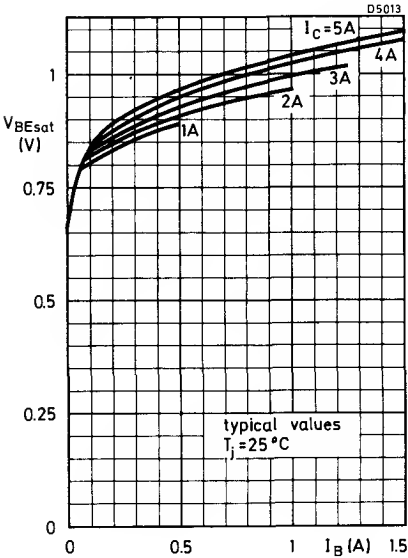
Safe Operating Area (Regions I, II and III forward biased)

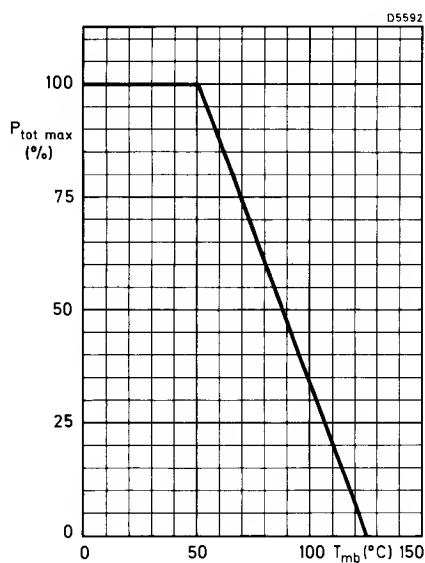
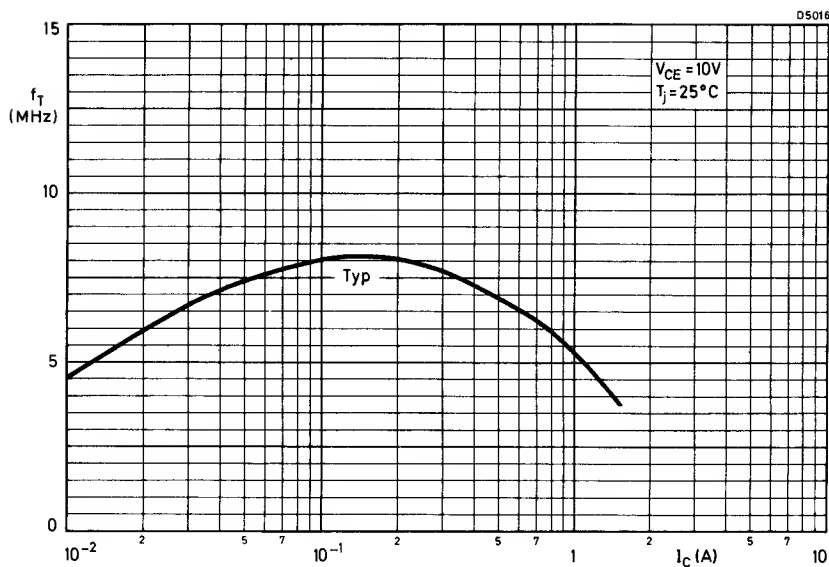
- I Region of permissible d.c. operation
- II Permissible extension for repetitive pulse operation
- III Area of permissible operation during turn-on in switched mode power supply circuits, provided $t_p \leq 0.6\mu\text{s}$ and $R_{BE} \leq 100\Omega$
- IV Repetitive pulse operation in this region is allowable, provided $V_{BE} \leq 0$ and $t_p \leq 2\text{ms}$



HIGH VOLTAGE N-P-N
SILICON POWER TRANSISTOR

BU126





APPLICATION INFORMATION (Note 1)

Switched-mode power supply circuits

Important factors in the design of switched-mode power supply circuits are the power losses and heatsink requirements of the output transistor and the base drive condition during turn-off. The basic arrangements for parallel and series-type switched-mode circuits are shown in Figs. 1, 2 and 3, together with the basic waveforms.

In power supply circuits for colour receivers the duty cycle δ varies between 0.4 and 0.6. Fig. 4 gives the nominal value of the recommended base current I_{Bend} versus the maximum peak collector current (which occurs at maximum load and minimum input voltage). Fig. 5 shows the base current waveform during turn-off.

Fig. 6 gives the total device dissipation P_{tot} versus the maximum peak collector current. The max. permissible thermal resistance for the heatsink can be calculated from:

$$R_{th(mb-a)max} \text{ (Note 2)} = \frac{T_{jmax} - T_{amb}}{P_{tot}} - R_{thj-mb}$$

For the BU126: $T_{jmax} = 125^{\circ}\text{C}$ and $R_{thj-mb} = 2,5^{\circ}\text{C/W}$

To ensure thermal stability, the thermal resistance of the heatsink used must not exceed the value plotted in Fig. 7.

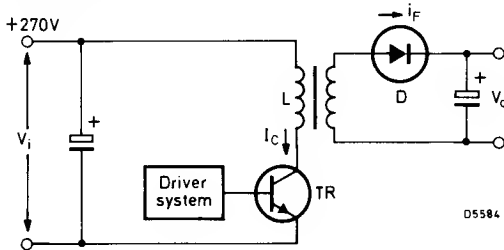
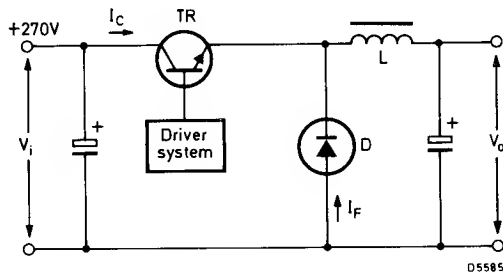


Fig. 1 Parallel type switched-mode power supply, basic circuit arrangement.

D5584

Fig. 2 Series type switched-mode power supply, basic circuit arrangement.



D5585

NOTES

1. Detailed application information available on request.
2. Including additional thermal resistances resulting from mounting hardware.

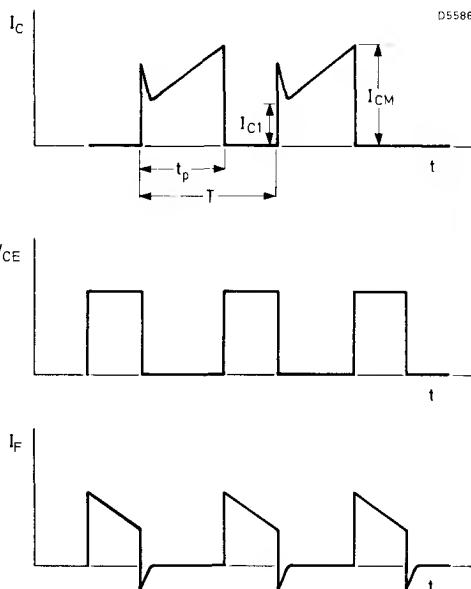


Fig. 3 Waveforms applying to switched-mode power supplies.

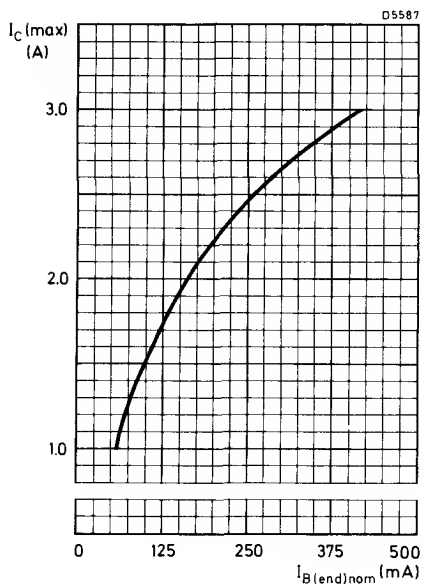


Fig. 4 Recommended nominal value of base current versus max. peak collector current.
Applies for ratio $I_{CM}/I_{C1} \geq 2$ (Fig. 3).

APPLICATION INFORMATION
(continued)

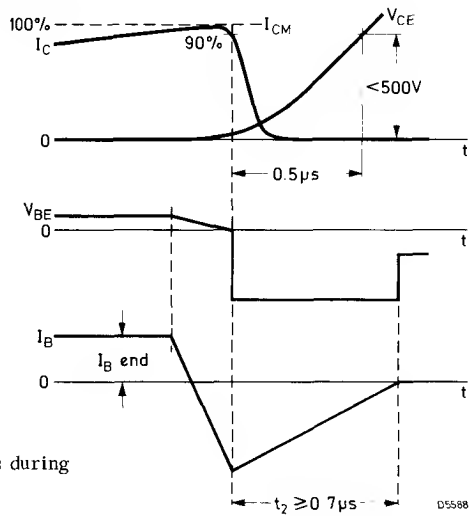


Fig. 5 Basic waveforms during current turn-off

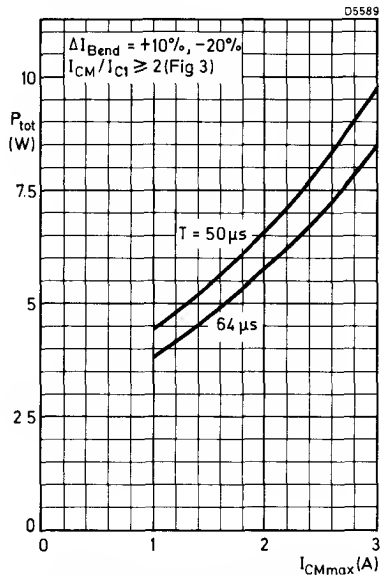


Fig. 6 Total transistor dissipation versus max. peak collector current.

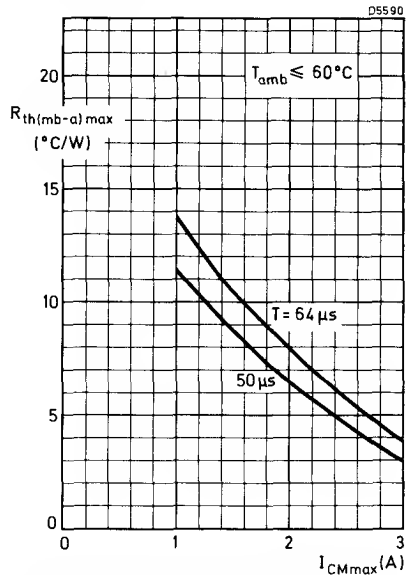
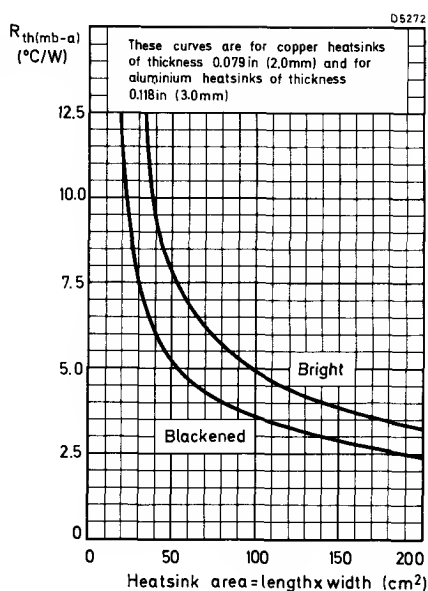
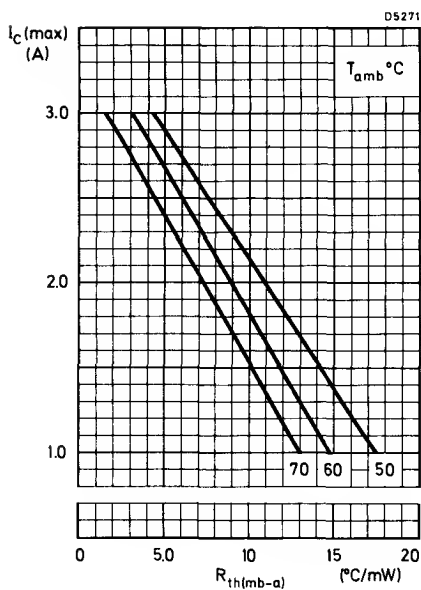
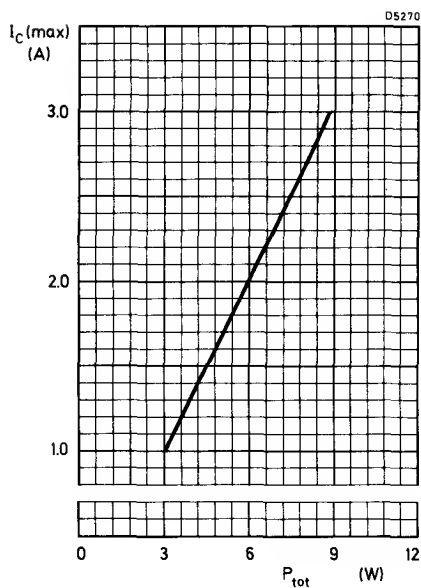


Fig. 7 Max. allowable value of $R_{th(mb-a)}$ to ensure thermal stability.



HIGH VOLTAGE
SILICON POWER TRANSISTOR

BU133

High voltage n-p-n power transistor intended for general purpose consumer applications.

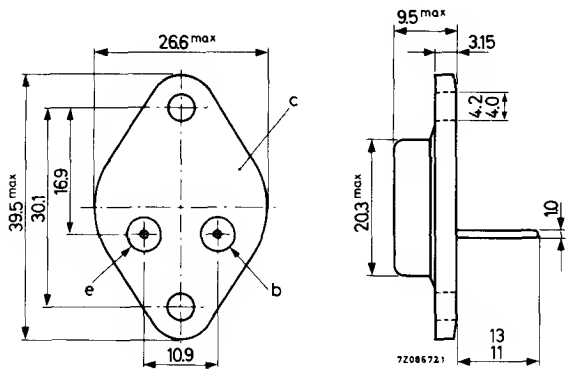
QUICK REFERENCE DATA				
Collector-emitter voltage ($V_{BE} = 0$) (peak value)	V_{CESM}	max.	750	V
Collector current (peak value)	I_{CM}	max.	6	A
Total power dissipation up to $T_{mb} = 50^{\circ}C$	P_{tot}	max.	30	W
Collector-emitter saturation voltage $I_C = 2.5A; I_B = 0.25A$	$V_{CE sat}$	<	10	V
Fall time $I_{CM} = 2.5A; I_{B1} = -I_{B2} = 0.5A; V_{CC} = 125V$	t_f	typ.	0.5	μs

MECHANICAL DATA

Dimensions in mm

Collector connected to case

TO-3



Accessories available: 56201 and 56214

RATINGS Limiting values of operation according to the absolute maximum system.

Voltages

Collector-emitter voltage ($V_{BE} = 0$) (peak value)	V_{CESM}	max.	750	V
Collector-emitter voltage ($-V_{BE} = 1.5V$) (peak value)	V_{CEXM}	max.	750	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	V

Currents

Collector current (d. c.)	I_C	max.	3	A
Collector current (peak value)	I_{CM}	max.	6	A
Reverse collector current (peak value)	$-I_{CM}$	max.	3	A
Base current (d. c.)	I_B	max.	2	A
Base current (peak value)	I_{BM}	max.	2	A
Reverse base current (d. c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100	mA
Reverse base current (peak value) (note 1)	$-I_{BM}$	max.	1.5	A

Power dissipation

Total power dissipation up to $T_{mb} = 50^{\circ}C$	P_{tot}	max.	30	W
--	-----------	------	----	---

Temperatures

Storage temperature	T_{stg}	-65 to +125	$^{\circ}C$
Junction temperature	T_j	max. 125	$^{\circ}C$

THERMAL RESISTANCE

From junction to mounting base	$R_{th(j-mb)}$	=	2.5 $^{\circ}C/W$
From mounting base to heatsink with mica washer and lead washer (56201 and 56214)	$R_{th mb-h}$	=	0.75 $^{\circ}C/W$
with lead washer (56214) only	$R_{th mb-h}$	=	0.5 $^{\circ}C/W$

Notes

1. Turn-off current.

HIGH VOLTAGE SILICON POWER TRANSISTOR

BU133

CHARACTERISTICS $T_j = 25^{\circ}\text{C}$ unless otherwise specified

Collector cut-off current (note 2)

$$V_{CEM} = 750\text{V}; V_{BE} = 0$$

$$V_{CEM} = 750\text{V}; V_{BE} = 0, T_j = 125^{\circ}\text{C}$$

$$I_{CES} < 0.5 \text{ mA}$$

$$I_{CES} < 2 \text{ mA}$$

Emitter cut-off current

$$I_C = 0; V_{EB} = 6\text{V}$$

$$I_{EBO} < 5 \text{ mA}$$

D.C. current gain

$$I_C = 1\text{A}; V_{CE} = 5\text{V}$$

$$h_{FE} \quad 15 \text{ to } 80$$

Saturation voltages

$$I_C = 2.5\text{A}; I_B = 0.25\text{A}$$

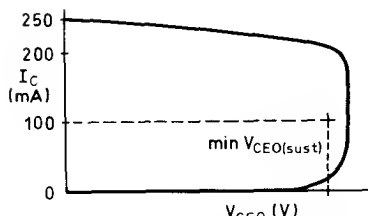
$$V_{CE \text{ sat}} < 10 \text{ V}$$

$$V_{BE \text{ sat}} < 1.5 \text{ V}$$

Collector-emitter sustaining voltage

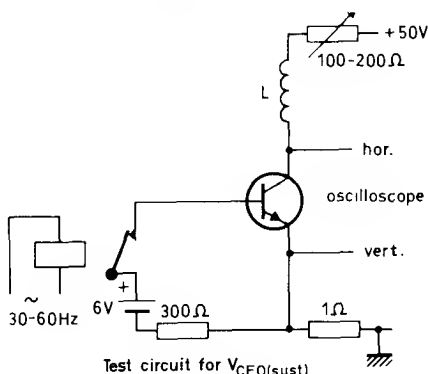
$$I_B = 0; I_C = 100\text{mA}; L = 25\text{mH}$$

$$V_{CEO \text{ sust}} > 250 \text{ V}$$



Oscilloscope display for $V_{CEO(sust)}$

D4039



D4038

Notes

2. Measured with a half sine wave voltage (curve tracer).

Mullard

CHARACTERISTICS (contd.) $T_j = 25^{\circ}\text{C}$ unless otherwise specified

Transition frequency at $f = 1\text{MHz}$

$$I_C = 0.2\text{A}; V_{CE} = 10\text{V}$$

f_T typ. 8 MHz

Collector capacitance at $f = 1\text{MHz}$

$$I_E = I_e = 0; V_{CB} = 10\text{V}$$

C_c typ. 85 pF

Emitter capacitance at $f = 1\text{kHz}$

$$I_C = I_c = 0; V_{EB} = 2\text{V}$$

C_e typ. 1.4 nF

Switching times

$$I_C = 2.5\text{A}; I_{B1} = -I_{B2} = 0.5\text{A}; V_{CC} = 125\text{V}$$

turn-off storage time

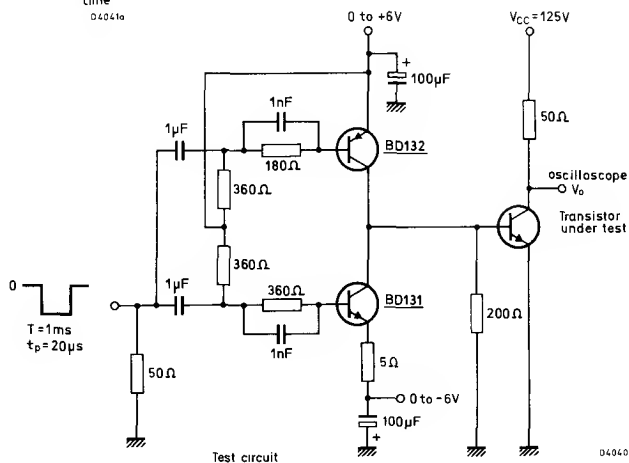
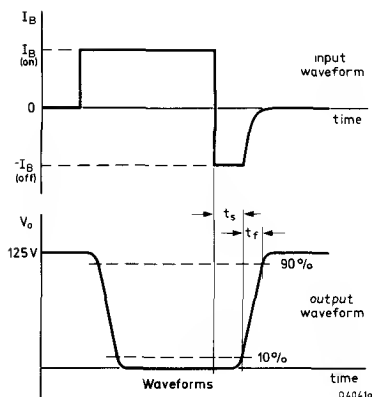
t_s typ. 2 ns

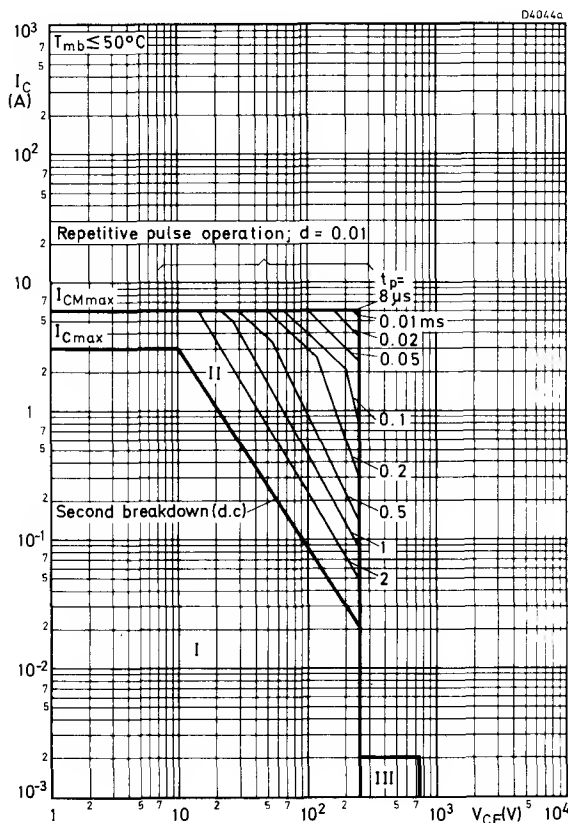
turn-off fall time

t_f typ. 0.5 μs

turn-off fall time, $T_{mb} = 95^{\circ}\text{C}$

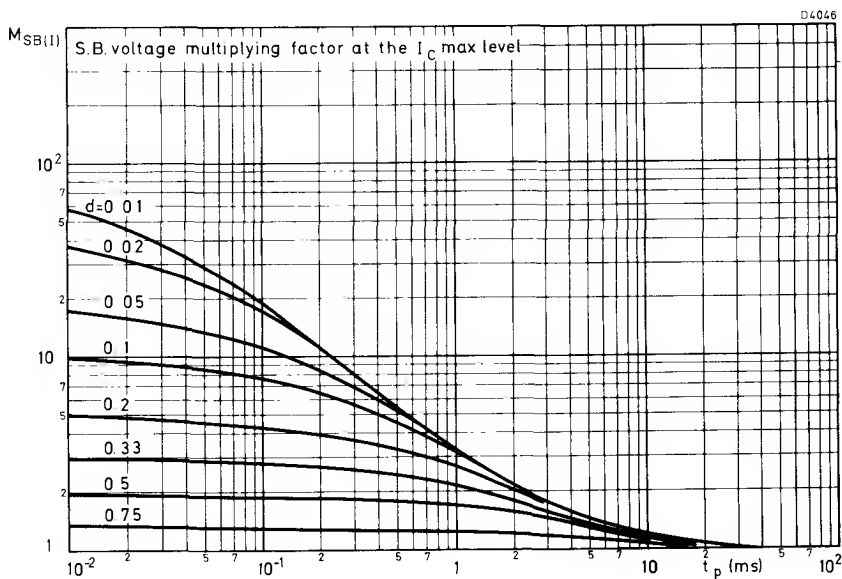
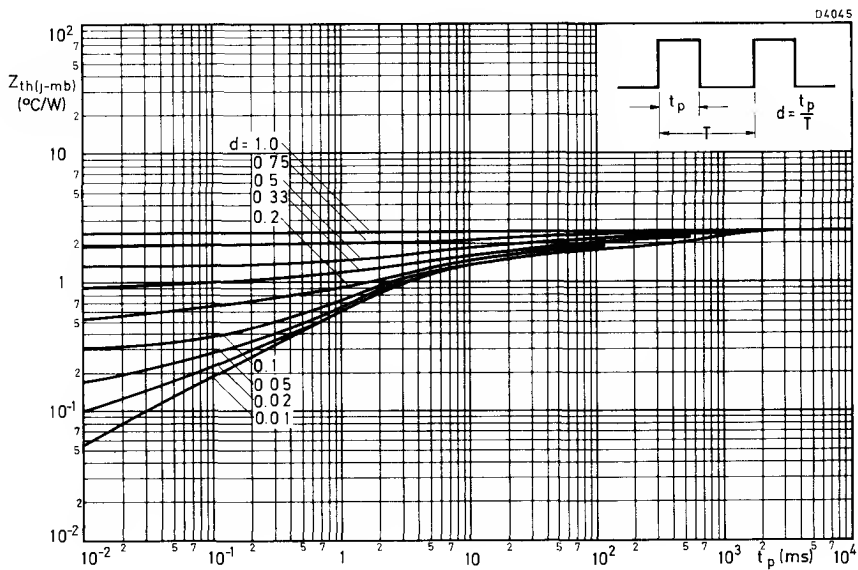
$t_f < 2 \mu\text{s}$

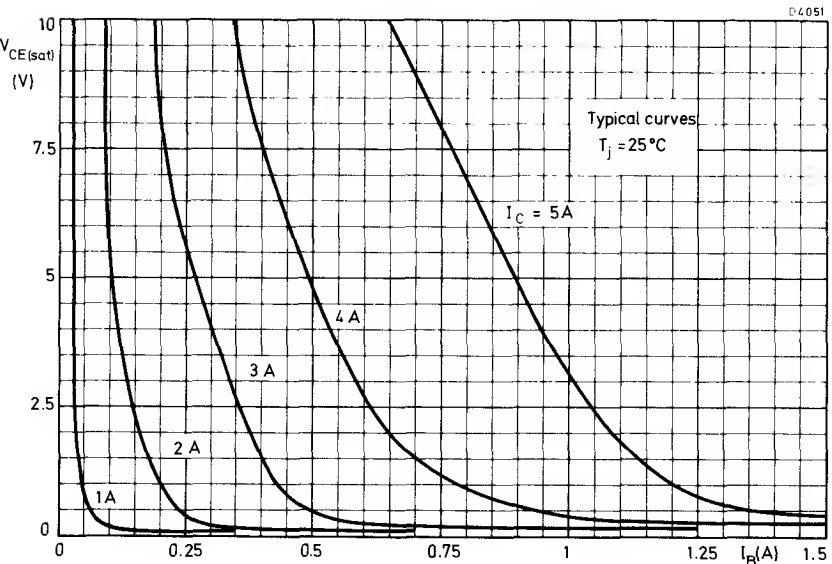
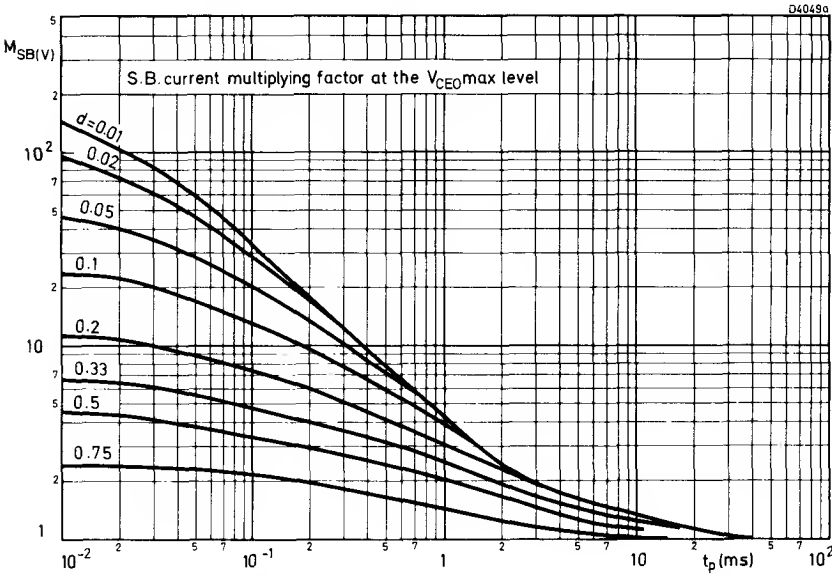


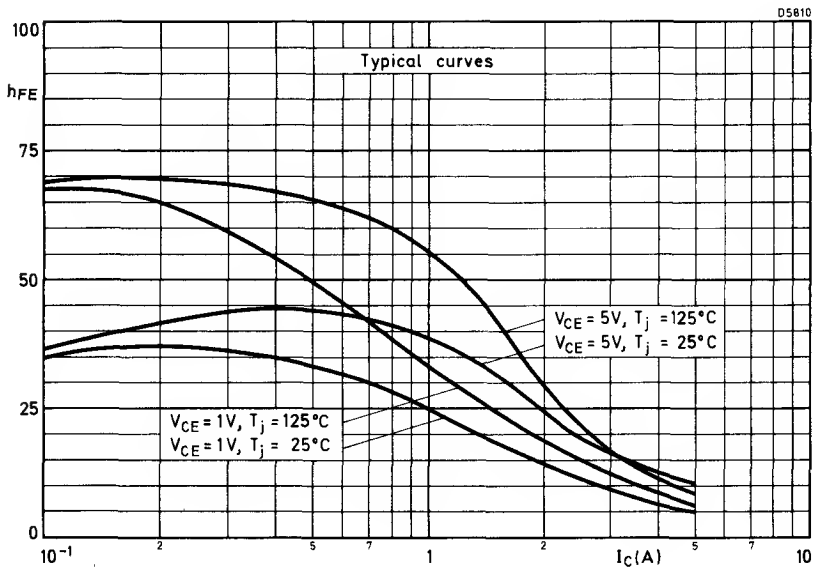
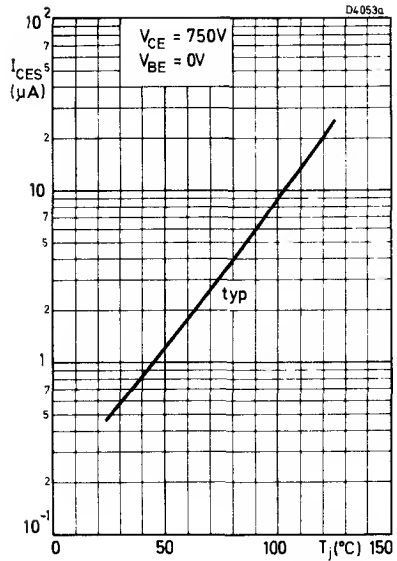
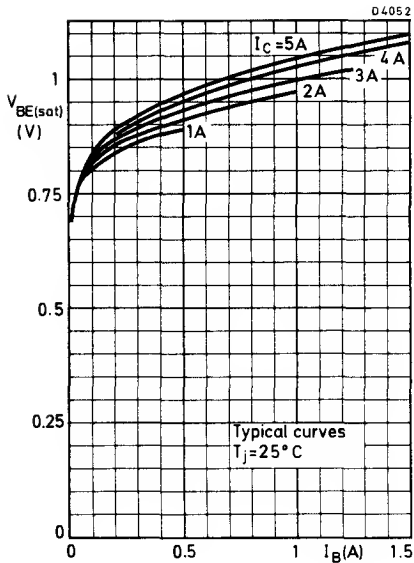


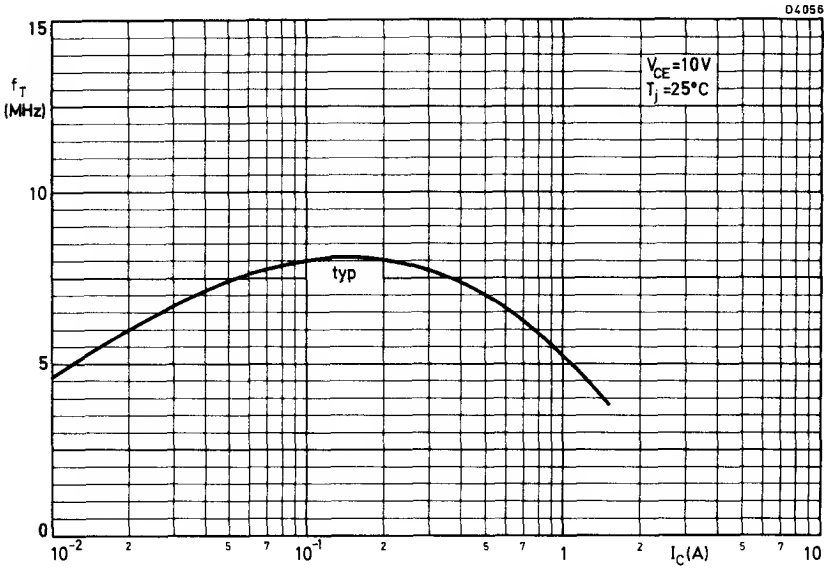
Safe Operating Area (Regions I and II forward biased)

- I Region of permissible d.c. operation
- II Permissible extension for repetitive pulsed operation
- III Repetitive pulsed operation in this region is allowable, provided $V_{BE} \leq 0V$ and $t_p \leq 2ms$









TENTATIVE DATA

The BU204, 205 and 206 are N-P-N High voltage power transistors intended for use in line output stages of television receivers.

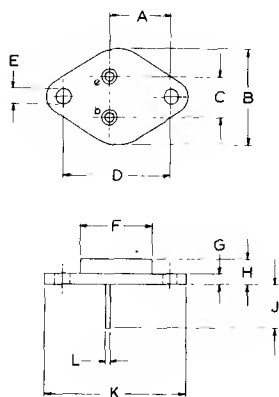
QUICK REFERENCE DATA

	BU204	BU205	BU206	
V_{CESM} max.	1300	1500	1700	V
I_C max. (d. c.)	2.5	2.5	2.5	A
P_{tot} max. ($T_{mb} \leq 90^\circ C$)	10	10	10	W
h_{FE} min. ($V_{CE} = 5V$; $I_C = 2A$)	2	2	1.8	
t_f typ. ($I_C = 2A$; $I_B = 1A$)	0.75	0.75	0.75	μs

OUTLINE AND DIMENSIONS

Conforms to BS3934 SO-5A/SB2-2

J. E. D. E. C. TO-3



	Millimetres		
	Min.	Nom.	Max.
A	-	16.9	-
B	-	-	26.6
C	-	10.9	-
D	-	30.1	-
E	4.0	-	4.2
F	-	-	20.3
G	-	3.15	-
H	-	-	9.5
J	11	-	13
K	-	-	39.5
L	-	1.0	-

Accessories available (High voltage types)

56336A insulated bushes, 56336B mica washer,

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BU204	BU205	BU206	
V_{CESM} max. ($V_{BE} = 0$)	1300	1500	1700	V
V_{CERM} max. ($R_{BE} \leq 100\Omega$)	1300	1500	1700	V
V_{CEO} max. (open base)	600	700	800	V
I_C max. (d. c.)	2.5	2.5	2.5	V
I_{CM} max. (peak value)	3.0	3.0	3.0	A
I_{BM} max. (peak value)	2.5	2.5	2.5	A
$-I_{BM}$ max. (peak value)* note 1	1.5	1.5	1.5	A
P_{tot} power dissipation (max)				
$T_{mb} \leq 90^\circ C$	10	10	10	W

TRANSIENT RATINGS (During flashover)

V_{CE} "Flashover"	1500	1650	1750	V
I_C "Flashover"	5	5	5	A

Temperature

T_{stg} range	-65 to +115	$^\circ C$
T_j (operating) max.	115	$^\circ C$

THERMAL CHARACTERISTICS

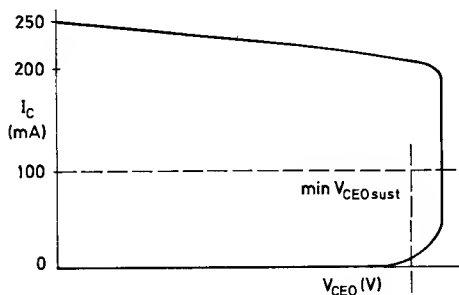
$R_{th(j-mb)}$	2.5	$^\circ C/W$
$R_{th(mb-h)}$ using mica washer 56336B	1.0	$^\circ C/W$

*Note 1

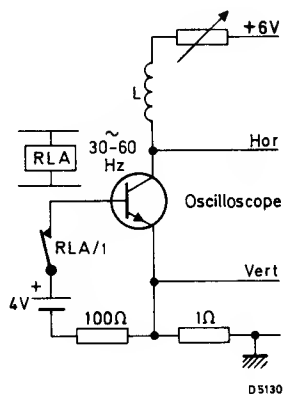
Turn off current in line deflection circuits.

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		BU204	BU205	BU206	
I_{CES}	Collector cut-off current (max) $V_{BE} = 0; V_{CE} = V_{CESM}$	1.0	1.0	1.0	mA
$h_{FE} \text{ (min)}$	Static forward current transfer ratio ($I_C = 2\text{A}; V_{CE} = 5\text{V}$)	2	2	1.8	
$+V_{EBO}$	Emitter-base voltage ($I_C = 0; I_E = 10\text{mA}$) (min)	5	5	5	V
	($I_C = 0; I_E = 100\text{mA}$) (typ)	7	7	7	V
$V_{CE(sat)}$	Collector-emitter saturation voltage (max) ($I_C = 2\text{A}; I_B = 1.0\text{A}$)	5	5	-	V
	($I_C = 2\text{A}; I_B = 1.1\text{A}$)	-	-	5	V
$V_{BE(sat)}$	Base-emitter saturation voltage (max) ($I_C = 2\text{A}; I_B = 1.0\text{A}$)	1.5	1.5	-	V
	($I_C = 2\text{A}; I_B = 1.1\text{A}$)	-	-	1.5	V
$V_{CEO(sust)}$	Collector-emitter sustaining voltage (min) ($I_B = 0; I_C = 100\text{mA}; L = 25\text{mH}$)	600	700	800	V

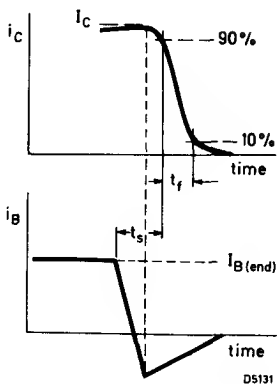


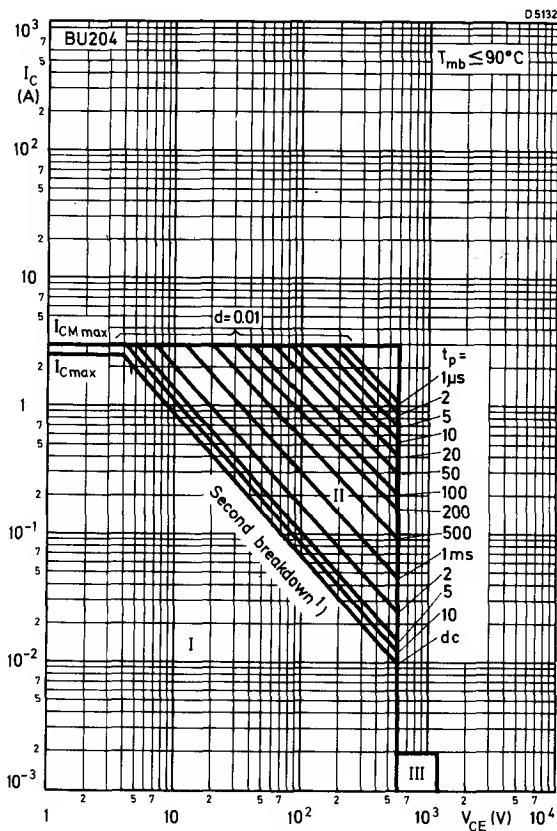
D 5129



ELECTRICAL CHARACTERISTICS (cont)

		BU204	BU205	BU206	
f_T	Transition frequency (typ) ($f = 5\text{MHz}$; $I_C = 0.1\text{A}$; $V_{CE} = 5\text{V}$)	7.5	7.5	7.5	MHz
C_{TC}	Collector capacitance (typ) ($f = 1\text{MHz}$; $I_E = I_e = 0$; $V_{CB} = 10\text{V}$)	65	65	65	pF
	Switching times (in line deflection circuit) ($I_C = 2\text{A}$; $I_{B(\text{end})} = 1\text{A}$; $L_B = 25\mu\text{H}$)				
t_f	Fall time (typ)	0.75	0.75	0.75	μs
t_s	Storage time (typ)	10	10	10	μs



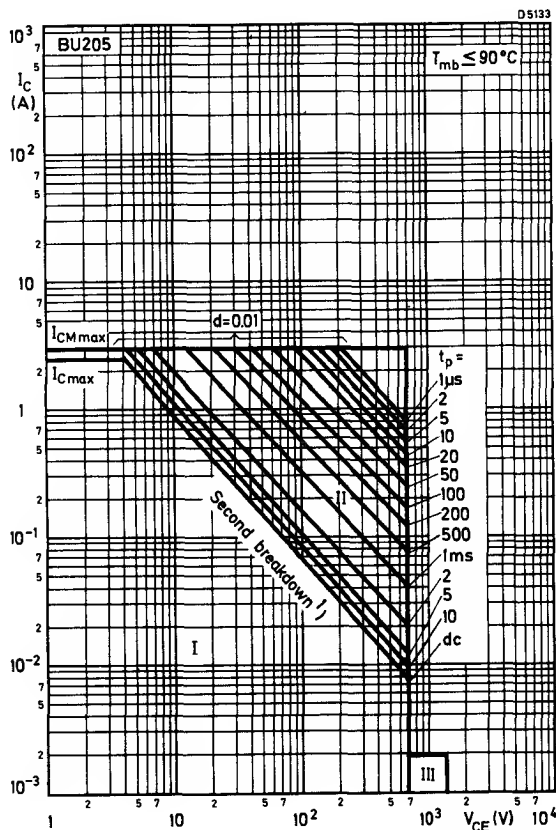


Safe Operation Area with the transistor forward biased.

I Region of permissible d. c. operation.

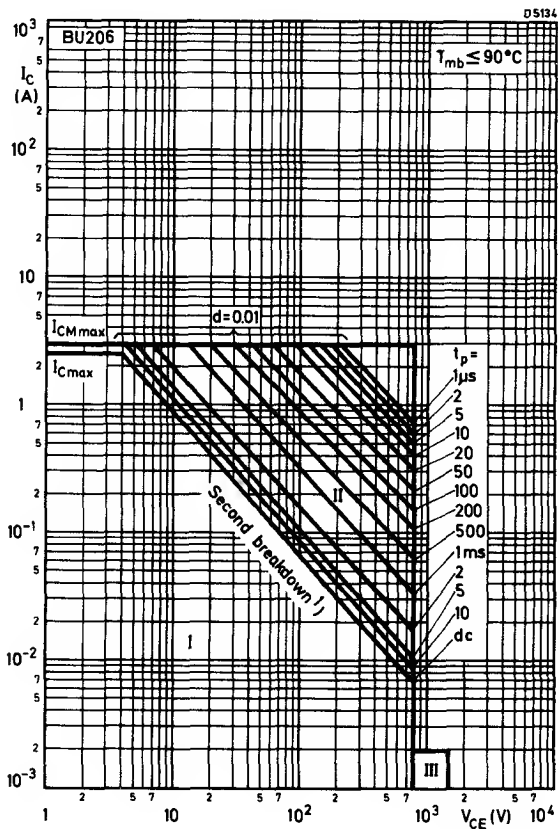
II Permissible extension for repetitive pulse operation.

III Repetitive pulse operation in this region is allowable,
provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu\text{s}$; $\delta \leq 0.25$.



Safe Operation Area with the transistor forward biased.

- I Region of permissible d. c. operation.
- II Permissible extension for repetitive pulse operation.
- III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu\text{s}$; $\delta \leq 0.25$.

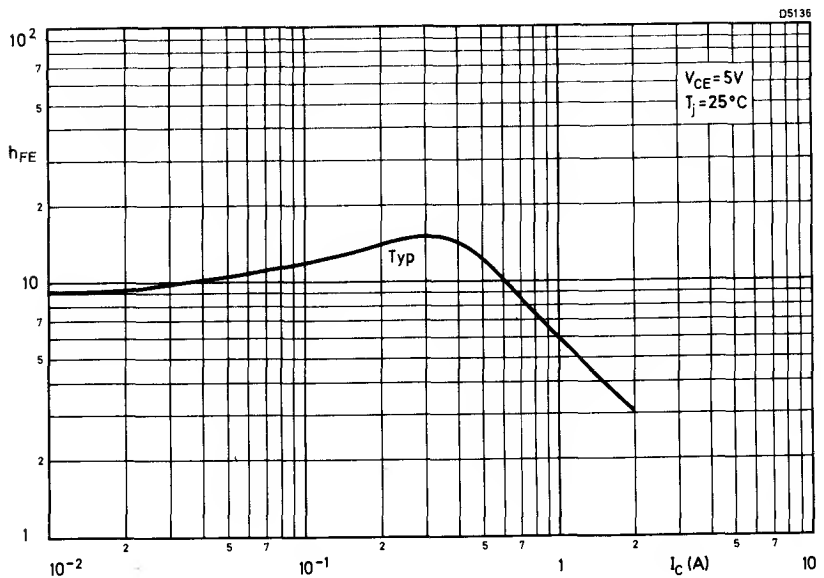
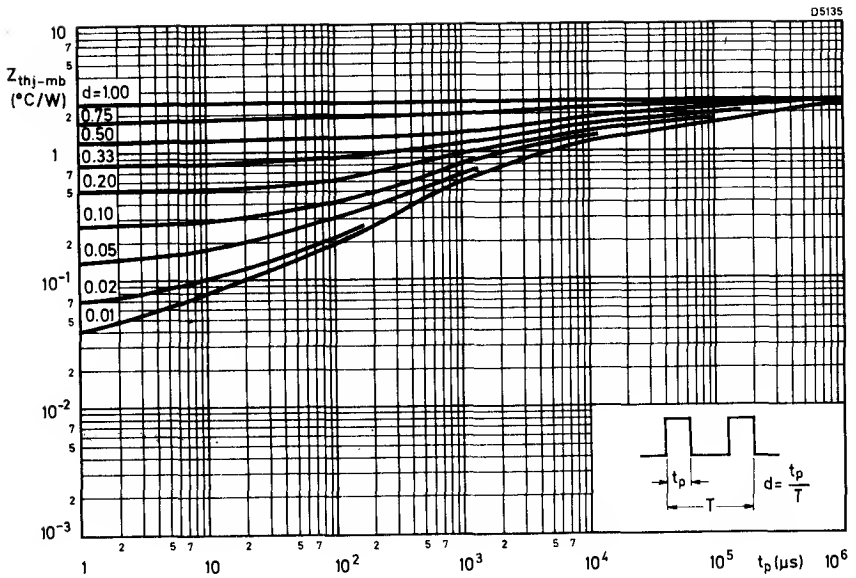


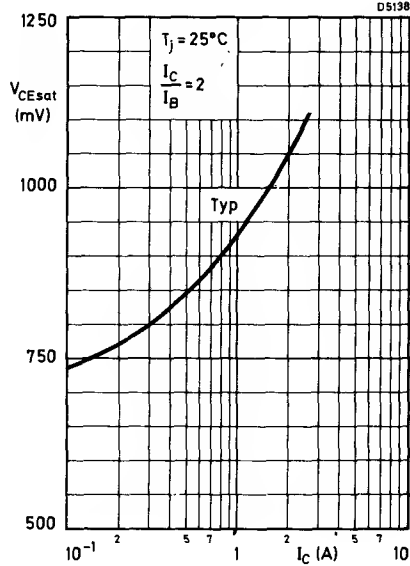
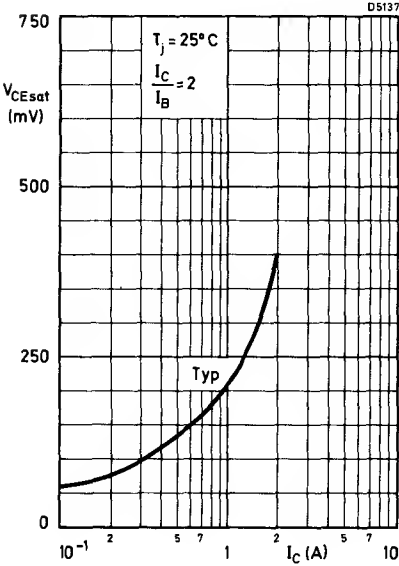
Safe Operating Area with the transistor forward biased.

I Region of permissible d. c. operation.

II Permissible extension for repetitive pulse operation.

III Repetitive pulse operation in this region is allowable,
provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.





TENTATIVE DATA

The BU207, 208 and 209 are N-P-N High voltage power transistors in metal envelopes intended for use in line output stages of colour television receivers.

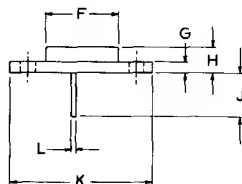
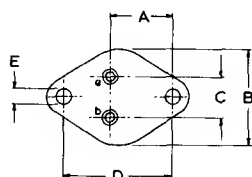
QUICK REFERENCE DATA

	BU207	BU208	BU209	
V_{CESM} max. ($V_{BE} = 0$; peak value)	1300	1500	1700	V
I_C max. (d. c.)	5	5	4	A
P_{tot} max. ($T_{mb} \leq 95^\circ C$)	12.5	12.5	12.5	W
h_{FE} (min) ($I_C = 4.5A$; $V_{CE} = 5V$)	2.25	2.25	-	
($I_C = 3A$; $V_{CE} = 5V$)	-	-	2.25	
t_f (typ) ($I_C = 4.5A$; $I_B = 1.8A$)	0.9	0.7	-	μs
($I_C = 3A$; $I_B = 1.3A$)	-	-	0.7	μs

OUTLINE AND DIMENSIONS.

Conforms to BS3934 SO-5A/SB2-2
J. E. D. E. C. TO-3.

Millimetres



	Min.	Nom.	Max.
A	-	16.9	-
B	-	-	26.6
C	-	10.9	-
D	-	30.1	-
E	4.0	-	4.2
F	-	-	20.3
G	-	3.15	-
H	-	-	9.5
J	11	-	13
K	-	-	39.5
L	-	1.0	-

Accessories available (High voltage types)

56336A insulated bushes, 56336B mica washer.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BU207	BU208	BU209	
V_{CESM} max. ($V_{BE} = 0$, peak value)	1300	1500	1700	V
V_{CERM} max. ($R_{BE} \leq 100\Omega$, peak value)	1300	1500	1700	V
V_{CEO} max. (open base)	600	700	800	V
I_C max. (d. c.)	5	5	4	A
I_{CM} max. (peak value)	7.5	7.5	6	A
I_{BM} max. (peak value)	4	4	4	A
$-I_{B(AV)}$ max. (d. c. or average over any 20ms period)	100	100	100	mA
$-I_{BM}$ max. (peak value, see note 1)	2.5	2.5	2.5	A
P_{tot} max. ($T_{mb} \leq 95^\circ\text{C}$)	12.5	12.5	12.5	W

TRANSIENT RATINGS (During flashover)

V_{CE} "Flashover"	1500	1650	1750	V
I_C "Flashover"	10	10	10	A

Temperature

T_{stg} range	-65 to +115	$^\circ\text{C}$
T_j (operating) max.	115	$^\circ\text{C}$

THERMAL CHARACTERISTIC

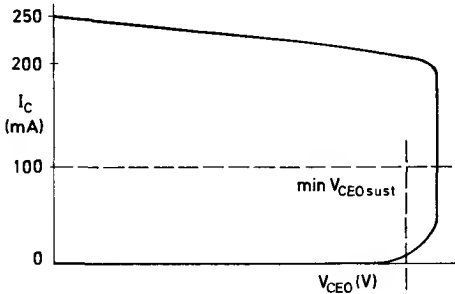
$R_{th(j-mb)}$ max.	1.6	$^\circ\text{C/W}$
$R_{th(mb-h)}$ with mica washer 56336B	1.0	$^\circ\text{C/W}$

Note 1

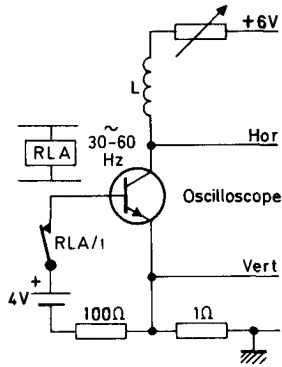
Turn off-current in line deflection circuits.

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$ unless otherwise stated)

		BU207	BU208	BU209	
I_{CES} max.	Collector cut-off current ($V_{\text{BE}} = 0$; $V_{\text{CE}} = V_{\text{CESM}}$ max)	1.0	1.0	1.0	mA
h_{FE} min.	Static forward current transfer ratio ($I_{\text{C}} = 4.5\text{A}$; $V_{\text{CE}} = 5\text{V}$) ($I_{\text{C}} = 3.0\text{A}$; $V_{\text{CE}} = 5\text{V}$)	2.25	2.25	- 2.25	
$+V_{\text{EBO}}$	Emitter-base voltage ($I_{\text{C}} = 0$; $I_{\text{E}} = 10\text{mA}$) min. ($I_{\text{C}} = 0$; $I_{\text{E}} = 100\text{mA}$) typ.	5 7	5 7	5 7	V V
$V_{\text{CE(sat)}}$ max.	Collector-emitter saturation voltage ($I_{\text{C}} = 4.5\text{A}$; $I_{\text{B}} = 2\text{A}$) ($I_{\text{C}} = 3\text{A}$; $I_{\text{B}} = 1.3\text{A}$)	5 -	5 -	- 5	V V
$V_{\text{BE(sat)}}$ max.	Base-emitter saturation voltage ($I_{\text{C}} = 4.5\text{A}$; $I_{\text{B}} = 2\text{A}$) ($I_{\text{C}} = 3\text{A}$; $I_{\text{B}} = 1.3\text{A}$)	1.5 -	1.5 -	- 1.5	V V
$V_{\text{CEO(sust)}}$	Collector-emitter sustaining voltage $I_{\text{B}} = 0$; $I_{\text{C}} = 100\text{mA}$; $L = 25\text{mH}$	600	700	800	V



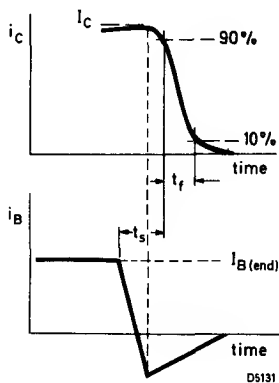
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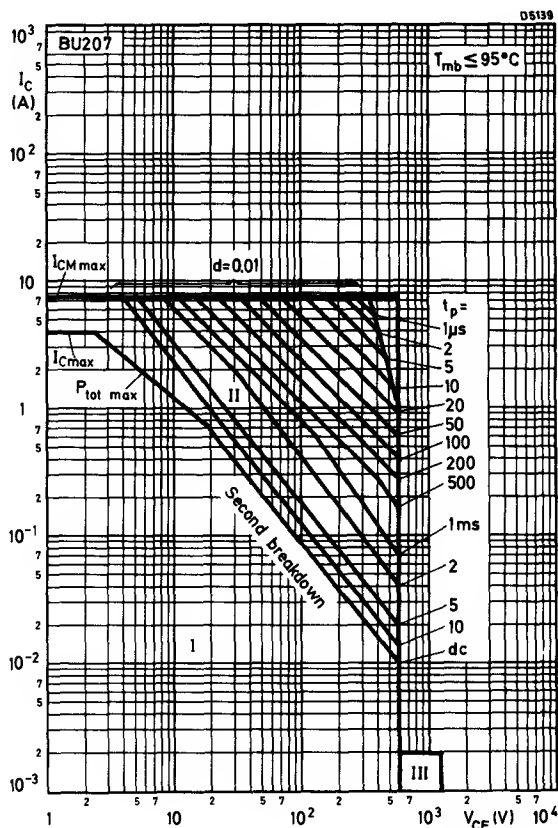


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ELECTRICAL CHARACTERISTICS (cont)

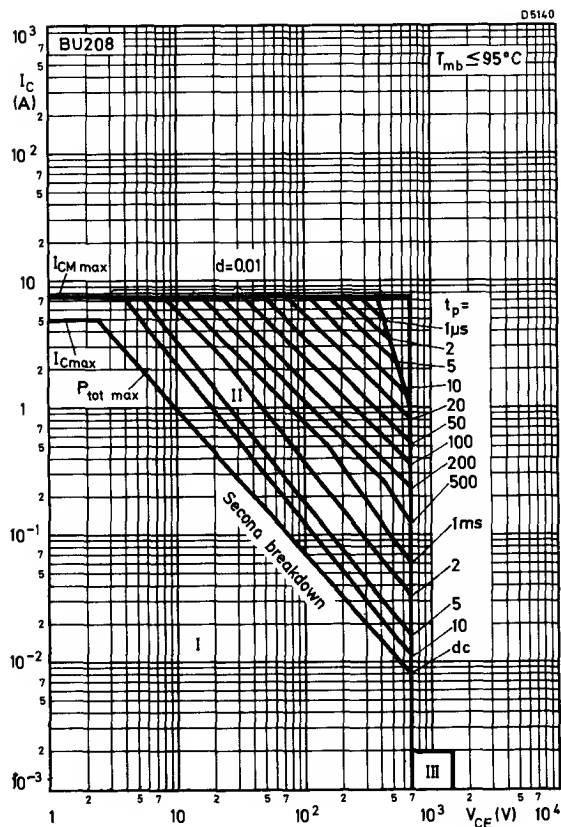
		BU207	BU208	BU209	
f_T (typ)	Transition frequency ($f = 5\text{MHz}$; $I_C = 0.1\text{A}$, $V_{CE} = 5\text{V}$)	7	7	7	MHz
C_{Tc} (typ)	Collector capacitance ($f = 1\text{MHz}$; $I_E = I_e = 0$; $V_{CB} = 10\text{V}$)	125	125	125	pF
Switching times (in line deflection circuit) ($L_B = 10\mu\text{H}$)					
t_f (typ)	Fall time				
	$I_C = 4.5\text{A}$; $I_{B(\text{end})} = 1.8\text{A}$	0.9	0.7	-	μs
	$I_C = 3.0\text{A}$; $I_{B(\text{end})} = 1.3\text{A}$	-	-	0.7	μs
t_s (typ)	Storage time				
	$I_C = 4.5\text{A}$; $I_{B(\text{end})} = 1.8\text{A}$	10	10	-	μs
	$I_C = 3.0\text{A}$; $I_{B(\text{end})} = 1.3\text{A}$	-	-	10	μs





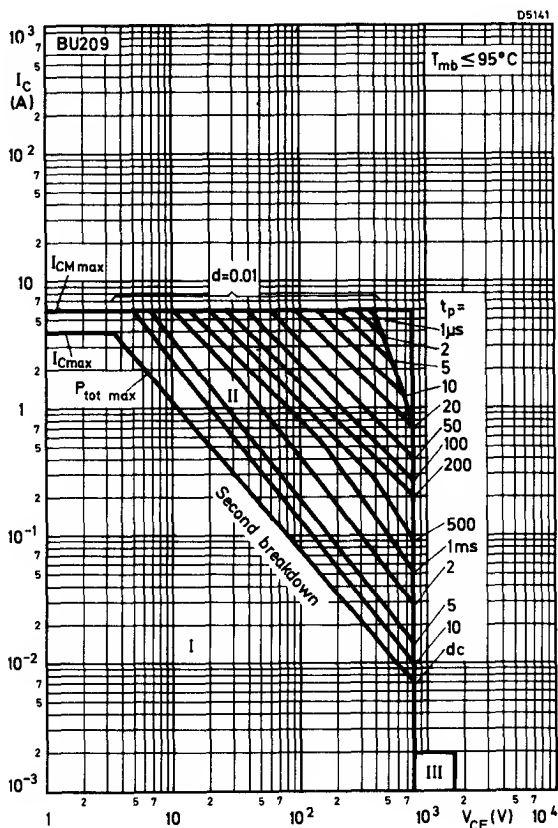
Safe Operating Area with the transistor forward biased.

- I Region of permissible d. c. operation.
- II Permissible extension for repetitive pulse operation.
- III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu\text{s}$; $\delta \leq 0.25$.



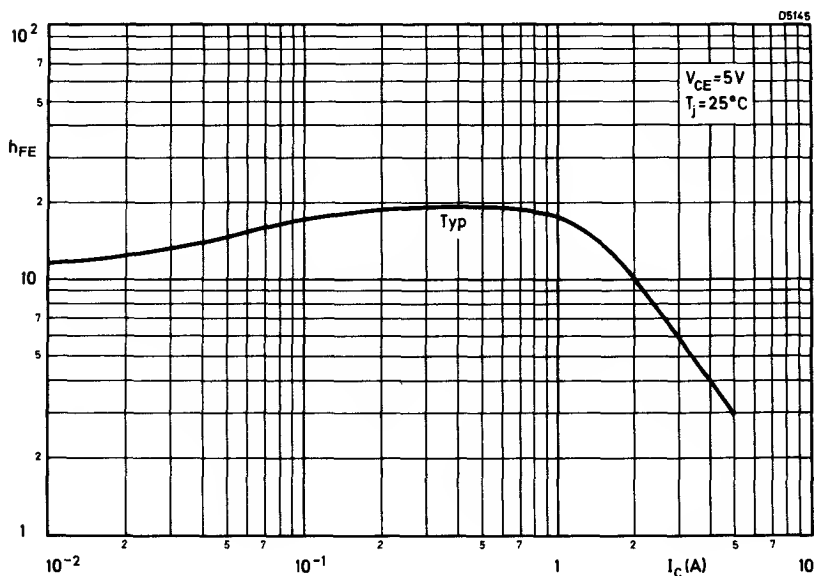
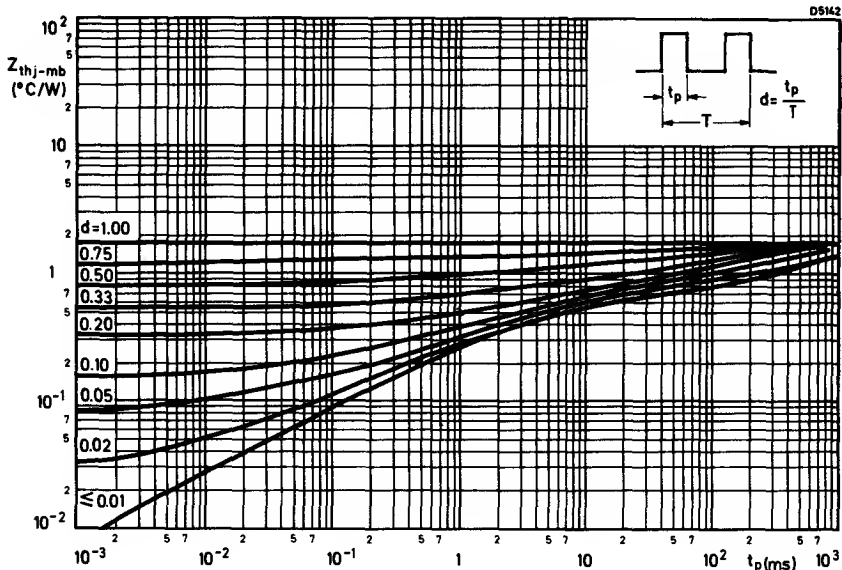
Safe Operating Area with the transistor forward biased.

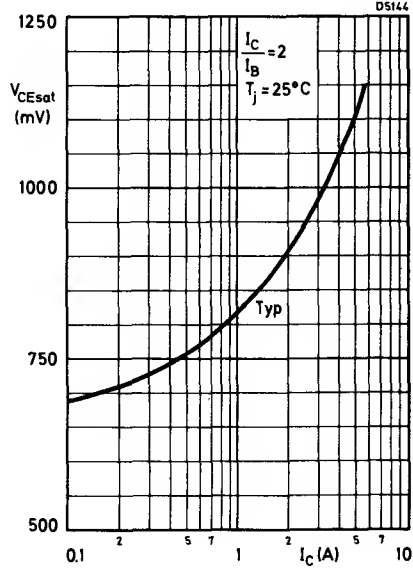
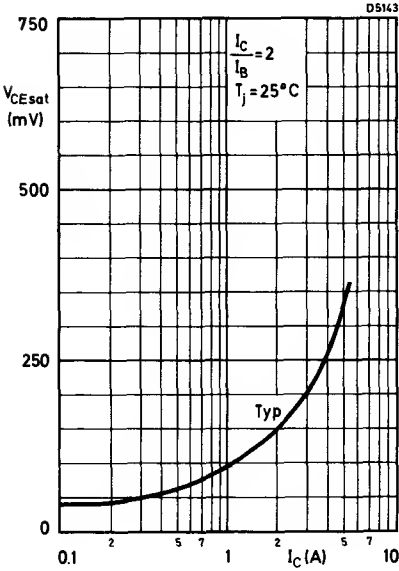
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Safe Operating Area with the transistor forward biased.

- I Region of permissible d. c. operation.
- II Permissible extension for repetitive pulse operation.
- III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu\text{s}$; $\delta \leq 0.25$.





QUICK REFERENCE DATA

Power junction transistors of the p-n-p alloy type intended for use in medium and high voltage and high current switching applications. Matched pairs of each type are available under the type number 2-OC

	OC28	OC29	OC35	OC36	
V_{CB} max. ($I_E = 0A$)	-80	-60	-60	-80	V
V_{CE} max. ($I_E = 0.5A$)	-60	-48	-48	-60	V
V_{CE} max. ($I_E = 6.0A$)	-60	-32	-32	-32	V
h_{FE} ($I_C = 1.0A$)	20-55	45-130	25-75	30-110	

Unless otherwise shown, data is applicable to all types

ABSOLUTE MAXIMUM RATINGS

The equipment designer must ensure that no transistor exceeds these ratings. In arriving at the actual operating conditions, variations in supply voltages, component tolerances and ambient temperatures must also be taken into account.

Collector voltage

	OC28	OC29	OC35	OC36	
V_{CB} max. ($I_E = 0A$)	-80	-60	-60	-80	V
V_{CE} max. ($I_E = 0.5A$)	-60	-48	-48	-60	V
V_{CE} max. ($I_E = 6.0A$)	-60	-32	-32	-32	V

Collector current

I_{CM} max.	10	A
$\dagger I_{C(AV)}$ max.	8.0	A

Emitter current

I_{EM} max.	12	A
$\dagger I_{E(AV)}$ max.	9.0	A

Reverse emitter-base voltage

V_{EB} max. ($I_C = 0A$)	-40	-20	-20	-40	V
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Base current

I_{BM} max.	2.0	A
$\dagger I_{B(AV)}$ max.	1.0	A

Total Dissipation at $T_{case} \leq 45^\circ C$

30 W

$T_{case} > 45^\circ C$

$$P_{tot} \text{ max.} = \frac{T_j \text{ max.} - T_{case}}{\theta_j - case}$$

\dagger Averaged over any 20ms period.

Mullard

Series

Temperature ratings

T_{stg} max.	75	°C
T_{stg} min.	-55	°C
T_j max. (Continuous operation)	90	°C
$\ddagger T_j$ max. (Intermittent operation total duration 200 hours)	100	°C
θ_{j-case} max.	1.5	°C/W
$\theta_{case-heat\ sink}$ max. (when mounted with metal washer 0.127mm thick and with mica washer)	0.5	°C/W

\ddagger Likelihood of full performance of a circuit at this temperature is also dependent on the type of application.

CHARACTERISTICS at $T_{case} = 25^\circ\text{C}$

Common base

		Typical production spread			
		Min.	Typ.	Max.	
Collector leakage current	I_{CBO}				
($V_{CB} = -500\text{mV}$, $I_E = 0\text{mA}$)		—	—	100	μA
($V_{CB} = -14\text{V}$, $I_E = 0\text{mA}$, $T_{case} = 100^\circ\text{C}$)		—	—	20	mA
($V_{CB} = -60\text{V}$, $I_E = 0\text{mA}$, $T_{case} = 100^\circ\text{C}$)	OC29, OC35	—	8.5	30	mA
($V_{CB} = -80\text{V}$, $I_E = 0\text{mA}$, $T_{case} = 100^\circ\text{C}$)	OC28, OC36	—	12	30	mA
Emitter cut-off voltage					
($V_{CB} = -48\text{V}$, $I_E = 0\text{mA}$, $T_{case} = 100^\circ\text{C}$)	V_{EB}	—	—	-500	mV

Common emitter

Collector knee voltage at $I_C = 6\text{A}$ (see Fig. 1)	$V_{CE(knee)}$	—	-0.5	-1.0	V
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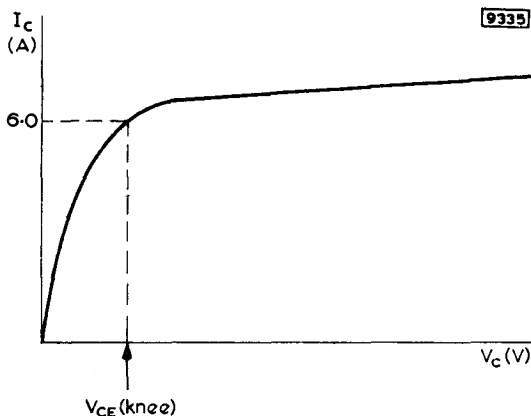


Fig. 1

		OC28		OC29		OC35		OC36	
Base current	I_B	min.	max.	min.	max.	min.	max.	min.	max.
($V_{CB} = 0V, I_E = 1A$)		17.5	50	7.2	21.5	13	38	9	33 mA
($V_{CB} = 0V, I_E = 6A$)		190	375	73	165	130	285	90	285 mA
Base input voltage	V_{BE}								
($V_{CB} = 0V, I_E = 1A$)		←-----800-----→ mV							
($V_{CB} = 0V, I_E = 6A$)		-0.6	-1.6	—	-1.6	-0.4	-1.4	—	-1.6 V
Current amplification factor	h_{FE}								
($V_{CE} = -14V, I_C = 30mA$)		20	—	—	—	—	—	—	—
($V_{CE} = -1V, I_C = 1A$)		20	55	45	130	25	75	30	110
($V_{CE} = -1V, I_C = 6A$)		15	30	35	80	20	45	20	65

BASIC PARAMETERS

Cut-off frequency

($V_{CB} = -6V, I_E = 300mA$)	f_{hfb}	—	250	—	kc/s
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Collector depletion capacitance

($V_{CB} = -12V, I_E = 0mA$)	c_{tc}	—	160	—	pF
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Emitter depletion capacitance

($V_{EB} = -6V, I_E = 0mA$)	c_{te}	—	165	—	pF
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Time constant, current feed

($V_{CE} = -4V, I_{CM} = 1A$)	$\frac{\beta}{\omega I}$	—	45	70	μs
($V_{CE} = -4V, I_{CM} = 6A$)		—	30	50	μs

Desaturation time constant

($V_{CE} = 0V, I_{BM} = 50mA$)	τ_s	—	30	50	μs
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OC28

Series

JUNCTION TRANSISTORS

Typical operation in on-off power switching circuit

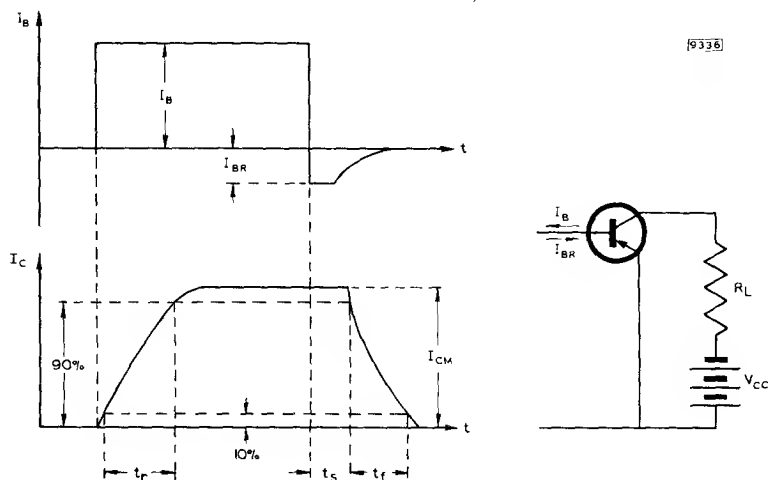


Fig. 2

D.C. supply voltage	V_{CC}	14		28		V
Load resistance	R_L	14	2.3	28	4.7	Ω
peak collector current	I_{CM}	1.0		6.0		A
		OC29 OC35		OC28 OC36		
'Turn On' base current	I_B	35	55	260	400	mA
'Reverse' base current	I_{BR}	8.7	13.7	65	100	mA
Switching times						
Rise time	t_r	20	20	20	20	μs
Storage time	t_s	15	15	15	15	μs
Fall time	t_f	40	35	40	35	μs

$$\text{Rise time } t_r = \frac{\beta}{\omega 1} \log_e \frac{h_{FE} |I_B|}{|I_B| - |I_{CM}|}$$

$$\text{Fall time } t_f = \frac{\beta}{\omega 1} \log_e \left[1 + \frac{|I_{CM}|}{h_{FE} |I_{BR}|} \right]$$

$$\text{Storage time } t_s = \tau_s \log_e \frac{|I_B| + |I_{BR}|}{\frac{|I_{CM}|}{h_{FE}} + |I_{BR}|}$$

Mullard

CHARACTERISTICS OF MATCHED PAIR(measured at $T_{\text{case}} = 25^{\circ}\text{C}$)

Ratio of the current amplification factors of the two transistors

at $V_{\text{CB}} = 0\text{V}$, $I_{\text{C}} = 300\text{mA}$ 1.2 : 1 $V_{\text{CB}} = 0\text{V}$, $I_{\text{C}} = 6\text{A}$ 1.2 : 1

Difference between the base-emitter voltages of the two transistors

at $V_{\text{CB}} = -14\text{V}$, $I_{\text{C}} = 30\text{mA}$ < 35 mV $V_{\text{CB}} = 0\text{V}$, $I_{\text{C}} = 6\text{A}$ < 300 mV**OPERATING NOTES****1. Dissipation and heat sink considerations**The maximum total dissipation $P_{\text{tot max.}} = (V_{\text{CE}} \times I_{\text{C}}) + (V_{\text{BE}} \times I_{\text{B}})$, is given by the relationship:—

$$P_{\text{tot max.}} = \frac{T_j \text{ max.} - T_{\text{amb}}}{\theta_m + \theta_i + \theta_h}$$

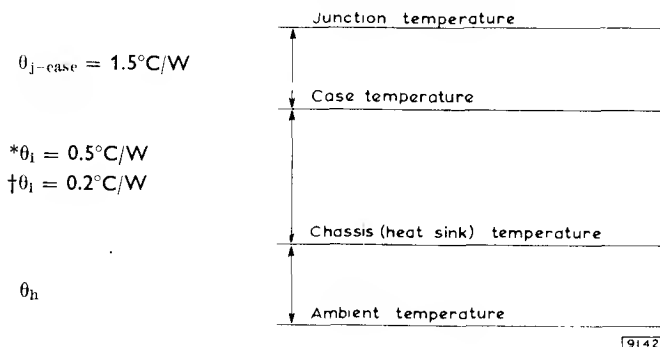
Where $\theta_m + \theta_i + \theta_h$ is equal to $\theta_{j \text{ amb.}}$ The various components of $\theta_{j \text{ amb.}}$ are illustrated below:

Fig. 3

*When mounted with a metal washer 0.127mm thick and a mica washer, or with a mica washer only and silicone grease, $\theta_i = 0.5^{\circ}\text{C/W}$. This value applies when the transistor is bolted down evenly on a flat heat sink. The metal washer is advantageous in taking up any irregularities in the heat sink surfaces.

\dagger When mounted directly on the chassis with a thin film of silicone grease between the contacting surfaces, $\theta_i = 0.2^{\circ}\text{C/W}$. This value applies when the transistor is bolted down evenly on a flat heat sink.

θ_h depends on the cooling conditions under which the transistor is used, i.e., dimensions, position and surface conditions of heat sink, etc. An air-cooled heat sink (7in. \times 7in. \times 1/16in. blackened aluminium) will have a value of $\theta_h = 2.2^{\circ}\text{C/W}$.

Series

θ_{jh} can be determined for a given collector dissipation and ambient temperature by measuring the case temperature.

$$\theta_{jh} = \frac{T_{case} - T_{amb}}{P_{tot}} - \theta_{jc}^{\circ}C/W$$

The following example illustrates the temperatures which occur at various points on the transistor at $p_c = 10W$, $T_j = 90^{\circ}C$, $\theta_{jh} = 2.2^{\circ}C/W$.

T_j	$= 90^{\circ}C$
T_{case}	$= 90 - (10 \times 1.5) = 75^{\circ}C$
$T_{heat\ sink}$	$= 75 - (10 \times 0.5) = 70^{\circ}C$
T_{amb}	$= 70 - (10 \times 2.2) = 48^{\circ}C$

The suitability of any design can be checked by measuring, with a thermocouple, the case temperature of the transistor operating at the selected collector dissipation and maximum ambient temperature. The point defined by the case temperature and the total dissipation must lie within the shaded area shown on the graph on page C10. If the point lies outside the shaded area the design is inadmissible and the dissipation must be reduced or the heatsink improved. The selected total dissipation should be the maximum attained by any transistor in the design being checked.

2. Transistors may be soldered directly into the circuit but the heat conducted to the junction should be kept to a minimum by the use of a thermal shunt.
3. Transistors may be dip soldered at a solder temperature of $240^{\circ}C$ for a maximum of 10 seconds up to a point 2mm from the seal.
4. Care must be taken to ensure good thermal contact between the transistor and heat sink. Burrs or thickening at the edges of the four holes must be removed and the transistor bolted down on a plane surface.

MECHANICAL DATA

Dimensions – see page D8.

Average weight

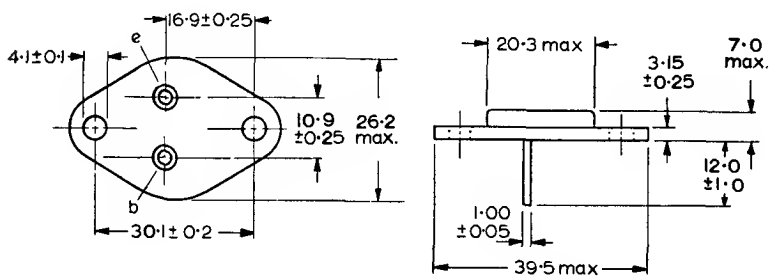
$\left\{ \begin{array}{l} 0.66 \text{ oz} \\ 18.6 \text{ g} \end{array} \right.$

ACCESSORIES

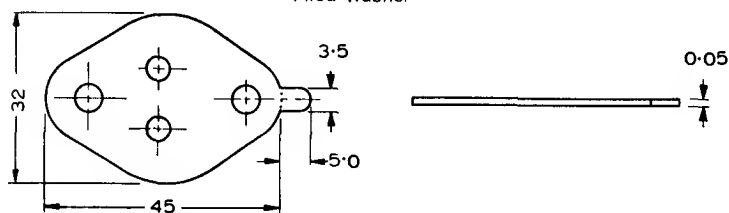
Accessories must be specifically ordered.

Accessory	Code No.	Notes
2 insulating bushes	56201a	Obtainable in packs for 10 or 100 transistors.
1 mica washer	56201b	
1 metal washer	56214	

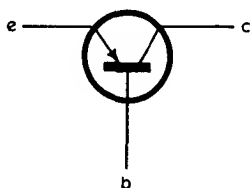
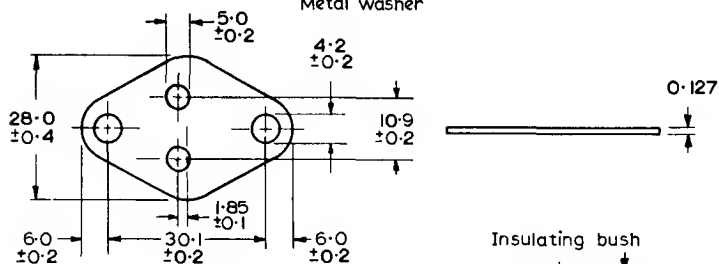
Transistor



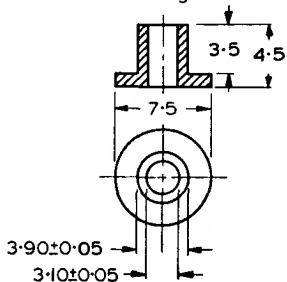
Mica washer



Metal washer

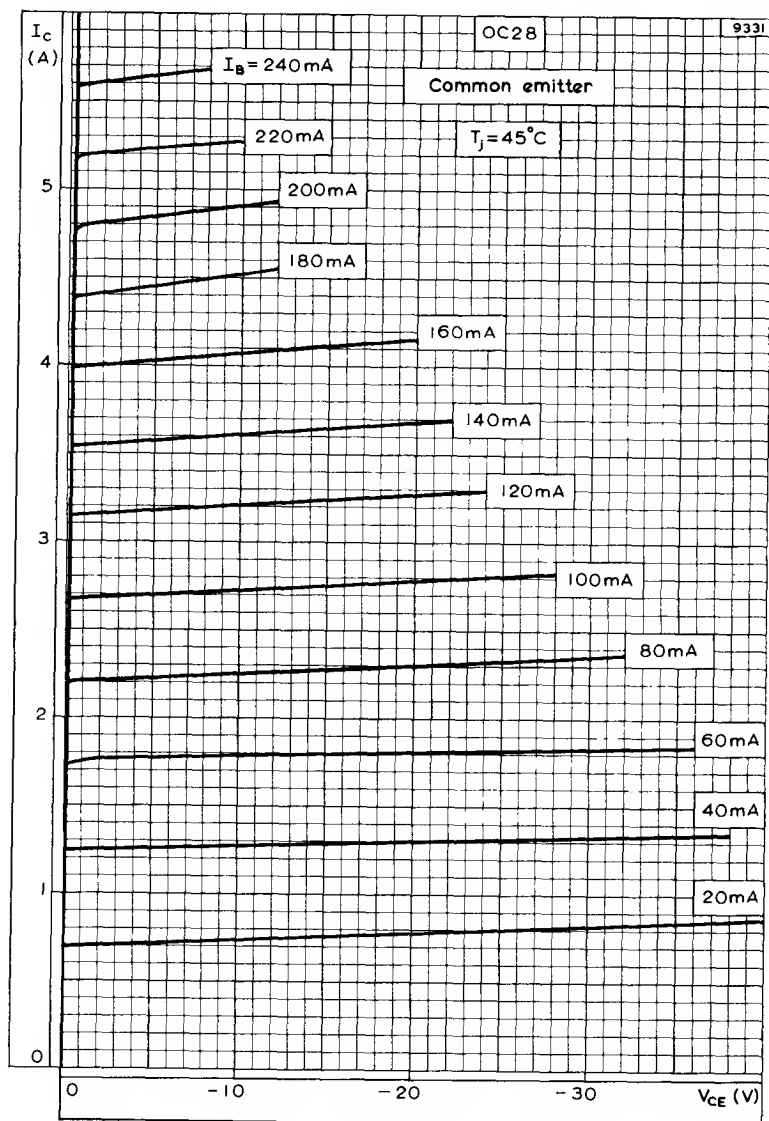


Insulating bush



All dimensions in mm

9484

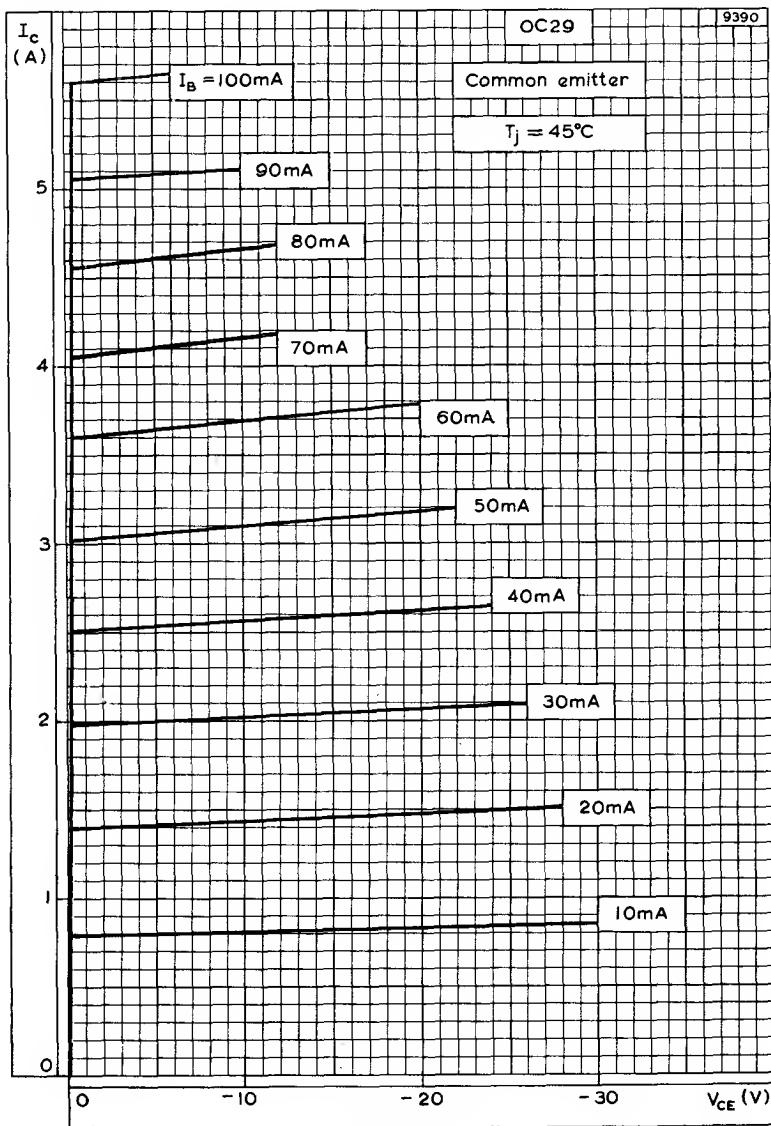


OUTPUT CHARACTERISTIC FOR OC28. COMMON EMITTER

OC28

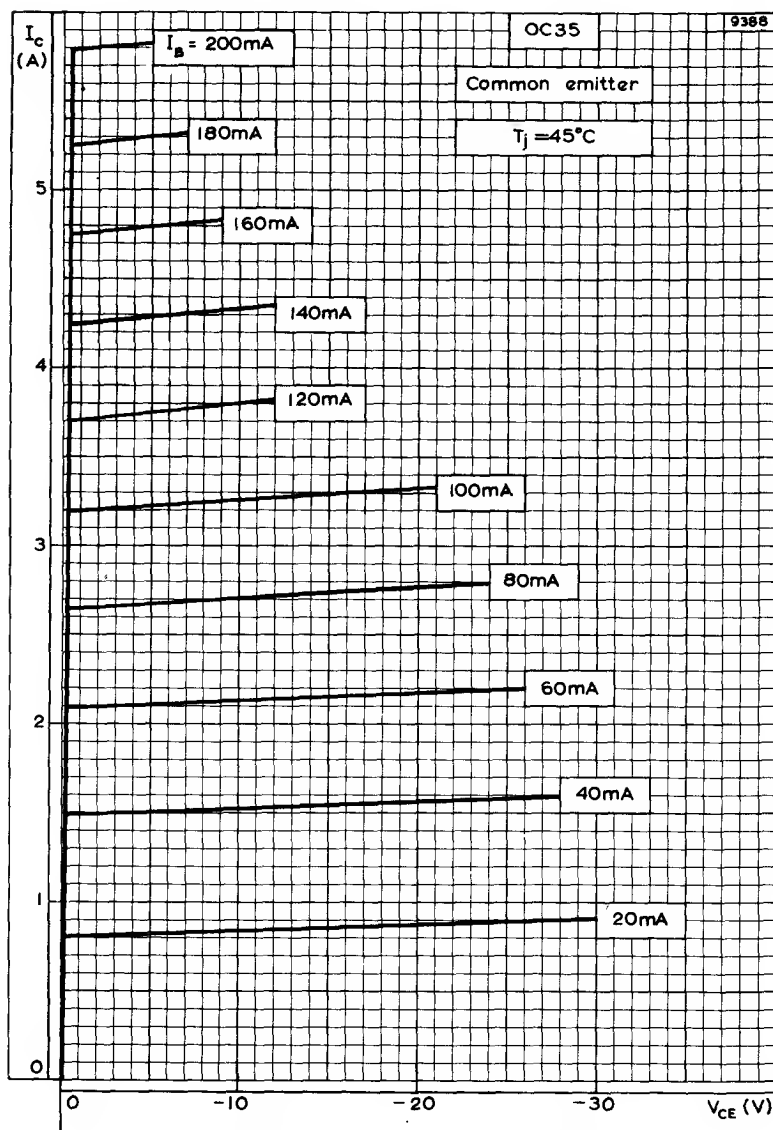
JUNCTION TRANSISTORS

Series



OUTPUT CHARACTERISTIC FOR OC29. COMMON EMITTER

Mullard

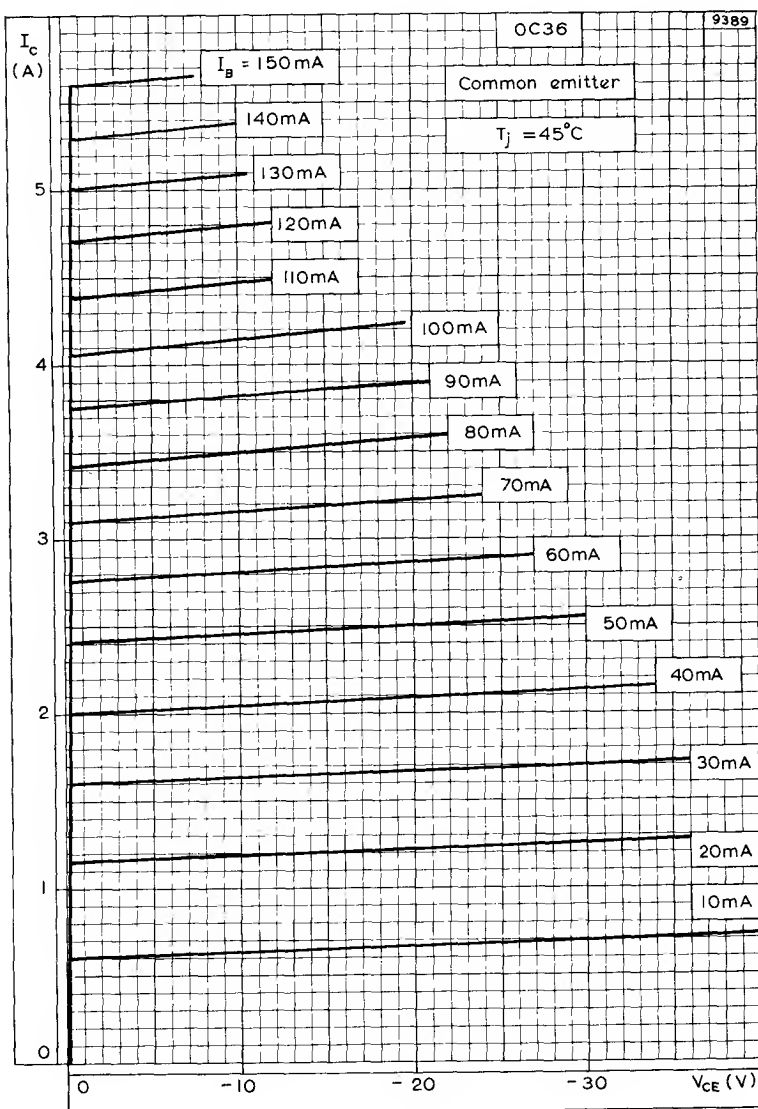


OUTPUT CHARACTERISTIC FOR OC35. COMMON EMITTER

OC28

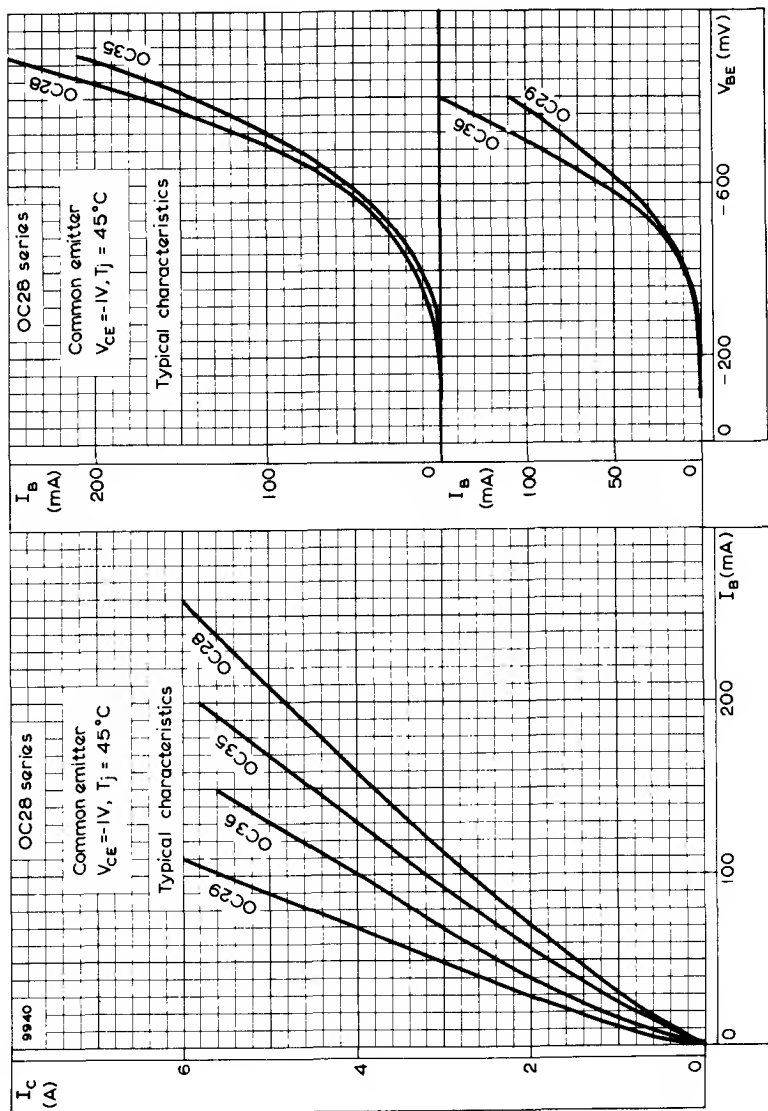
JUNCTION TRANSISTORS

Series

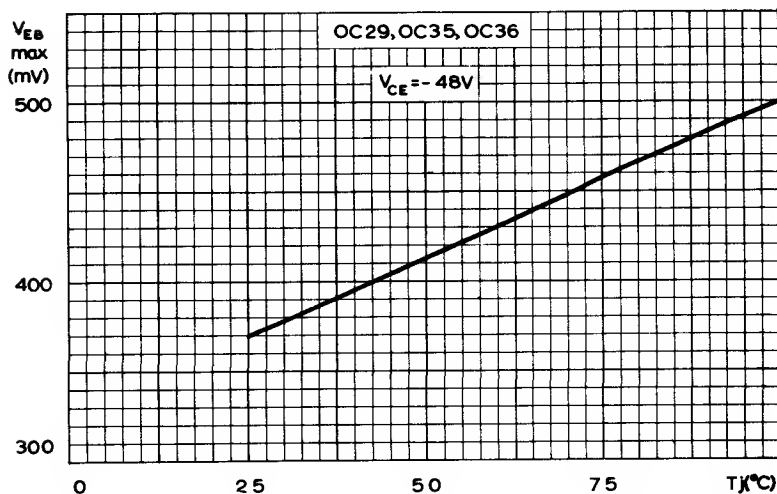
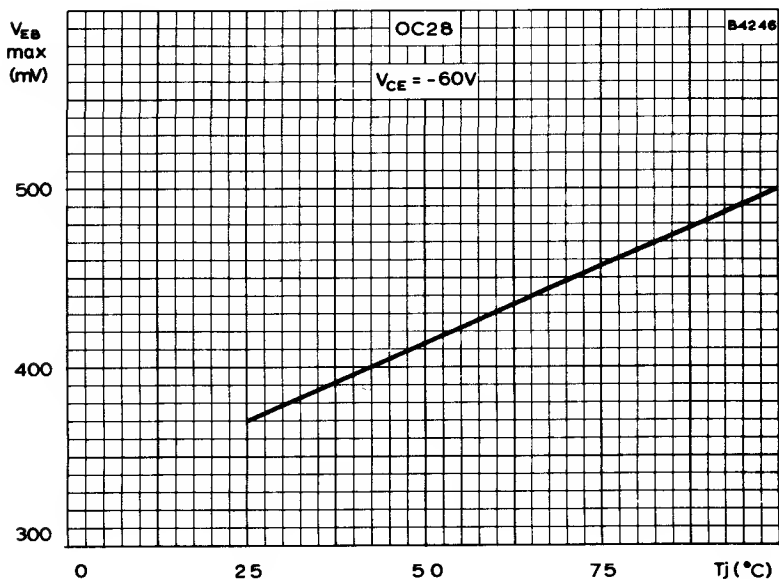


OUTPUT CHARACTERISTIC FOR OC36. COMMON EMITTER

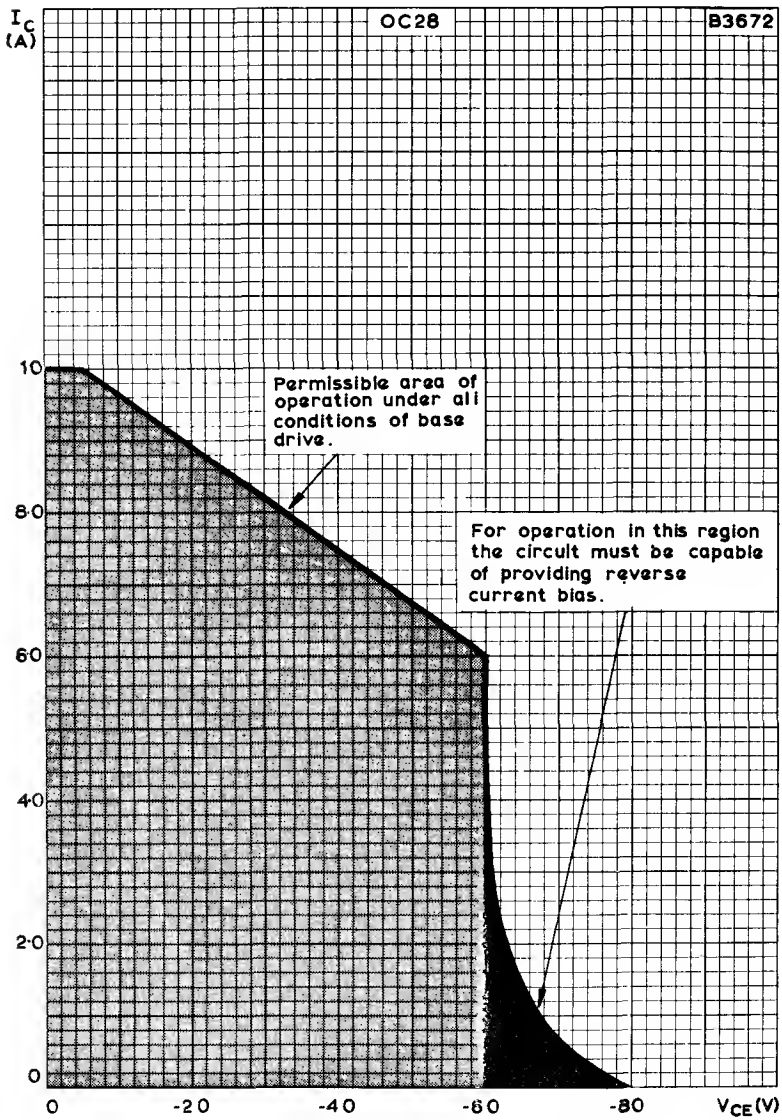
Mullard



TRANSFER AND INPUT CHARACTERISTICS. COMMON EMITTER



VARIAION OF MAXIMUM EMITTER-BASE CUT-OFF VOLTAGE WITH JUNCTION TEMPERATURE

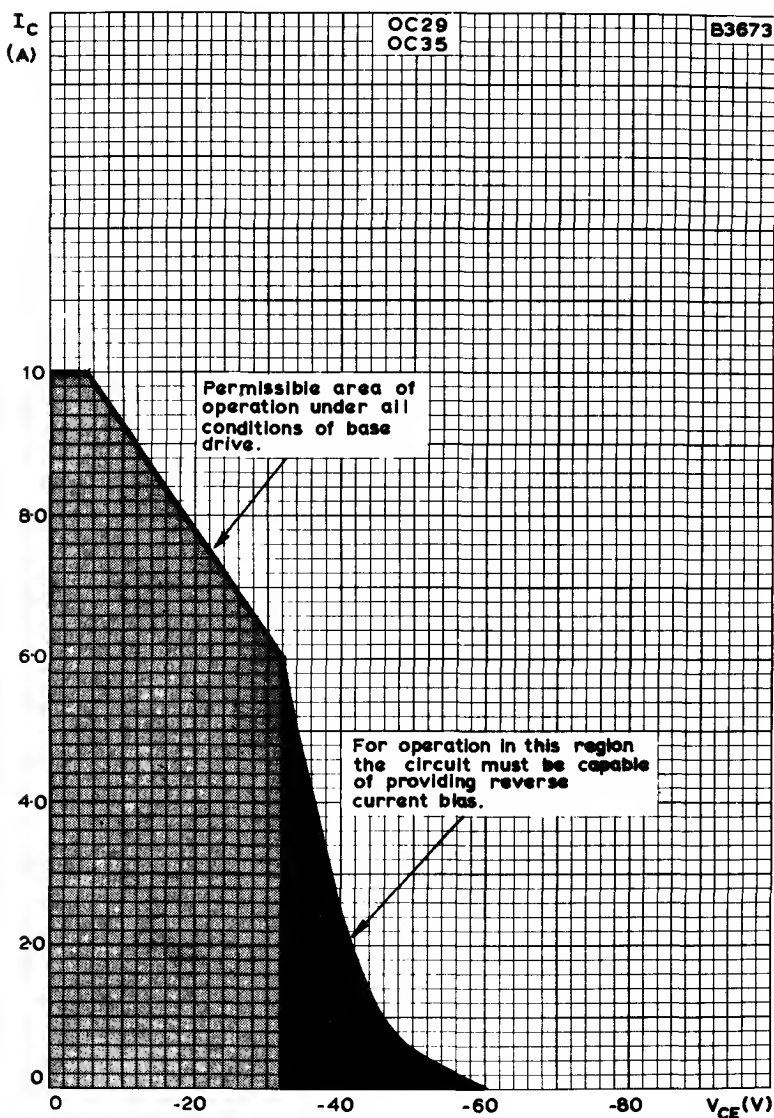


COLLECTOR CURRENT PLOTTED AGAINST ABSOLUTE MAXIMUM
COLLECTOR-EMITTER VOLTAGE. OC28

OC28

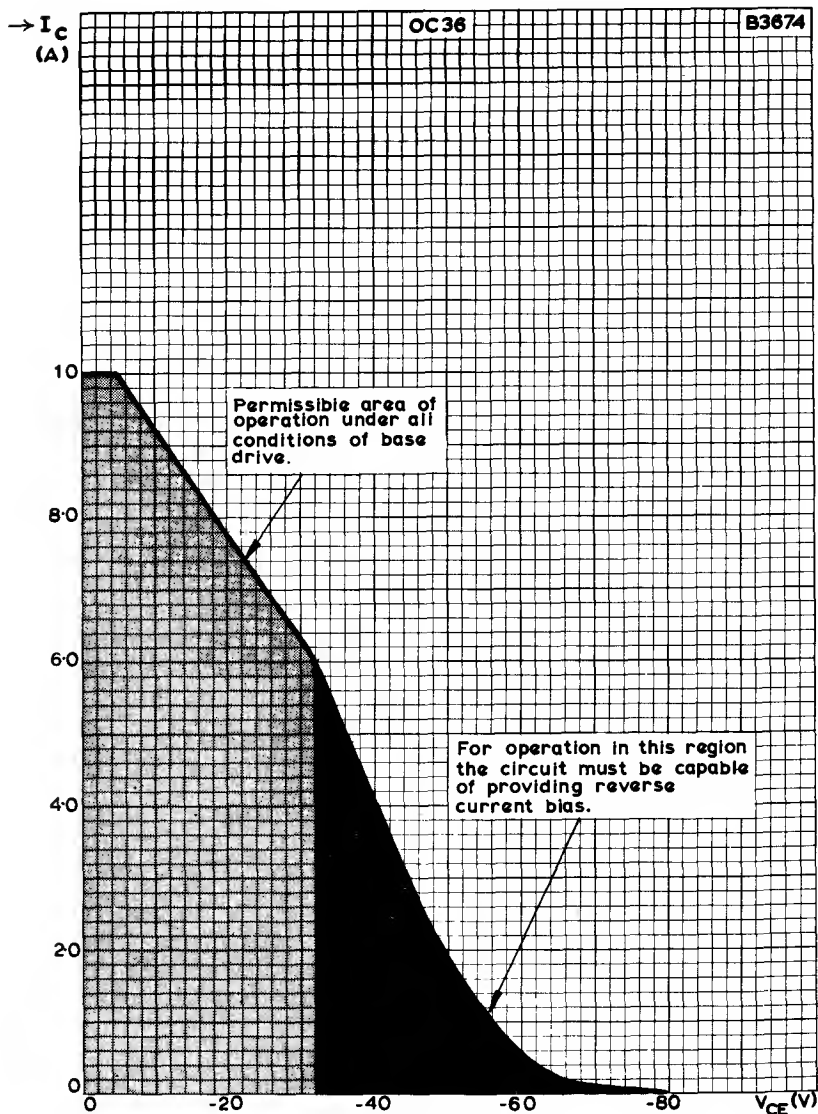
JUNCTION TRANSISTORS

Series



COLLECTOR CURRENT PLOTTED AGAINST ABSOLUTE MAXIMUM
COLLECTOR-EMITTER VOLTAGE. OC29, OC35

Mullard

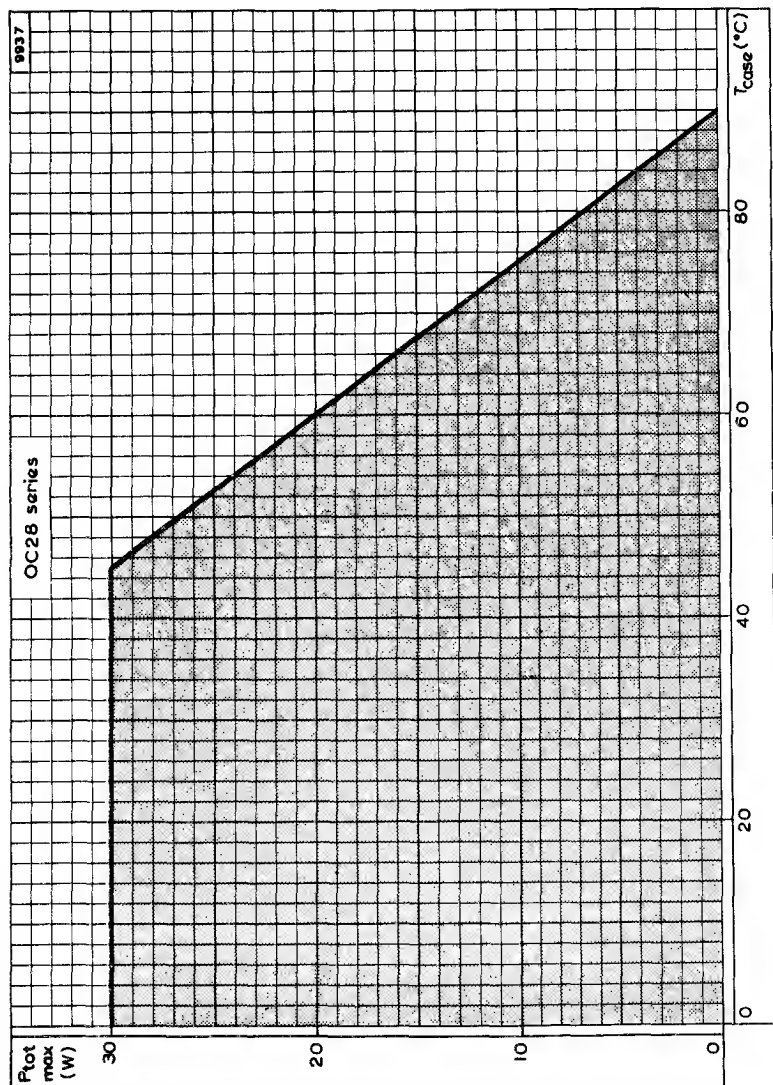


COLLECTOR CURRENT PLOTTED AGAINST ABSOLUTE MAXIMUM
COLLECTOR-EMITTER VOLTAGE. OC36

OC28

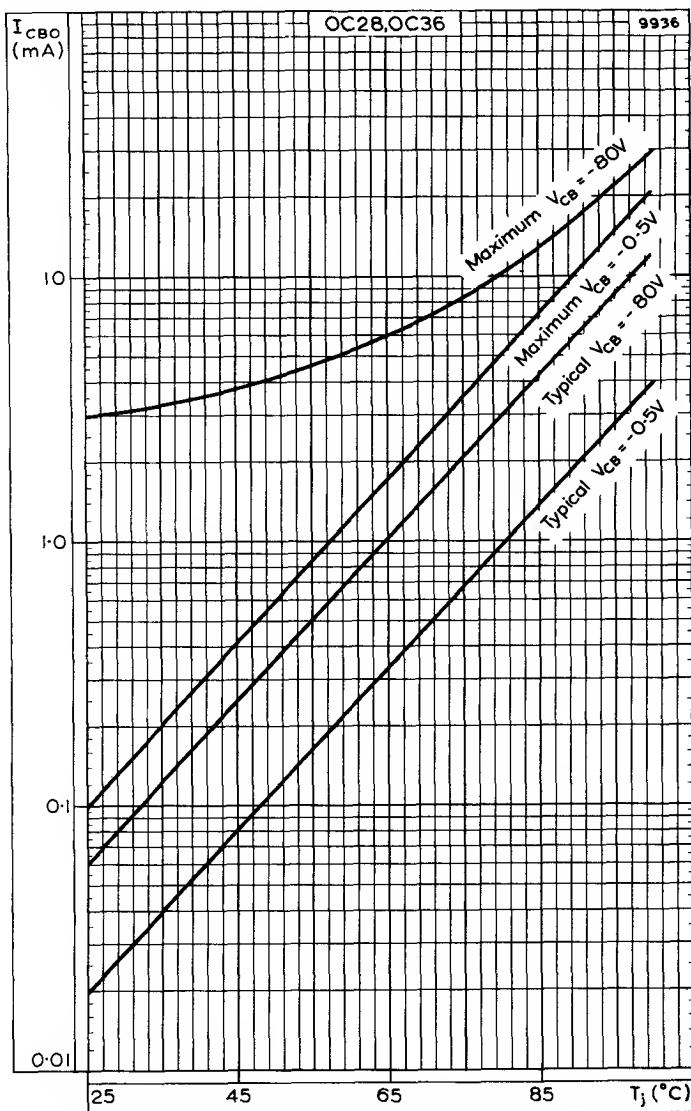
JUNCTION TRANSISTORS

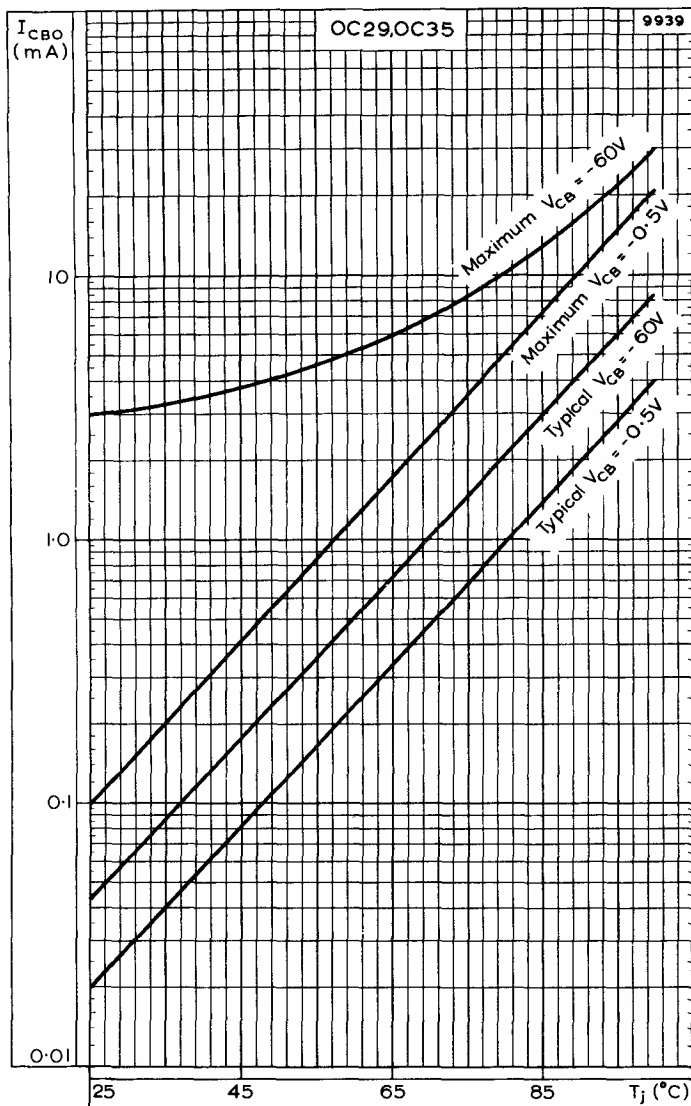
Series



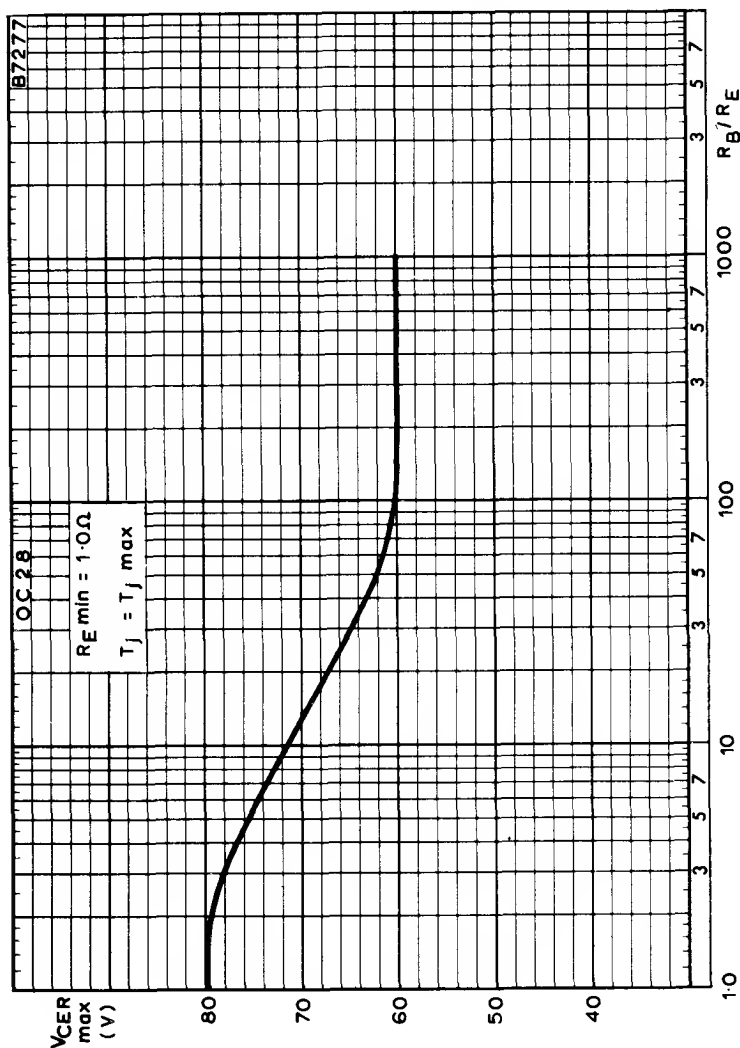
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST CASE TEMPERATURE

Mullard

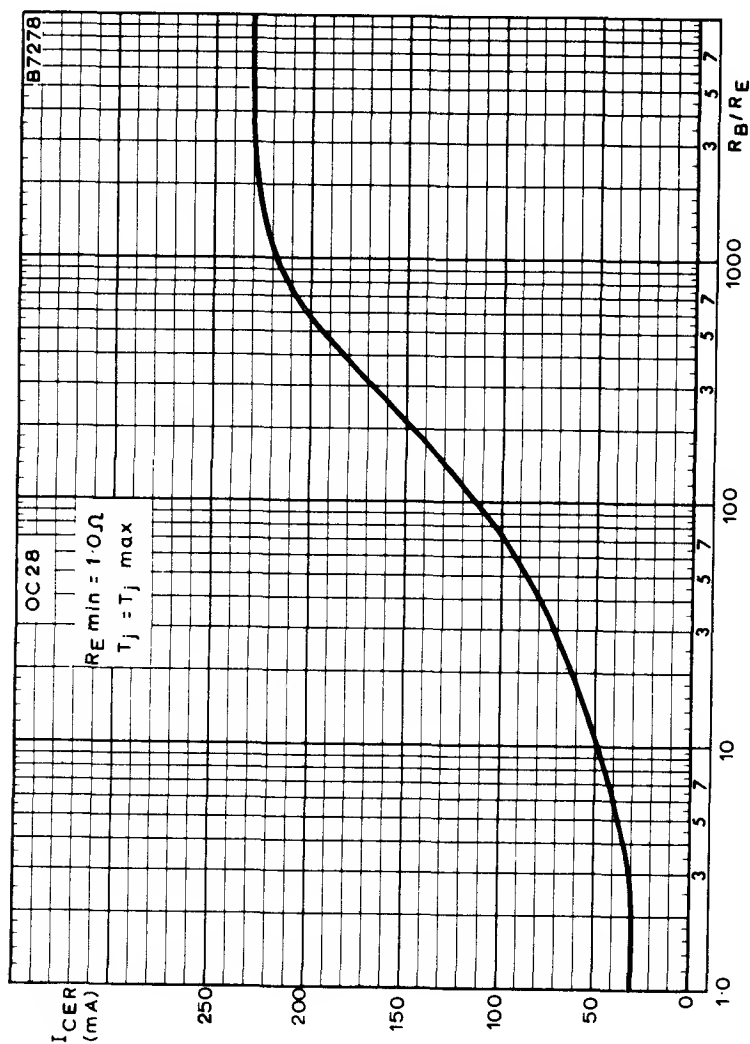
VARIATION OF I_{CB0} WITH JUNCTION TEMPERATURE. OC28, OC36



VARIATION OF I_{CBO} WITH JUNCTION TEMPERATURE. OC29, OC35



MAXIMUM PERMISSIBLE COLLECTOR-EMITTER VOLTAGE PLOTTED
AGAINST RATIO OF R_B/R_E



TYPICAL VARIATION OF I_{CER} WITH RATIO OF R_B/R_E

SILICON N-P-N PLANAR TRANSISTOR

2N1613

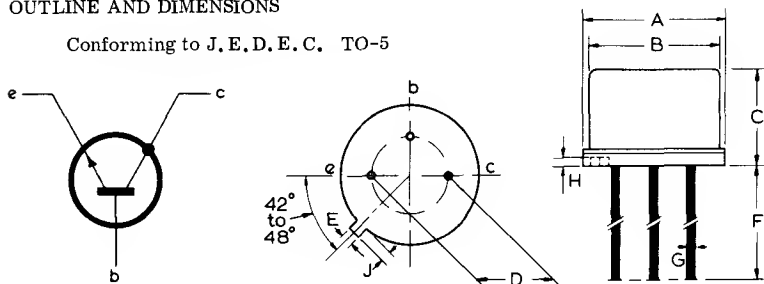
Silicon n-p-n double diffused planar transistor designed for a wide variety of applications including d. c. amplifiers, high speed switching and high speed amplifiers.

QUICK REFERENCE DATA

V_{CB} max. ($I_E = 0$)	+75	V
V_{CE} max.	+30	V
I_C max.	500	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)	800	mW
h_{FE} ($I_{CM} = 150\text{mA}$, $V_{CE} = +10\text{V}$)	40 - 120	
f_T typ. ($I_C = 50\text{mA}$, $V_{CE} = +10\text{V}$, $f = 20\text{Mc/s}$)	60	Mc/s

OUTLINE AND DIMENSIONS

Conforming to J. E. D. E. C. TO-5



B2390

Collector connected to envelope

	Millimetres				Millimetres		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	8.64	8.9	9.4	F	38	-	-
B	7.75	8.15	8.50	G	-	0.45	-
C	6.10	6.35	6.60	*H	-	0.4	-
D	-	5.08	-	J	0.74	0.85	1.01
E	0.71	0.79	0.86	*Thickness of locating tab.			

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\dagger V_{CB} \text{ max.}$	+75	V
$\dagger V_{CER} \text{ max. (} R_{BE} \leq 10\Omega \text{)}$	+50	V
$\dagger V_{EB} \text{ max.}$	+7.0	V
$\dagger V_{CEO} \text{ max. (} I_B = 0 \text{)}$	+30	V
$I_{CM} \text{ max.}$	500	mA
$\dagger P_{tot} \text{ max. } T_{case} = 25^{\circ}\text{C}$	3.0	W
$T_{case} = 100^{\circ}\text{C}$	1.7	W
$T_{amb} = 25^{\circ}\text{C}$	0.8	W

Thermal

$\dagger T_{stg} \text{ min.}$	-65	$^{\circ}\text{C}$
$T_{stg} \text{ max.}$	200*	$^{\circ}\text{C}$
$\dagger T_j \text{ (operating range)}$	-65 to +200	$^{\circ}\text{C}$

*See Soldering and Wiring Recommendation No. 4.

THERMAL CHARACTERISTIC

$\dagger R_{th(j-case)}$	58.3	deg C/W
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SILICON N-P-N PLANAR TRANSISTOR

2N1613

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Max.	
$\dagger I_{CBO}$	Collector cut-off current			
	$V_{CB} = 60\text{V}, I_E = 0$	-	10	nA
	$V_{CB} = 60\text{V}, I_E = 0,$ $T_{amb} = 150^{\circ}\text{C}$	-	10	μA
$\dagger I_{EBO}$	Emitter cut-off current			
	$V_{EB} = +5.0\text{V}, I_C = 0$	-	10	nA
$\dagger V_{BR(CBO)}$	Collector-base breakdown voltage			
	$I_C = 100\mu\text{A}$	+75	-	V
$\dagger V_{BR(EBO)}$	Emitter-base breakdown voltage			
	$I_E = 100\mu\text{A}, I_C = 0$	+7.0	-	V
$\dagger V_{CER(sat)}$	Collector-emitter voltage			
	$R_{BE} \leq 10\Omega, I_C = 10\text{mA}$ (See note 1)	+50	-	V
$\dagger V_{CE(sat)}$	Collector-emitter saturation voltage			
	$I_B = 15\text{mA}, I_C = 150\text{mA}$ (See note 1)	-	+1.5	V
$\dagger V_{BE(sat)}$	Base-emitter saturation voltage			
	$I_B = 15\text{mA}, I_C = 150\text{mA}$ (see note 1)	-	+1.3	V
$\dagger h_{FE}$	Large signal forward current transfer ratio			
	$I_C = 150\text{mA}, V_{CE} = 10\text{V}$ (See note 1)	40	120	
	$I_C = 500\text{mA}, V_{CE} = 10\text{V}$ (See note 1)	20	-	
	$I_C = 10\text{mA}, V_{CE} = 10\text{V}$ (See note 1)	35	-	
	$I_C = 10\text{mA}, V_{CE} = 10\text{V},$ $T_{amb} = -55^{\circ}\text{C},$ (See note 1)	20	-	

Mullard

		Min.	Max.	
$t_d + t_r + t_f$	Switching time $I_C = 50\text{mA}$, $V_{BE(\text{on})} = +1.0\text{V}$, $V_{BE(\text{off})} = +1.0\text{V}$, (See Fig. 1)	-	30	ns
$\dagger h_{fe}$	Small signal forward current transfer ratio $I_C = 1.0\text{mA}$, $V_{CE} = 5.0\text{V}$ $I_C = 5.0\text{mA}$, $V_{CE} = 10\text{V}$	30 35	100 150	
$\dagger h_{ib}$	Input impedance $I_C = 1.0\text{mA}$, $V_{CB} = 5.0\text{V}$ $I_C = 5.0\text{mA}$, $V_{CB} = 10\text{V}$	24 1.0	35 8.0	Ω Ω
$\dagger h_{rb}$	Voltage feedback ratio $I_C = 1.0\text{mA}$, $V_{CB} = 5.0\text{V}$ $I_C = 5.0\text{mA}$, $V_{CB} = 10\text{V}$	-	3.0	$\times 10^{-4}$ $\times 10^{-4}$
$\dagger h_{ob}$	Output admittance $I_C = 1.0\text{mA}$, $V_{CB} = 5.0\text{V}$ $I_C = 5.0\text{mA}$, $V_{CB} = 10\text{V}$	0.1 0.1	0.5 1.0	μmhos μmhos
$\dagger h_{fe}$	High frequency current transfer ratio $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 20\text{Mc/s}$	3.0	-	
$\dagger c_{ob}$	Output capacitance $I_C = 0\text{mA}$, $V_{CB} = 10\text{V}$	-	25	pF
$\dagger c_{ib}$	Input capacitance $I_C = 0\text{mA}$, $V_{EB} = 0.5\text{V}$	-	80	pF
$\dagger \text{N.F.}$	Noise figure $I_C = 0.3\text{mA}$, $V_{CE} = 10\text{V}$, $f = 1000\text{c/s}$, $R_S = 510\Omega$, 1 cycle bandwidth	-	12	dB

\dagger J.E.D.E.C. Registered Data.

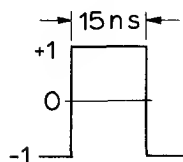
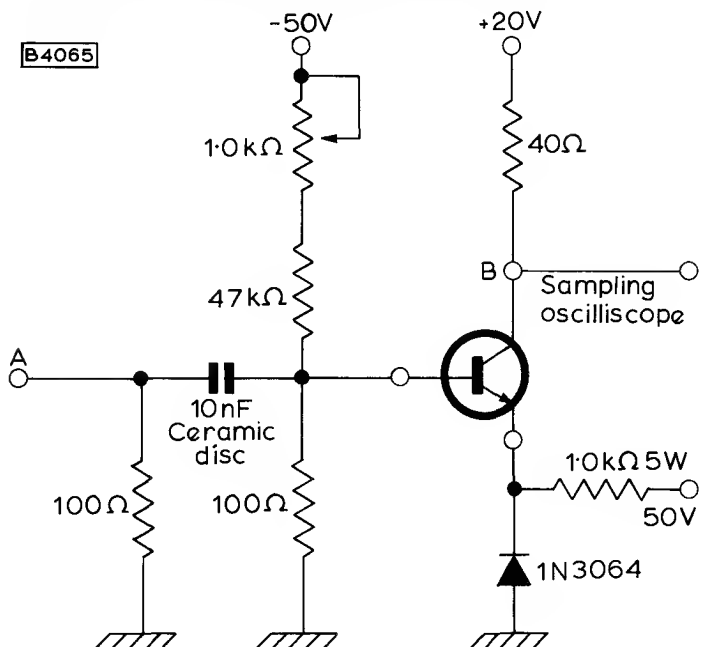
NOTE

1. Measured under pulsed conditions to prevent excessive dissipation
P.W. = 300 μs , duty cycle $\leq 1\%$.

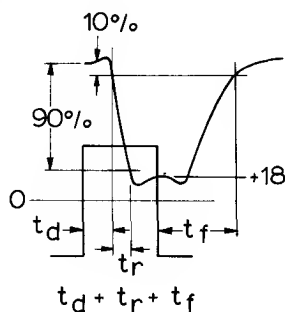
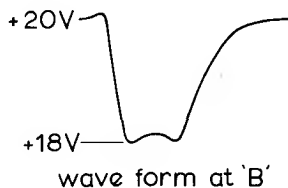
SOLDERING AND WIRING RECOMMENDATIONS

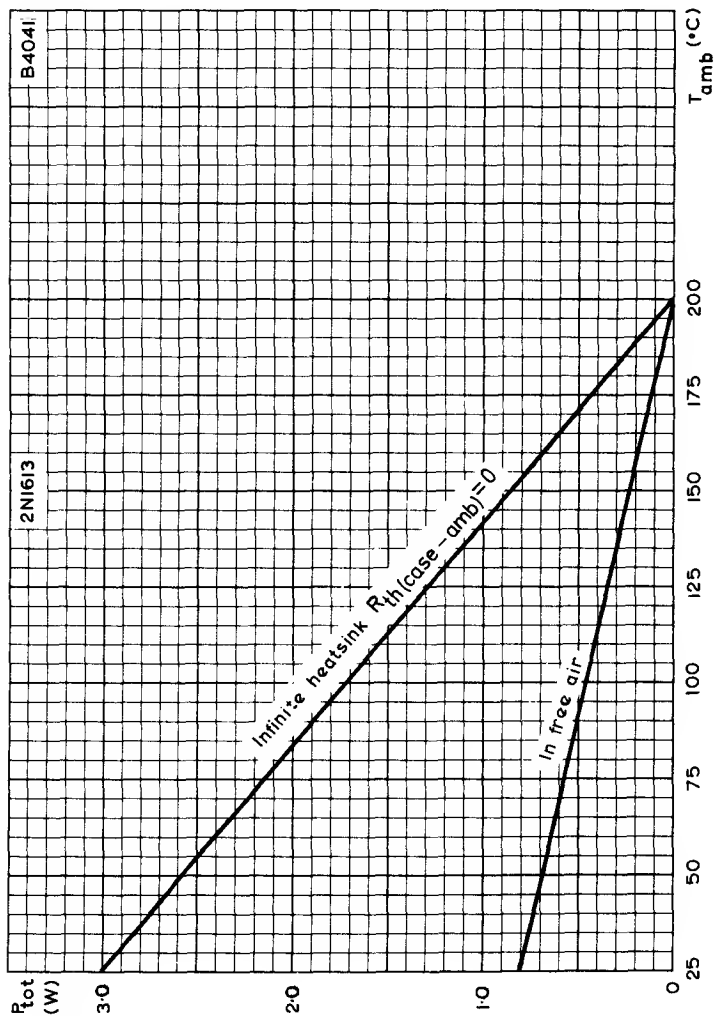
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. After storage at temperatures greater than 125°C it may be necessary to take precautions in order to ensure adequate solderability of the leads.

SWITCHING CHARACTERISTIC MEASUREMENT CIRCUIT

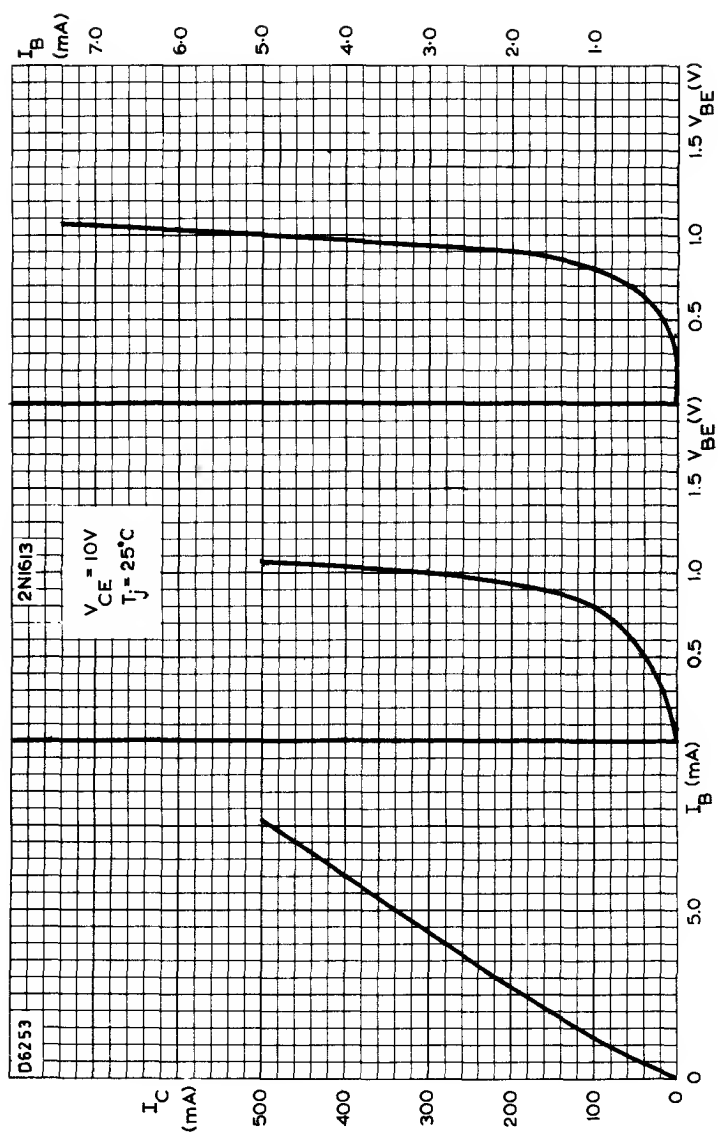


wave form at 'A'
from pulse generator
($< 1\text{ns}$ rise time)
($< 1\text{ns}$ fall time)

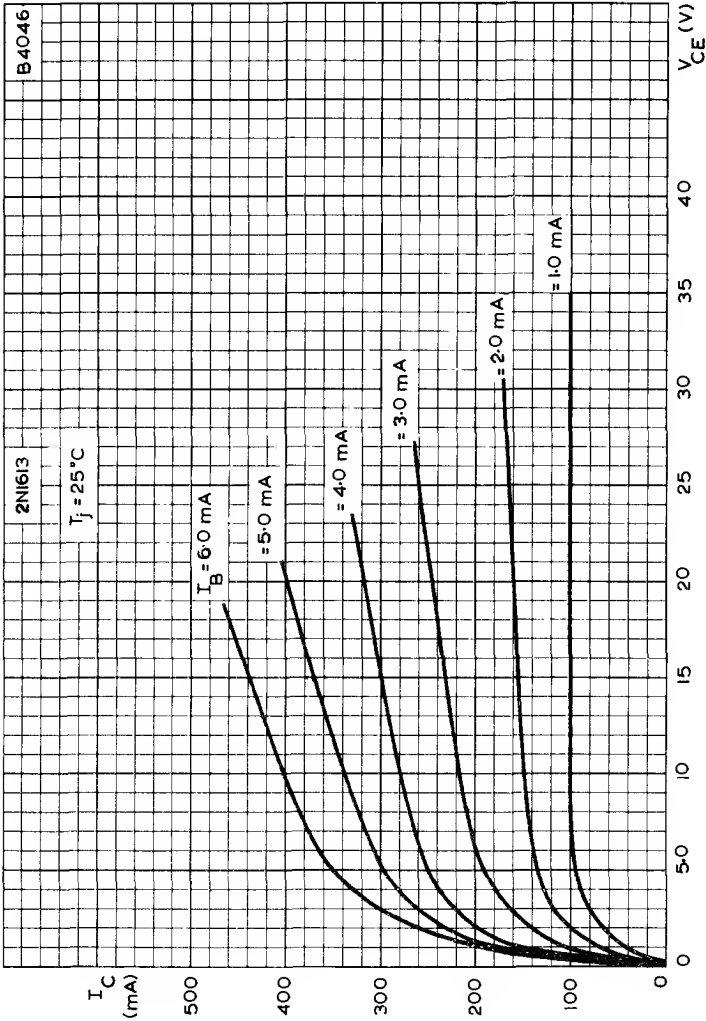




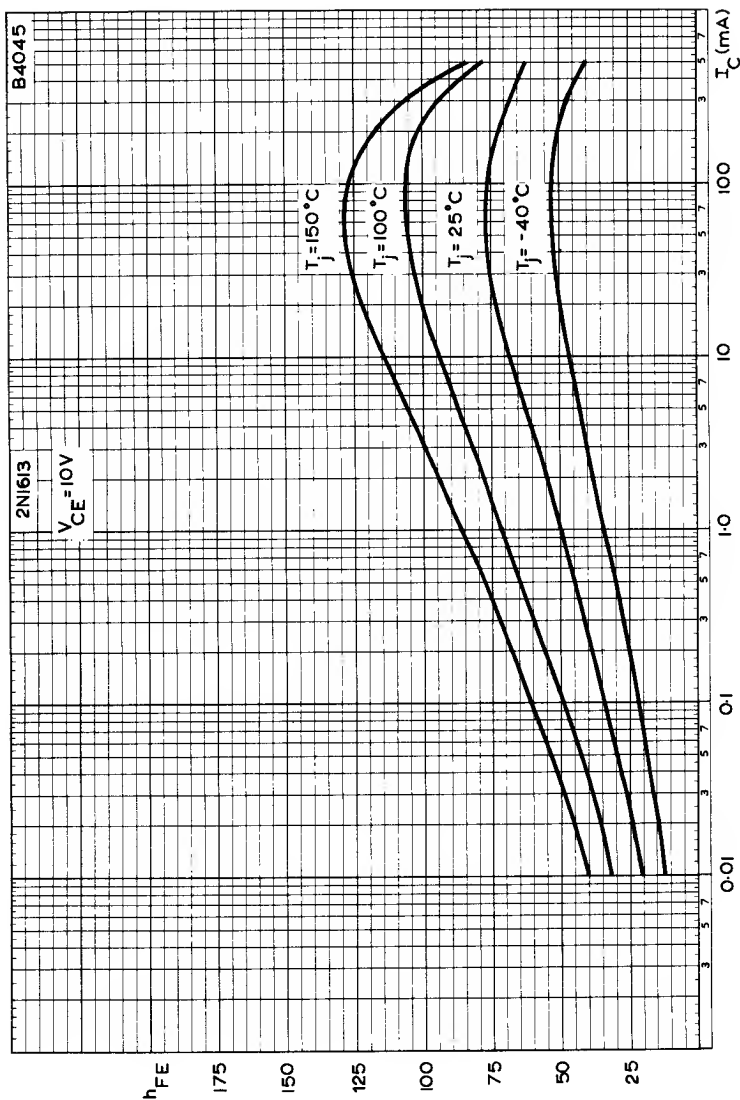
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT
TEMPERATURE



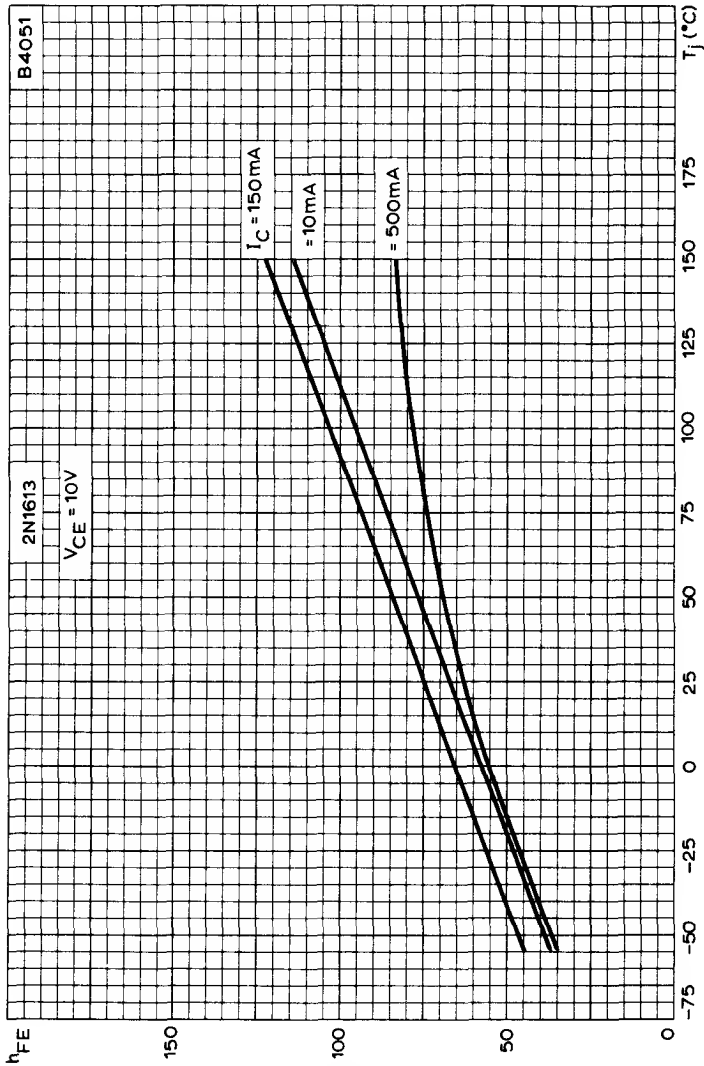
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



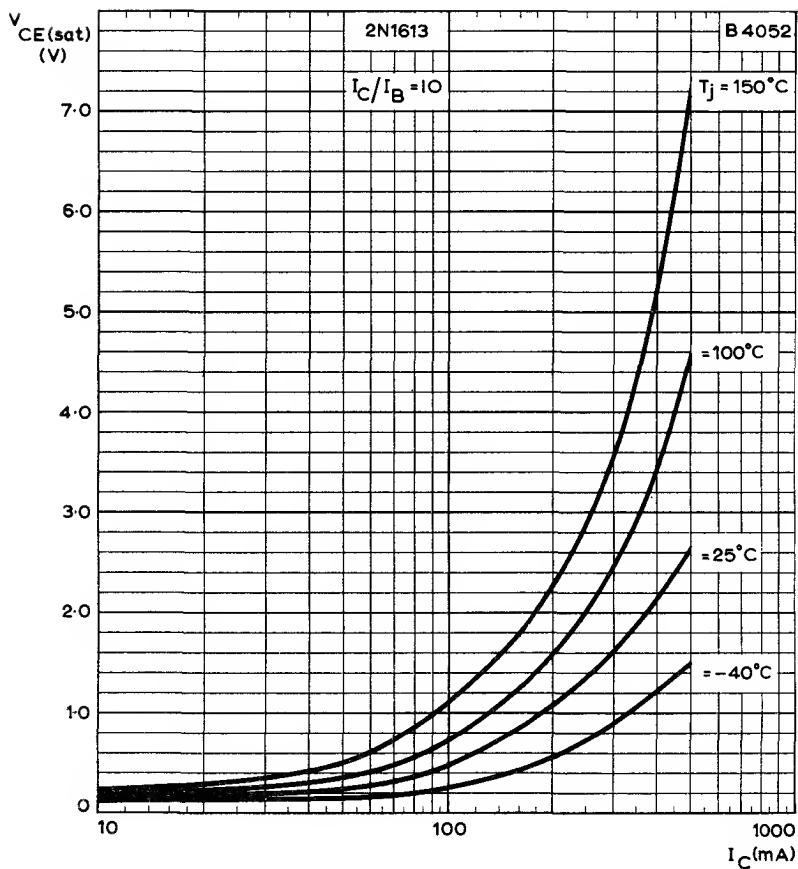
TYPICAL OUTPUT CHARACTERISTIC



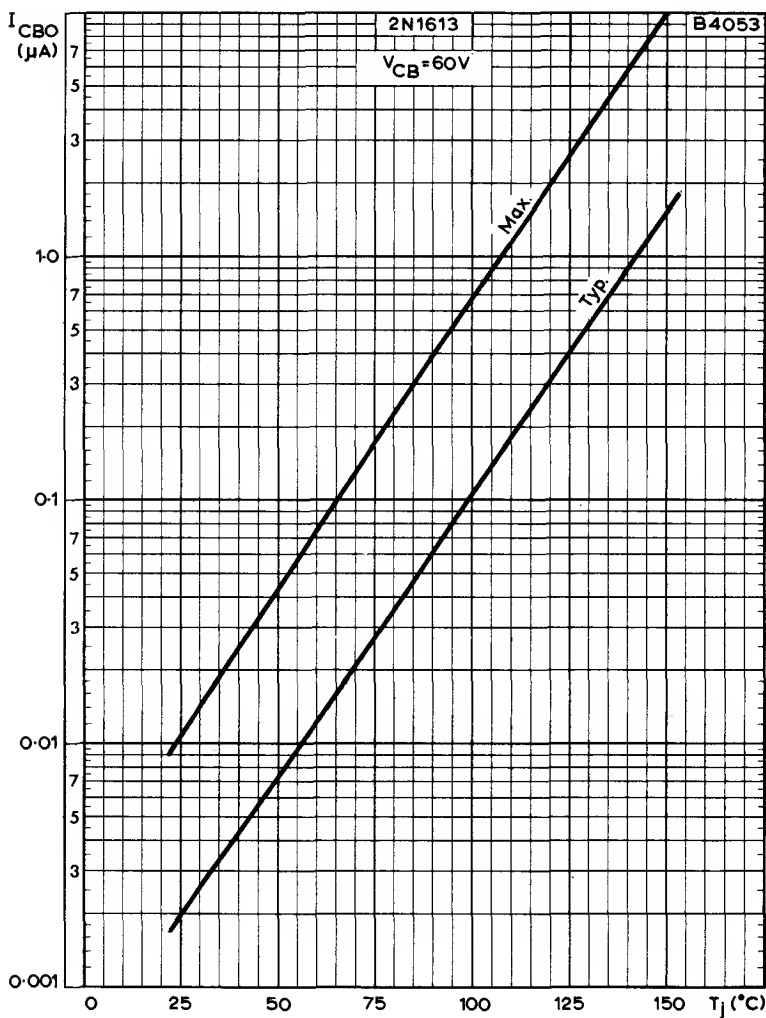
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO
PLOTTED AGAINST COLLECTOR CURRENT WITH JUNCTION
TEMPERATURE AS PARAMETER



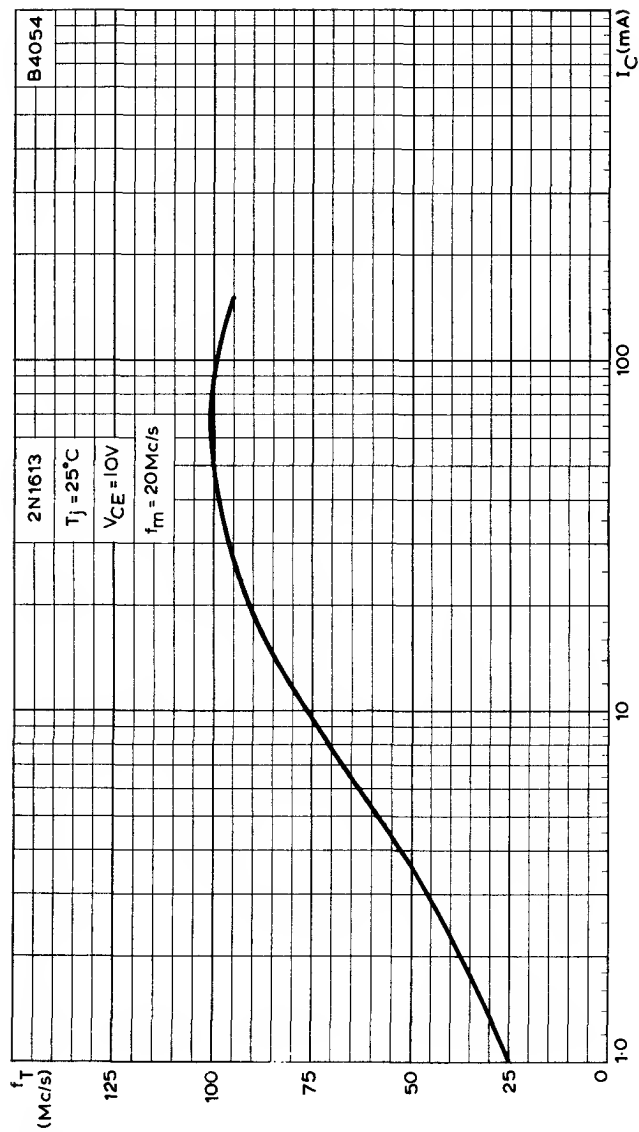
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO
PLOTTED AGAINST JUNCTION TEMPERATURE WITH COLLECTOR
CURRENT AS PARAMETER



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED
AGAINST COLLECTOR CURRENT WITH JUNCTION TEMPERATURE
AS PARAMETER



SPREAD OF COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST
JUNCTION TEMPERATURE



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT

SILICON PLANAR N-P-N TRANSISTOR

2N1711

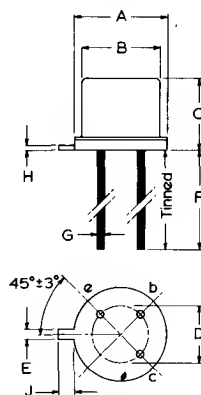
Silicon n-p-n double diffused planar transistor designed for a wide variety of applications including d.c. and wideband amplifiers.

QUICK REFERENCE DATA

V_{CBO} max. ($I_E = 0$)	+75	V
V_{CER} max. ($R_{BE} \leq 10\Omega$)	+50	V
I_{CM} max.	1.0	A
P_{tot} max. ($T_{amb} = 25^\circ C$)	800	mW
h_{FE} ($I_{CM} = 150mA$, $V_{CE} = +10V$)	100 - 300	

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-5



Millimetres

	Min.	Nom.	Max.
A	8.64	8.9	9.4
B	7.75	8.15	8.5
C	6.1	6.35	6.6
D	-	5.08	-
E	0.71	0.79	0.86
F	38	-	-
G	-	0.45	-
H	-	0.4	-
J	0.74	0.85	1.01

Collector connected to envelope

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\uparrow V_{CBO}$ max. ($I_E = 0$)	+75	V
$\uparrow V_{CER}$ max. ($R_{BE} \leq 10\Omega$)	+50	V
$\uparrow V_{EBO}$ max. ($I_C = 0$)	+7.0	V
V_{CEO} max. ($I_B = 0$)	+30	V
$\uparrow I_{CM}$ max.	1.0	A
$\uparrow P_{tot}$ max. $T_{case} = 25^\circ C$	3.0	W
$T_{case} = 100^\circ C$	1.7	W
$T_{amb} = 25^\circ C$	800	mW

Temperature

$\uparrow T_{stg}$ min.	-65	$^\circ C$
T_{stg} max.	200*	$^\circ C$
$\uparrow T_j$ (operating range)	-65 to +200	$^\circ C$

*See Soldering and Wiring Recommendation No.4.

THERMAL CHARACTERISTICS

$\uparrow \theta_{j-case}$	58.3 degC/W
$\uparrow \theta_{j-amb}$	219 degC/W

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise stated)

		Min.	Max.	
$\uparrow I_{CBO}$	Collector cut-off current			
	$V_{CB} = 60V, I_E = 0$	-	10	nA
	$V_{CB} = 60V, I_E = 0, T_{amb} = 150^\circ C$	-	10	μA
$\uparrow I_{EBO}$	Emitter cut-off current			
	$V_{EB} = 5.0V, I_C = 0$	-	5.0	nA
$\uparrow V_{BR(CBO)}$	Collector-base breakdown voltage			
	$I_C = 100\mu A, I_E = 0$	+75	-	V
$\uparrow V_{BR(EBO)}$	Emitter-base breakdown voltage			
	$I_E = 100\mu A, I_C = 0$	+7.0	-	V
$\uparrow V_{CER(sust)}$	Collector-emitter sustaining voltage (See note 1)			
	$R_{BE} \leq 10\Omega, I_C = 100mA$	+50	-	V

SILICON PLANAR N-P-N TRANSISTOR

2N1711

		Min.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage (See note 1) $I_B = 15mA, I_C = 150mA$	-	+1.5	V
$V_{BE(sat)}$	Base-emitter saturation voltage (See note 1) $I_B = 15mA, I_C = 150mA$	-	+1.3	V
h_{FE}	Large signal forward current transfer ratio $I_C = 500mA, V_{CE} = 10V$ (See note 1) $I_C = 150mA, V_{CE} = 10V$ (See note 1) $I_C = 10mA, V_{CE} = 10V$ (See note 1) $I_C = 10mA, V_{CE} = 10V,$ $T_{amb} = -55^{\circ}C$ $I_C = 0.1mA, V_{CE} = 10V$ $I_C = 0.01mA, V_{CE} = 10V$	40 100 75 35 35 20	- 300 - - -	
Small Signal characteristics				
h_{fe}	Small signal forward current transfer ratio $I_C = 1.0mA, V_{CE} = 5.0V,$ $f = 1.0kc/s$ $I_C = 5.0mA, V_{CE} = 10V,$ $f = 1.0kc/s$	50 70	200 300	
h_{ib}	Input impedance $I_C = 1.0mA, V_{CB} = 5.0V,$ $f = 1.0kc/s$ $I_C = 5.0mA, V_{CB} = 10V,$ $f = 1.0kc/s$	24 4.0	34 8.0	Ω Ω
h_{rb}	Voltage feedback ratio $I_C = 1.0mA, V_{CB} = 5.0V,$ $f = 1.0kc/s$ $I_C = 5.0mA, V_{CB} = 10V,$ $f = 1.0kc/s$	- -	5.0 5.0	$\times 10^{-4}$ $\times 10^{-4}$

Mullard

		Min.	Max.	
$\dagger h_{ob}$	Output admittance $I_C = 1.0\text{mA}$, $V_{CB} = 5.0\text{V}$, $f = 1.0\text{kc/s}$	0.1	0.5	μmho
	$I_C = 5.0\text{mA}$, $V_{CB} = 10\text{V}$, $f = 1.0\text{kc/s}$	0.1	1.0	μmho
$\dagger h_{fe}$	Small signal forward current transfer ratio $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 20\text{Mc/s}$	3.5	-	
$\dagger c_{ob}$	Output capacitance $I_C = 0$, $V_{CB} = 10\text{V}$	-	25	pF
$\dagger c_{ib}$	Input capacitance $I_C = 0$, $V_{EB} = 0.5\text{V}$	-	80	pF
$\dagger NF$	Noise figure $I_C = 0.3\text{mA}$, $V_{CE} = 10\text{V}$, $f = 1.0\text{kc/s}$, $R_S = 510\Omega$, 1 cycle bandwidth	-	8.0	dB
$\dagger J, E, D, E, C$. registered data				

NOTE

1. Measured under pulsed conditions to prevent excessive dissipation pulse duration = 300 μs , duty cycle $\leq 1\%$.

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245 $^{\circ}\text{C}$ for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored above 100 $^{\circ}\text{C}$ before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR

2N2297

Silicon n-p-n epitaxial planar transistor intended for large signal h.f. and v.h.f. amplifier applications.

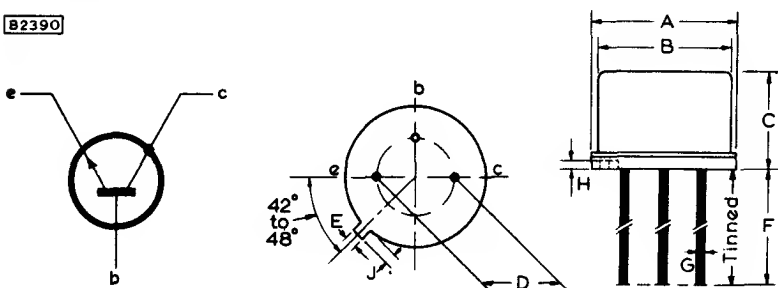
QUICK REFERENCE DATA

V_{CB} max. ($I_E = 0$)	+80	V
V_{CE} max.	+35	V
I_C max.	1.0	A
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)	800	mW
h_{FE} ($I_{CM} = 150\text{mA}$, $V_{CE} = +10\text{V}$)	40-120	
f_T min. ($I_C = 50\text{mA}$, $V_{CE} = +10\text{V}$, $f = 20\text{Mc/s}$)	60	Mc/s

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-5

82390



Collector connected to envelope

	Millimetres				Millimetres		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	8.64	8.9	9.4	F	38	-	-
B	7.75	8.15	8.50	G	-	0.45	-
C	6.10	6.35	6.60	*H	-	0.4	-
D	-	5.08	-	J	0.74	0.85	1.01
E	0.71	0.79	0.86	*Thickness of locating tab.			

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RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\dagger V_{CB} \text{ max. } (I_E = 0)$	+80	V
$\dagger V_{CE} \text{ max. } (I_B = 0)$	+35	V
$\dagger V_{EB} \text{ max. } (I_C = 0)$	+7.0	V
$\dagger I_C \text{ max.}$	1.0	A
$\dagger P_{\text{tot}} \text{ max. } T_{\text{case}} = 25^\circ \text{C}$	5.0	W
$T_{\text{case}} = 100^\circ \text{C}$	2.8	W
$T_{\text{amb}} = 25^\circ \text{C}$	0.8	W

Thermal

$\dagger T_{\text{stg}} \text{ min.}$	-65	$^\circ \text{C}$
$T_{\text{stg}} \text{ max.}$	200*	$^\circ \text{C}$
$\dagger T_j \text{ max. (operating)}$	200	$^\circ \text{C}$

*See Soldering and Wiring Recommendation No. 4.

THERMAL CHARACTERISTICS

$\dagger \text{Derating factor at } T_{\text{case}} = 25^\circ \text{C}$	28.6	mW/deg C
$T_{\text{amb}} = 25^\circ \text{C}$	4.6	mW/deg C

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR

2N2297

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

		Min.	Max.	
I_{CBO}	Collector cut-off current			
	$V_{CB} = +60\text{V}, I_E = 0$	-	10	nA
	$V_{CB} = +60\text{V}, I_E = 0,$ $T_{amb} = 150$	-	10	μA
I_{EBO}	Emitter cut-off current			
	$V_{EB} = 5.0\text{V}, I_C = 0$	-	10	nA
$V_{CEO(sust.)}$	Collector-emitter sustaining voltage			
	$I_C = 30\text{mA}$ (See note 1)	35	-	V
$V_{(BR)CBO}$	Collector-base breakdown voltage			
	$I_C = 100\mu\text{A}, I_E = 0$	80	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage			
	$I_E = 100\mu\text{A}, I_C = 0$	7.0	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage			
	$I_C = 150\text{mA}, I_B = 15\text{mA}$	-	0.2	V
	$I_C = 1.0\text{A}, I_B = 100\text{mA}$ (See notes 1 and 2)	-	1.0	V
$V_{BE(sat)}$	Base-emitter saturation voltage			
	$I_C = 1.0\text{A}, I_B = 100\text{mA}$ (See notes 1 and 2)	-	1.6	V
h_{FE}	Large signal forward current transfer ratio			
	$I_C = 150\text{mA}, V_{CE} = 10\text{V}$ (See note 1)	40	120	
	$I_C = 10\text{mA}, V_{CE} = 10\text{V}$ (See note 1)	30	-	
	$I_C = 1.0\text{A}, V_{CE} = 10\text{V}$ (See note 1)	15	-	

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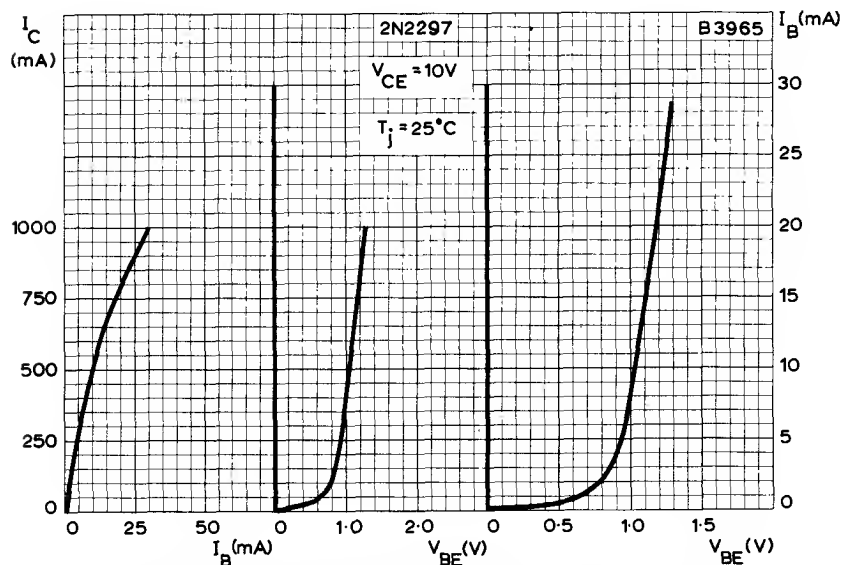
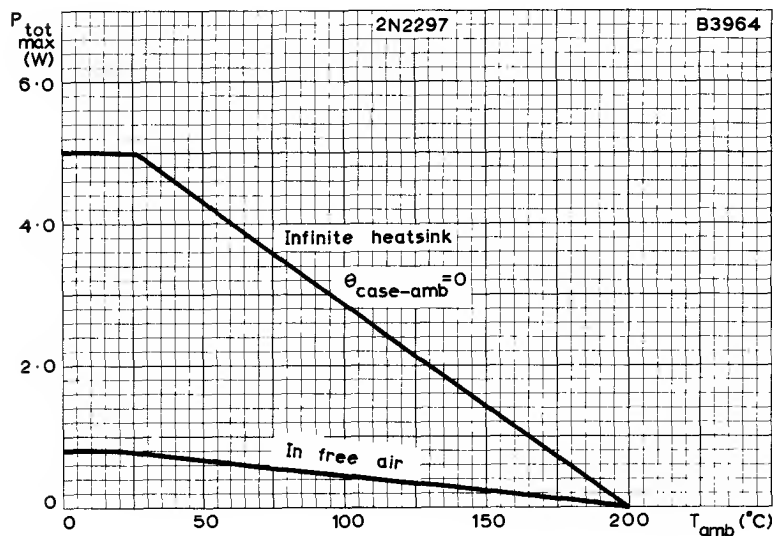
		Min.	Max.	
f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = +10\text{V}$, $f = 20\text{Mc/s}$	60	-	Mc/s
$t_{c_{ob}}$	Output capacitance $V_{CB} = 10\text{V}$, $I_E = 0$	-	12	pF
$t_{c_{ib}}$	Open-circuit input capacitance $I_C = 0$, $V_{EB} = 0.5\text{V}$	-	80	pF
t_{r_b}, c_c	Collector-base time constant $I_C = 10\text{mA}$, $V_{CB} = 10\text{V}$, $f = 4.0\text{Mc/s}$	-	800	ps
\dagger J,E,D,E,C. Registered Data.				

NOTES

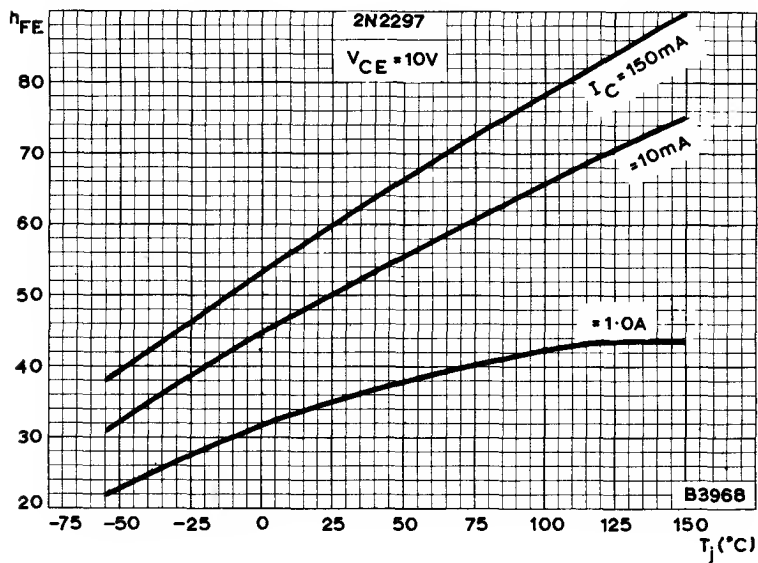
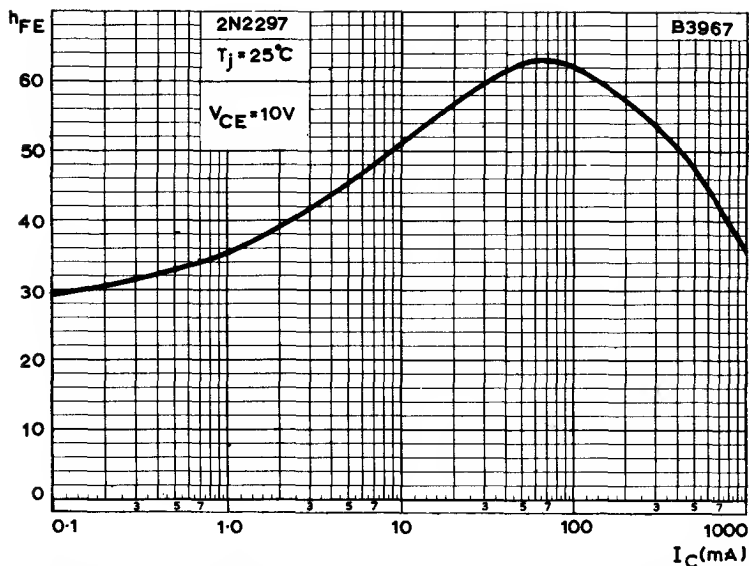
1. Measured under pulsed conditions to prevent excessive dissipation. P.W. $\approx 300\mu\text{s}$, duty cycle $\leq 1\%$.
2. Measured at a point on the lead $\leq 12.7\text{mm}$ (0.5in) from the seating plane of the transistor

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. After storage at temperatures greater than 125°C it may be necessary to take precautions in order to ensure adequate solderability of the leads.



MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE.
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



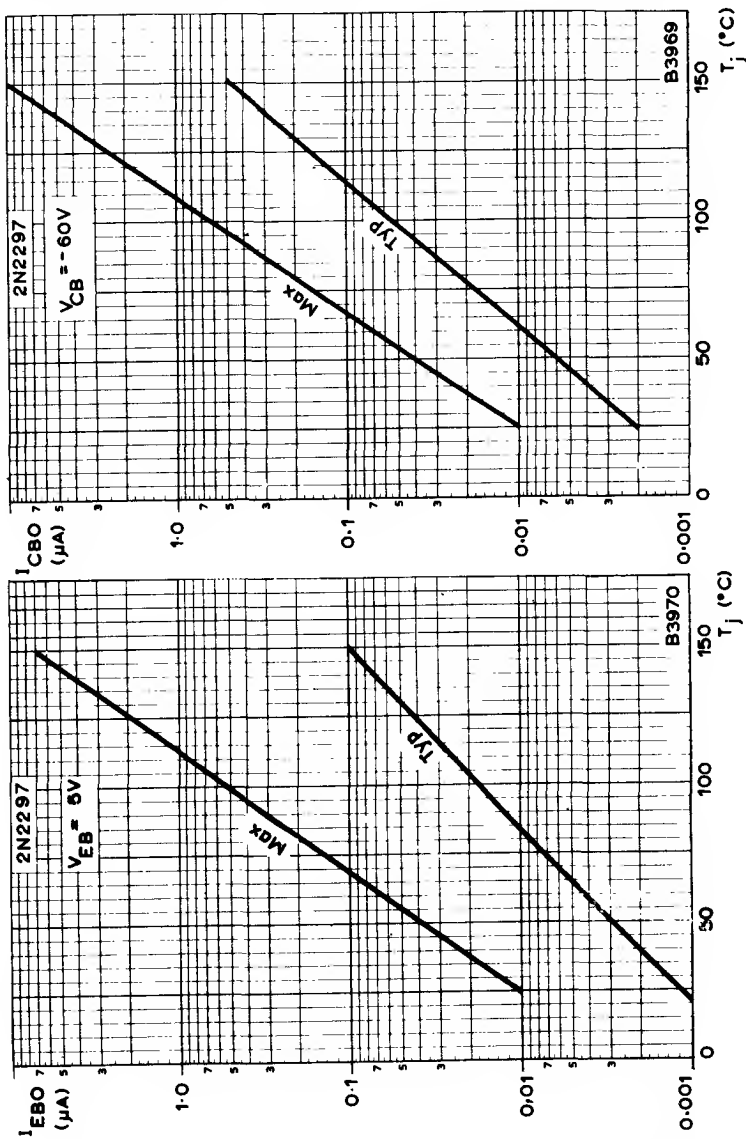
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO
 PLOTTED AGAINST COLLECTOR CURRENT

TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO
 PLOTTED AGAINST JUNCTION TEMPERATURE

Mullard

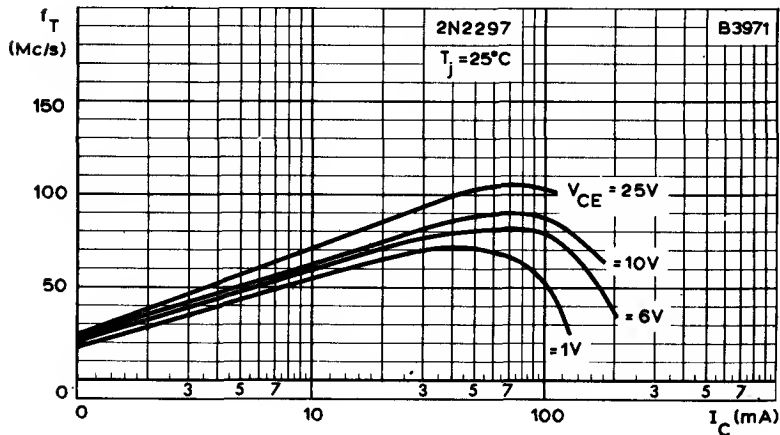
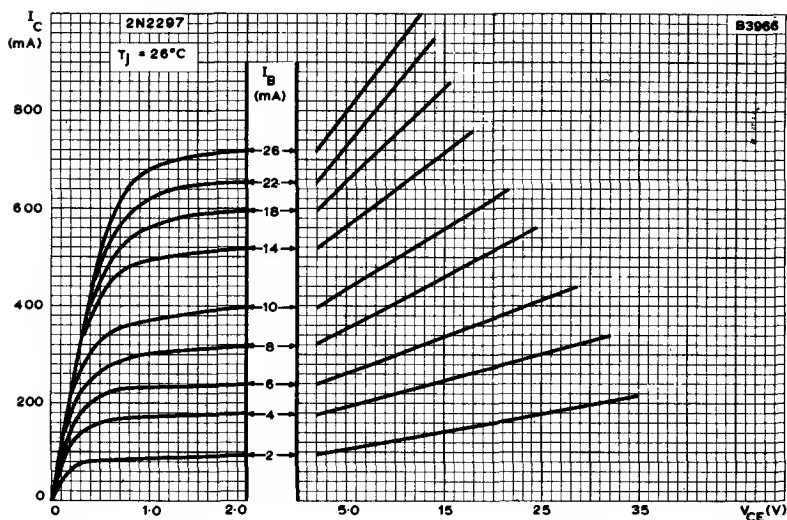
SILICON N-P-N EPITAXIAL
PLANAR TRANSISTOR

2N2297



COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST JUNCTION
TEMPERATURE
EMITTER CUT-OFF CURRENT PLOTTED AGAINST JUNCTION
TEMPERATURE

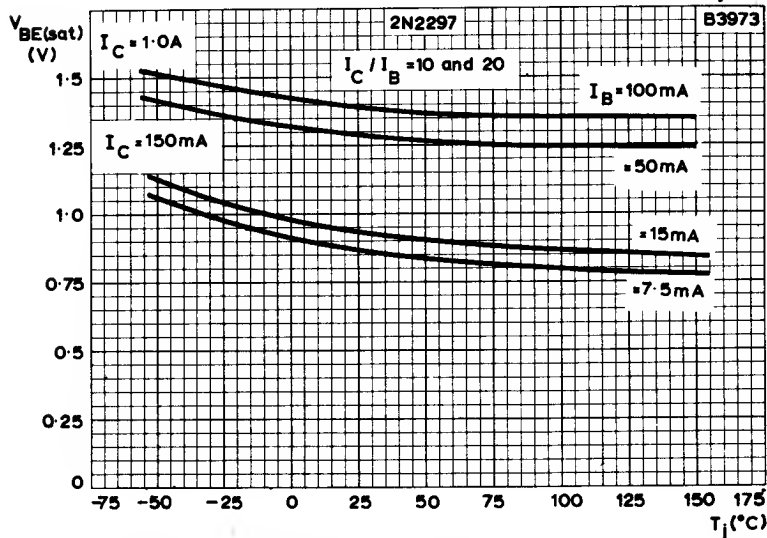
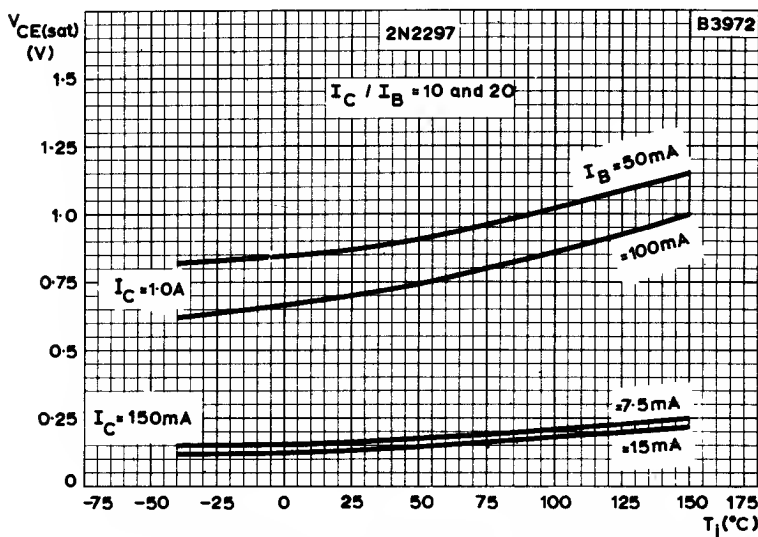
Mullard



TYPICAL OUTPUT CHARACTERISTICS. $T_j = 25^\circ\text{C}$
 TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR
 CURRENT.
 COLLECTOR-EMITTER VOLTAGE AS PARAMETER

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR

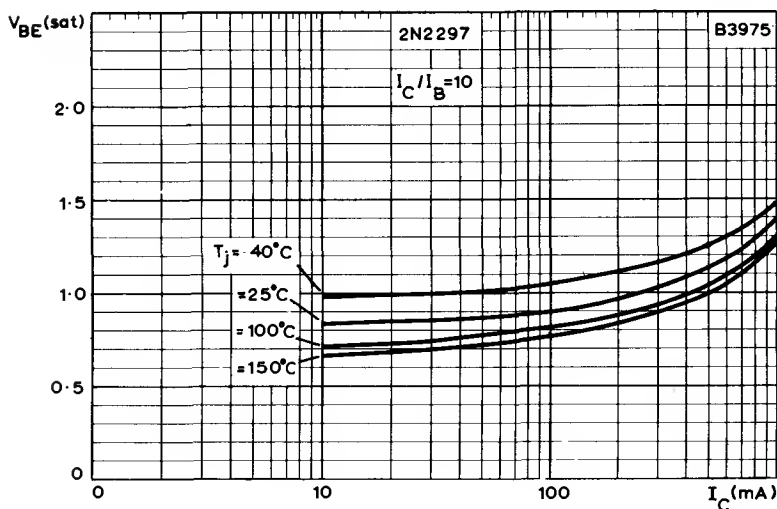
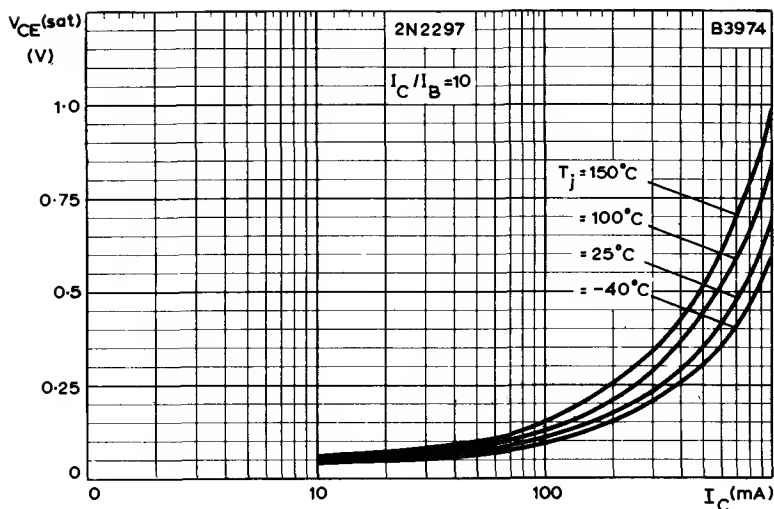
2N2297



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED
AGAINST JUNCTION TEMPERATURE. COLLECTOR AND BASE
CURRENTS AS PARAMETERS

TYPICAL BASE-EMITTER SATURATION VOLTAGE PLOTTED AGAINST
JUNCTION TEMPERATURE. COLLECTOR AND BASE CURRENTS
AS PARAMETERS

Mullard

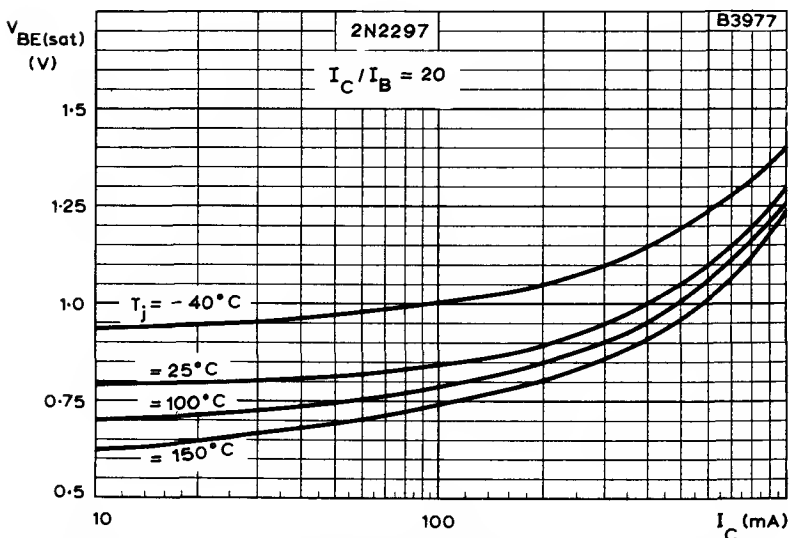
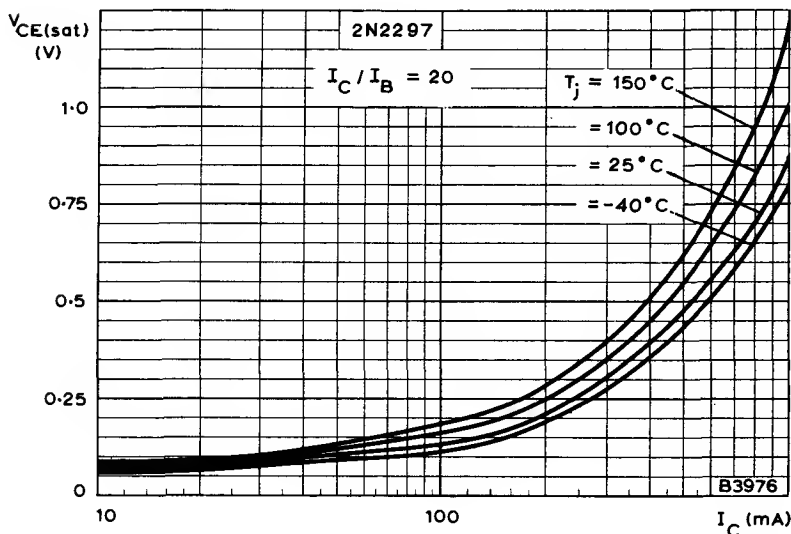


TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C/I_B = 10$.

TYPICAL BASE-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C/I_B = 10$.

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR

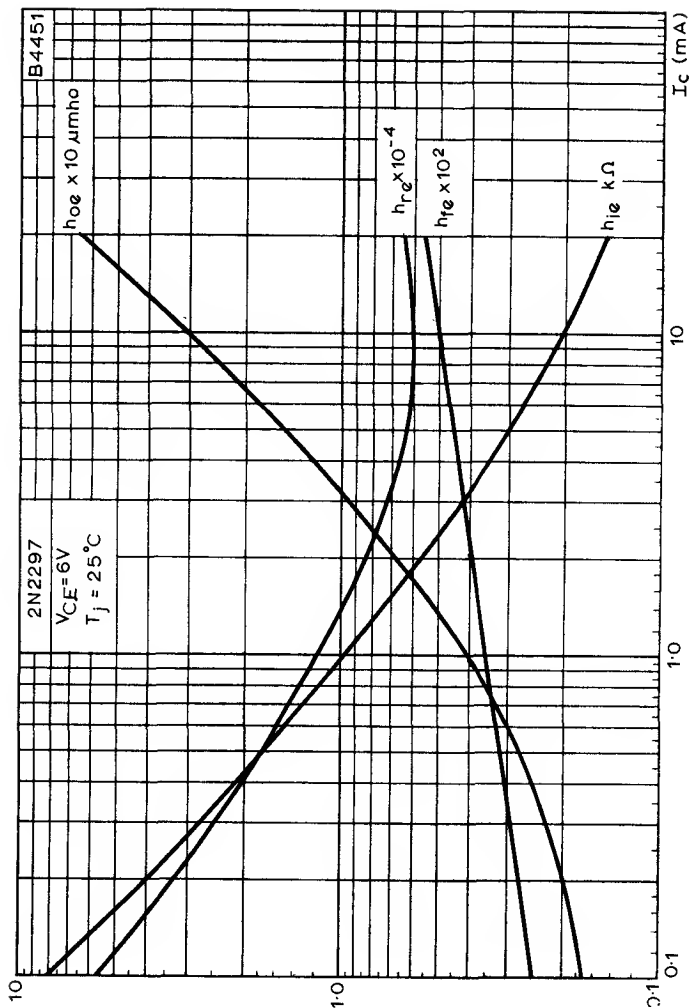
2N2297



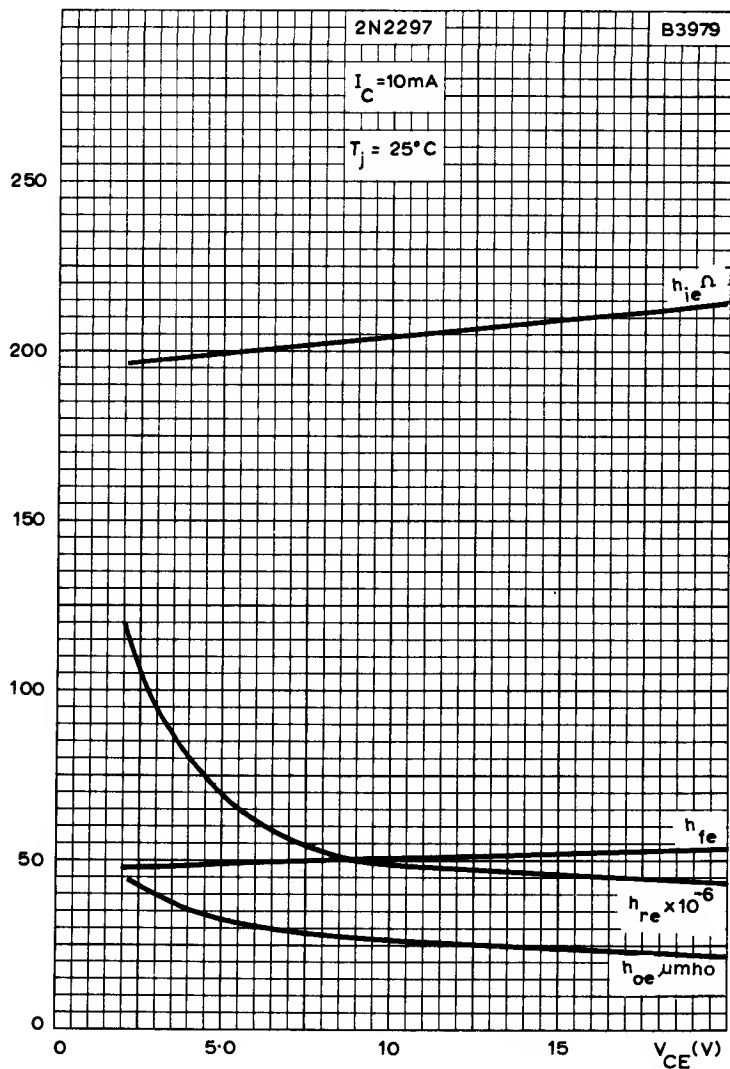
TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C / I_B = 20$.

TYPICAL BASE-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C / I_B = 20$.

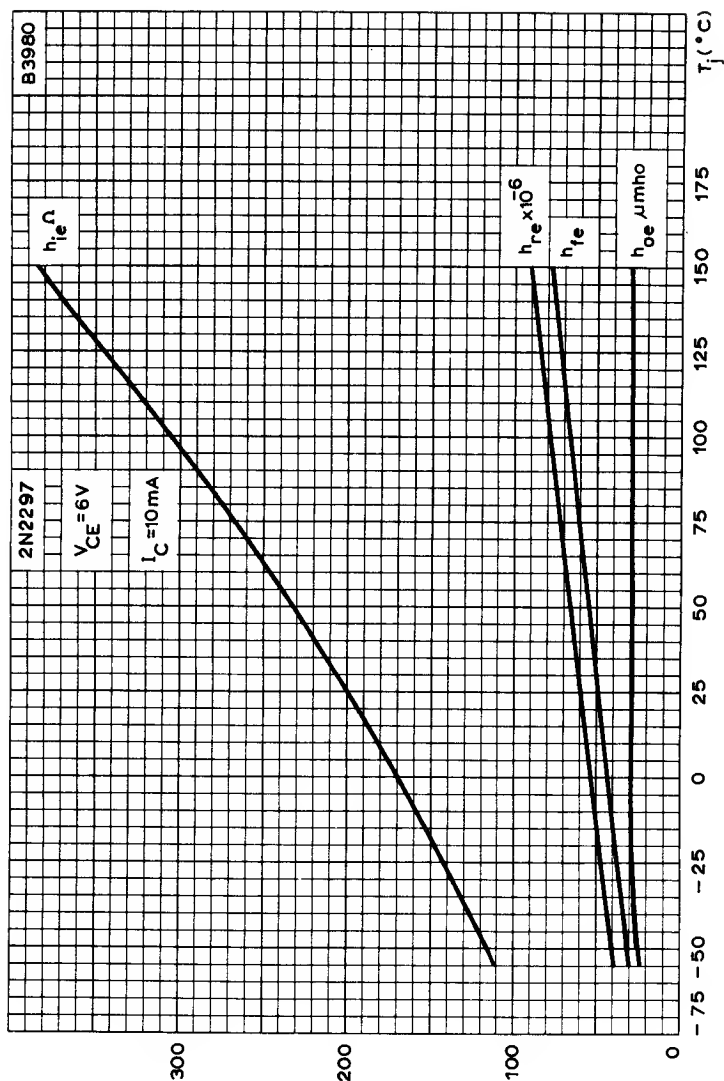
Mullard



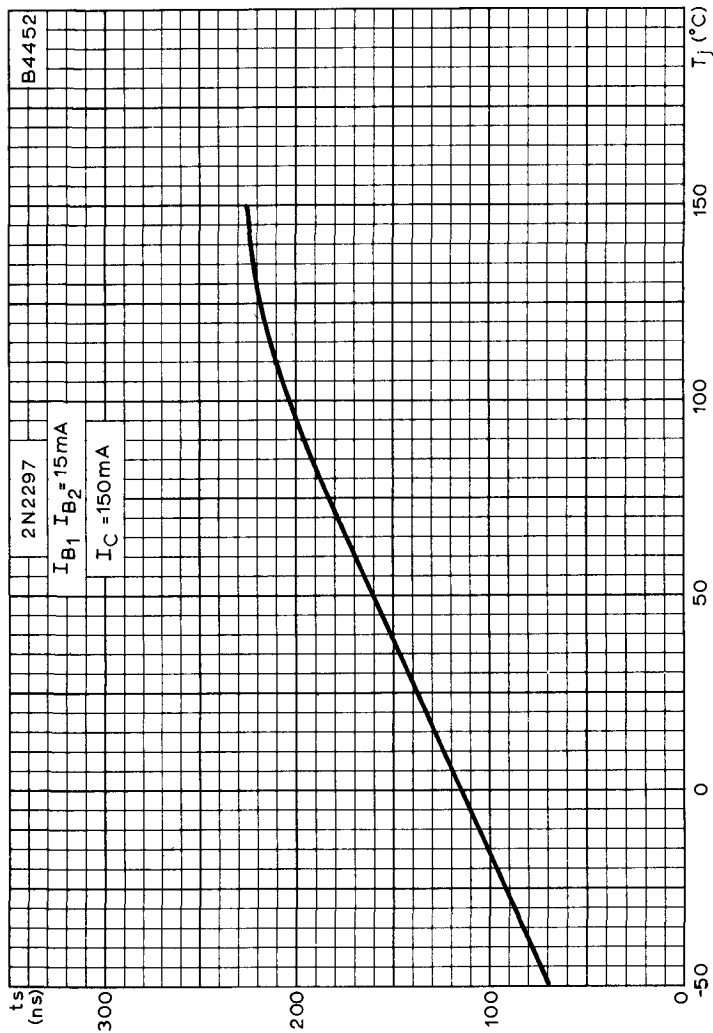
TYPICAL VARIATION OF h PARAMETERS WITH COLLECTOR CURRENT



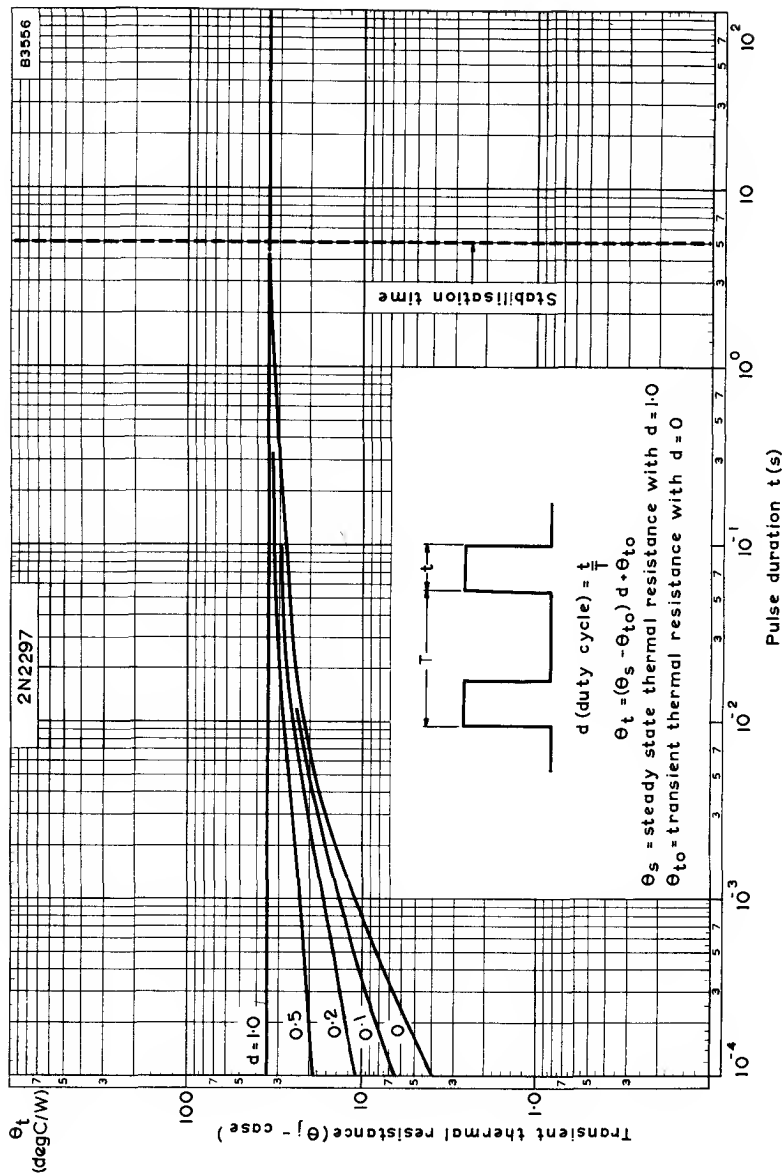
TYPICAL VARIATION OF h PARAMETERS WITH COLLECTOR-EMITTER
VOLTAGE



TYPICAL VARIATION OF h PARAMETERS WITH JUNCTION TEMPERATURE



TYPICAL VARIATION OF STORAGE TIME WITH JUNCTION TEMPERATURE



TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS
PLOTTED AGAINST PULSE DURATION

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

2N2369A

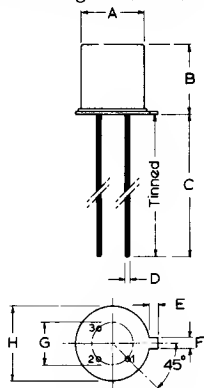
Silicon planar epitaxial n-p-n transistor primarily intended for high-speed saturated switching and high frequency amplifier applications. TO-18 construction with collector connected to envelope.

QUICK REFERENCE DATA

V_{CBO} max.	40	V
V_{CEO} max.	15	V
I_{CM} max.	500	mA
P_{tot} max. ($T_{amb} = 25^{\circ}\text{C}$)	360	mW
T_j max.	200	$^{\circ}\text{C}$
h_{FE} min. ($I_C = 10\text{mA}$, $V_{CE} = 1.0\text{V}$)	40-120	
f_T min. ($I_C = 10\text{mA}$, $f = 100\text{MHz}$)	500	MHz
t_s max. ($I_C = I_B = -I_{BM} = 10\text{mA}$)	13	ns

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-18



Millimetres

	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.33
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections 1. Emitter

2. Base

3. Collector connected to envelope

Mullard

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	40	V
V_{CES} max.	40	V
V_{CEO} max. ($I_C = 0.01$ to 10mA)	15	V
V_{EBO} max.	4.5	V
I_{CM} max. ($10\mu\text{s}$ pulse)	500	mA
I_C max.	200	mA
P_{tot} max. $T_{amb} = 25^\circ\text{C}$	360	mW
$T_{case} = 25^\circ\text{C}$	1200	mW
$T_{case} = 100^\circ\text{C}$	680	mW

Temperature

T_{stg} min.	-65	$^\circ\text{C}$
T_{stg} max.	200	$^\circ\text{C}$
T_j max.	200	$^\circ\text{C}$

†THERMAL CHARACTERISTICS

Derating factors $T_{amb} \geq 25^\circ\text{C}$	2.06	mW/degC
$T_{case} \geq 25^\circ\text{C}$	6.85	mW/degC

†ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 20\text{V}$, $I_E = 0$, $T_{amb} = 150^\circ\text{C}$	-	30	μA
I_{CES}	Collector-emitter cut-off current $V_{CE} = 20\text{V}$, $V_{BE} = 0$	-	0.4	μA
$-I_{BEX}$	Base current $V_{CE} = 20\text{V}$, $V_{BE} = 0$	-	0.4	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\mu\text{A}$, $I_E = 0$	40	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage $I_C = 10\mu\text{A}$, $V_{BE} = 0$	40	-	V

† J. E. D. E. C. registered data.

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

2N2369A

		Min.	Max.	
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 10\mu A, I_C = 0$	4.5	-	V
$V_{CEO(sust)}$	*Collector-emitter sustaining voltage $I_C = 10mA, I_B = 0$	15	-	V
h_{FE}	*Large signal forward current transfer ratio $I_C = 10mA, V_{CE} = 1.0V$ $I_C = 10mA, V_{CE} = 0.35V,$ $T_{amb} = -55^{\circ}C$ $I_C = 30mA, V_{CE} = 0.4V$ $I_C = 100mA, V_{CE} = 1.0V$	40 20 30 20	120 - - -	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 10mA, I_B = 1.0mA$ $I_C = 10mA, I_B = 1.0mA,$ $T_{amb} = 125^{\circ}C$ $I_C = 30mA, I_B = 3.0mA$ $I_C = 100mA, I_B = 10mA$	- - - -	0.20 0.30 0.25 0.50	V V V V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 10mA, I_B = 1.0mA$ $I_C = 10mA, I_B = 1.0mA,$ $T_{amb} = 125^{\circ}C$ $I_C = 10mA, I_B = 1.0mA$ $T_{amb} = -55^{\circ}C$ $I_C = 30mA, I_B = 3.0mA$ $I_C = 100mA, I_B = 10mA$	0.70 0.59 - - -	0.85 - 1.02 1.15 1.60	V V V V V
f_T	Transition frequency $V_{CE} = 10V, I_C = 10mA,$ $f = 100MHz$	500	-	MHz

*Measured under pulsed conditions to avoid excessive dissipation, pulse width = 300 μ s duty cycle $\leq 2\%$.

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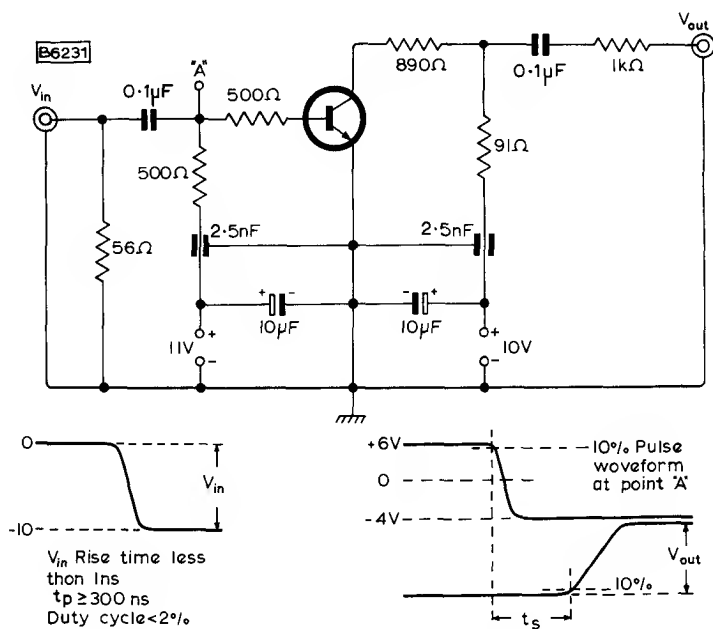
		Min.	Max.	
c_{tc}	Collector capacitance $V_{CB} = 5.0V, I_E = I_C = 0,$ $f = 140kHz$	-	4.0	pF
t_s	Storage time (see fig.1.) $I_C = I_B = -I_{BM} = 10mA$	-	13	ns
t_{on}	Turn-on time (see fig.2.) $I_C = 10mA, I_B = 3.0mA$	-	12	ns
t_{off}	Turn-off time (see fig.2.) $I_C = 10mA, I_B = 3.0mA,$ $-I_{BM} = 1.5mA$	-	18	ns

SOLDERING RECOMMENDATION

†Max. T_{lead} 1/16" from case for 60 seconds is 300°C.

†J.E.D.E.C. registered data

STORAGE TIME TEST CIRCUIT



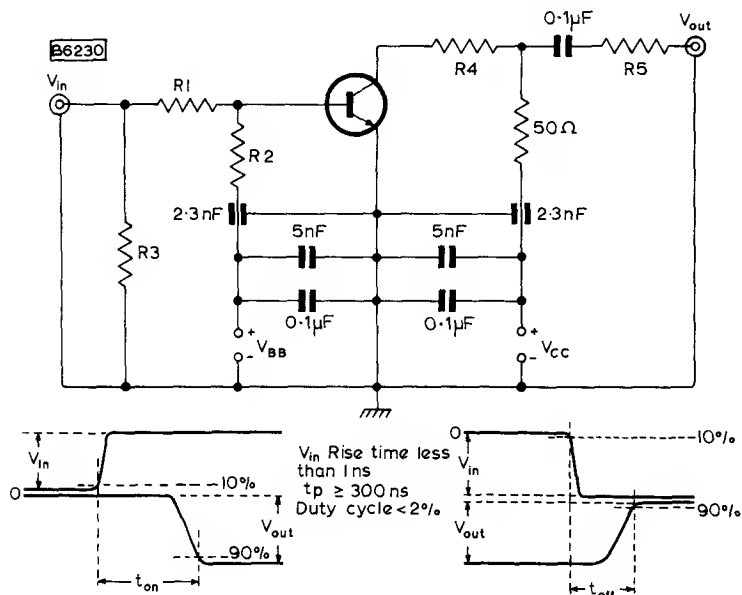
Input and output waveforms

Fig. 1

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

2N2369A

t_{on} AND t_{off} TEST CIRCUIT



Input and output waveforms

Fig. 2

Circuit conditions:

V_{CC}	$R_1 = R_2$	R_3	R_4	R_5	t_{on}		t_{off}	
					V_{BB}	V_{in}	V_{BB}	V_{in}
(V)	(k Ω)	(Ω)	(Ω)	(Ω)	(V)	(V)	(V)	(V)
3.0	3.3	50	220	0	-3.0	15	12	-15

Mullard

**P-N-P SILICON PLANAR
EPITAXIAL TRANSISTORS**

**2N2904
2N2904A**

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

QUICK REFERENCE DATA

	2N2904	2N2904A	
$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C < 100\text{mA}$)	40	60	V
$-I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)		600	mW
T_j max.		200	$^\circ\text{C}$
h_{FE} ($-I_C = 150\text{mA}$, $-V_{CE} = 10\text{V}$)	40-120		
f_T min. ($-I_C = 50\text{mA}$, $f = 100\text{MHz}$)	200		MHz
t_s max. ($-I_{CS} = 150\text{mA}$, $-I_B = +I_{BM} = 15\text{mA}$)	80		ns

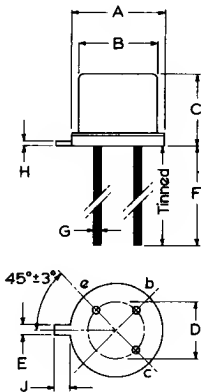
Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

Millimetres

	Min.	Nom.	Max.
A	8.64	8.90	9.40
B	7.75	8.15	8.50
C	6.10	6.35	6.60
D	-	5.08	-
E	0.71	0.79	0.86
F	38	-	-
G	-	0.45	-
H	-	0.4	-
J	0.74	0.85	1.0



Collector connected to envelope

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\uparrow -V_{CBO}$ max.		60	V
$\uparrow -V_{CEO}$ max. ($-I_C = 0$ to 100mA)	2N2904	40	V
	2N2904A	60	V
$\uparrow -V_{EBO}$ max.		5.0	V
$\uparrow -I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)		600	mW

Temperature

T_{stg} min.		-65	$^\circ\text{C}$
T_{stg} max.		200	$^\circ\text{C}$
T_j max.		200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

Θ_{j-amb}		292	degC/W
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†ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 50\text{V}, I_E = 0$	2N2904	-	20	nA
		2N2904A	-	10	nA
	$-V_{CB} = 50\text{V}, I_E = 0,$				
	$T_{amb} = 150^\circ\text{C}$	2N2904	-	20	μA
		2N2904A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE} = 30\text{V}, +V_{BE} = 0.5\text{V}$		-	50	nA
I_{BEX}	Base current				
	$-V_{CE} = 30\text{V}, +V_{BE} = 0.5\text{V}$		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C = 10\mu\text{A}, I_E = 0$		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C = 10\text{mA}, I_B = 0$	2N2904	40	-	V
		2N2904A	60	-	V

*Pulse condition, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

†J.E.D.E.C. registered data.

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2904
2N2904A

		Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A, I_C = 0$	5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$	-	0.4	V
	$-I_C = 500mA, -I_B = 50mA$	-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$	-	1.3	V
	$-I_C = 500mA, -I_B = 50mA$	-	2.6	V
h_{FE}	Static forward current transfer ratio			
	$-I_C = 0.1mA, -V_{CE} = 10V$ 2N2904	20	-	
	2N2904A	40	-	
	$-I_C = 1.0mA, -V_{CE} = 10V$ 2N2904	25	-	
	2N2904A	40	-	
	$-I_C = 10mA, -V_{CE} = 10V$ 2N2904	35	-	
	2N2904A	40	-	
	* $-I_C = 150mA, -V_{CE} = 10V$	40	120	
	* $-I_C = 500mA, -V_{CE} = 10V$ 2N2904	20	-	
	2N2904A	40	-	
c_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V, I_E = 0, f = 100kHz$	-	8.0	pF
c_{ib}	Common base, open circuit input capacitance $V_{BE} = 2.0V, I_C = 0, f = 100kHz$	-	30	pF
f_T	Transition frequency $-V_{CE} = 20V, -I_C = 50mA,$ $f = 100MHz$	200	-	MHz

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Mullard

Switching characteristics

Max.

Turn-on (see Fig.1)

$$-V_{CC} = 30V, -I_{CS} = 150mA, -I_B = 15mA$$

t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	45	ns

Turn-off (see Fig.2)

$$-V_{CC} = 6V, -I_{CS} = 150mA, -I_B = +I_{BM} = 15mA$$

t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time ($t_s + t_f$)	100	ns

TEST CIRCUITS

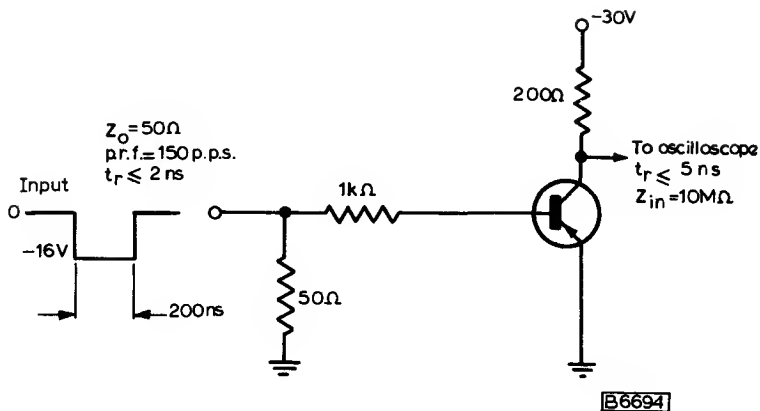


Fig.1

Test circuit for determining delay, rise and turn-on time

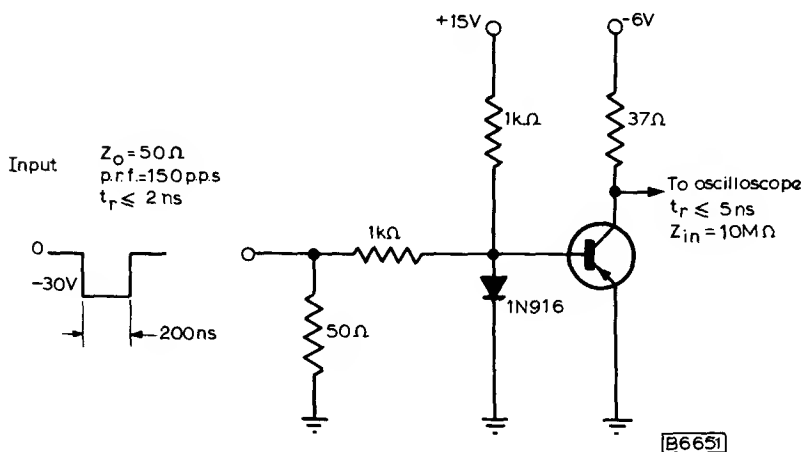


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

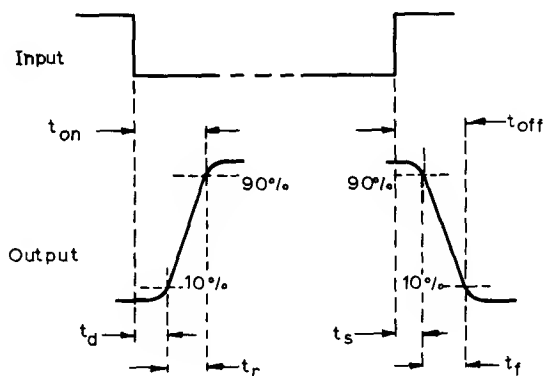
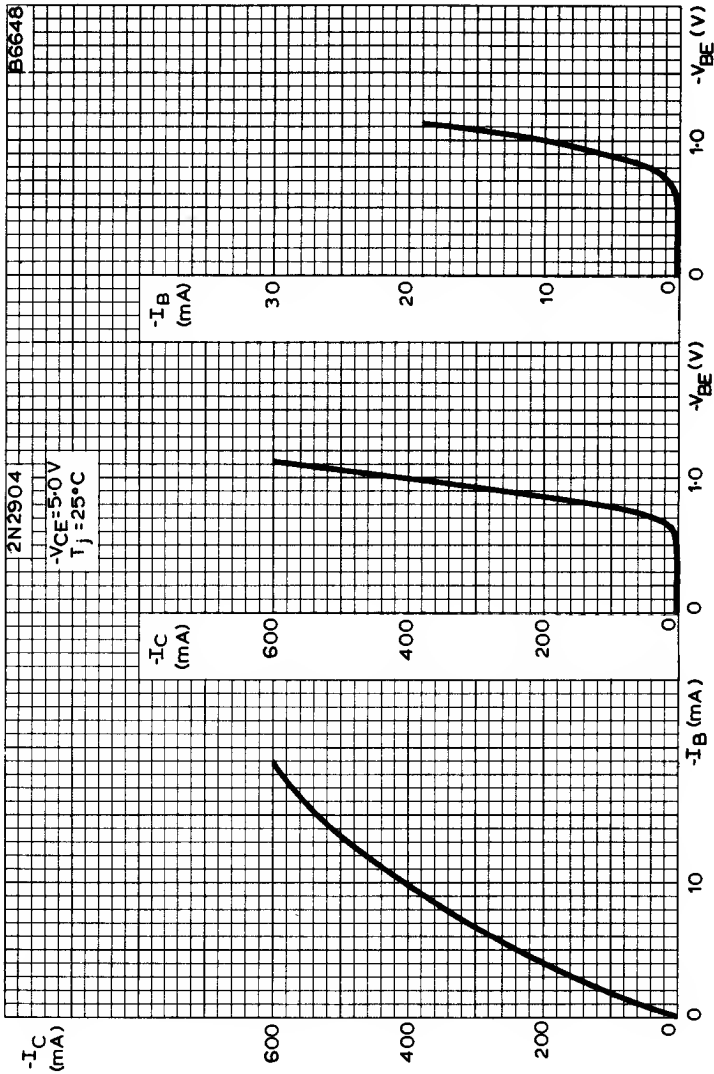
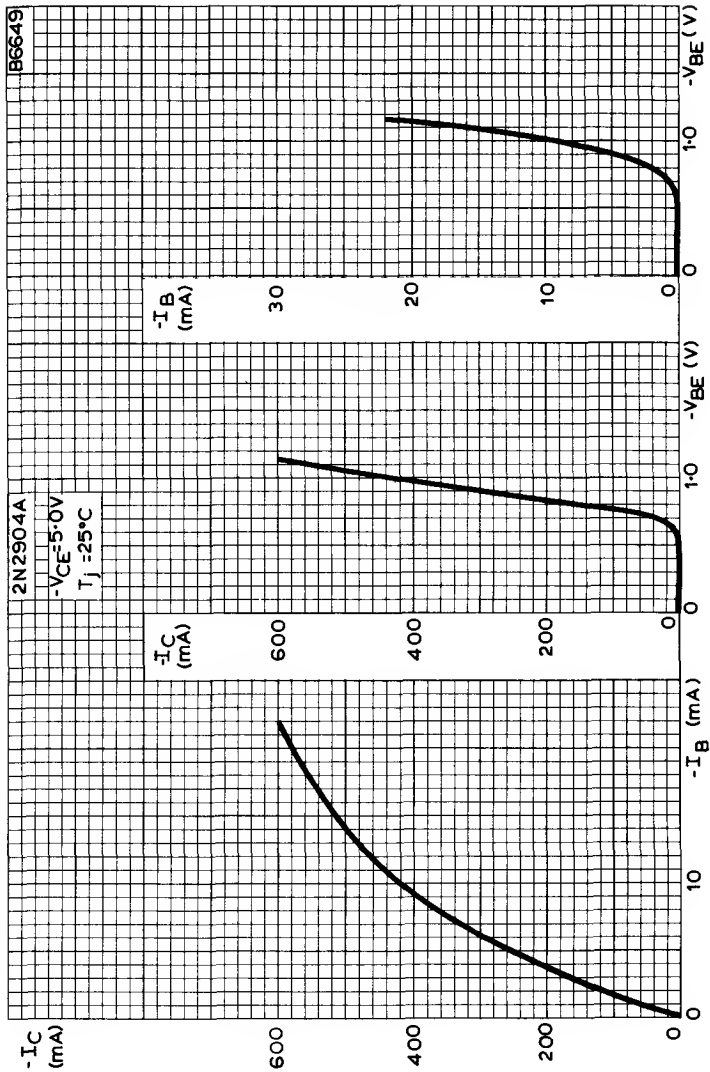


Fig. 3

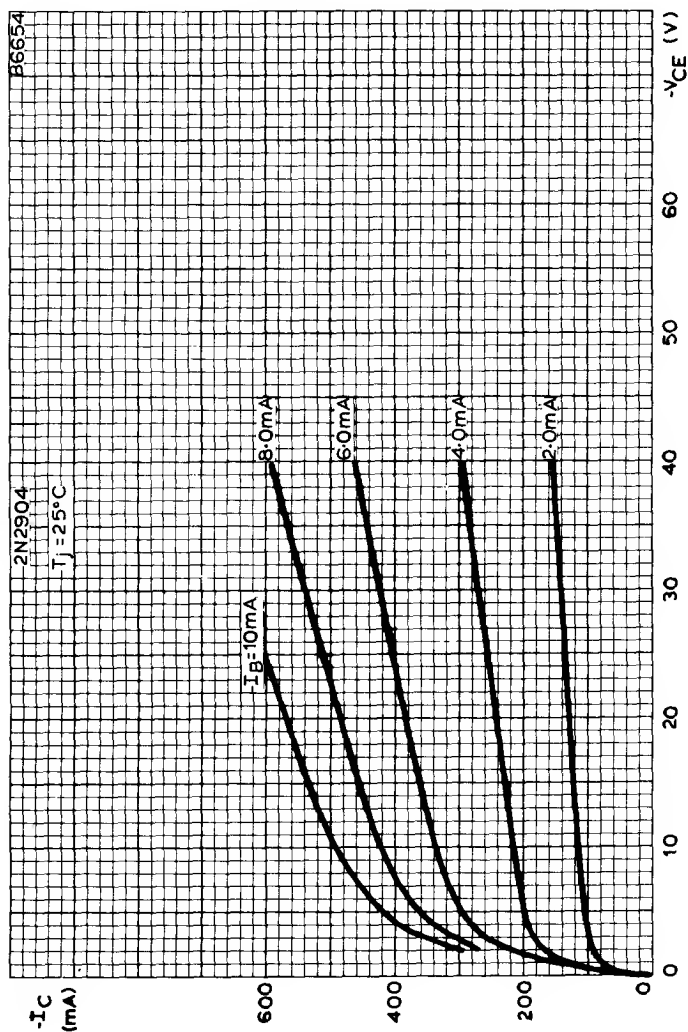
B6655



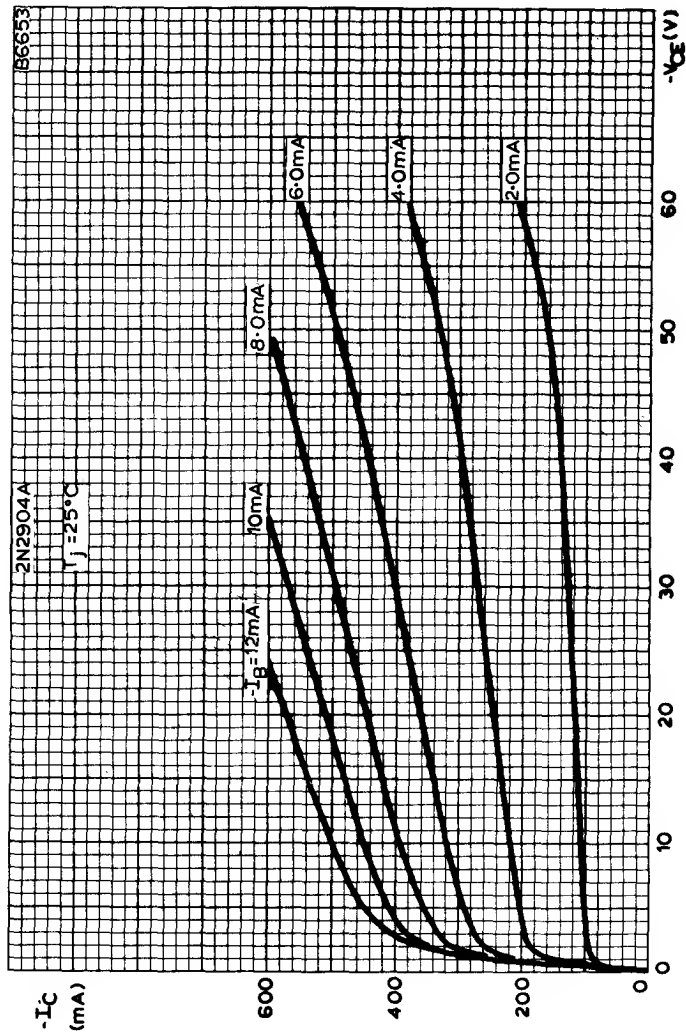
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS

Mullard

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2905 2N2905A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

QUICK REFERENCE DATA

	2N2905	2N2905A	
$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max.	40	60	V
$-I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)		600	mW
T_j max.		200	$^\circ\text{C}$
h_{FE} ($-I_C = 150\text{mA}$, $-V_{CE} = 10\text{V}$)		100-300	
f_T min. ($-I_C = 50\text{mA}$, $f = 100\text{MHz}$)		200	MHz
t_s max. ($-I_{CS} = 150\text{mA}$, $-I_B = +I_{BM} = 15\text{mA}$)		80	ns

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

	Millimetres		
	Min.	Typ.	Max.
A	9.10	-	9.39
B	8.2	-	8.50
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to envelope

Mullard

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C = 0$ to 100mA)	2N2905	40	V
	2N2905A	60	V
$-V_{EBO}$ max.		5.0	V
$-I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^\circ C$)		600	mW

Temperature

T_{stg} min.		-65	$^\circ C$
T_{stg} max.		200	$^\circ C$
T_j max.		200	$^\circ C$

†THERMAL CHARACTERISTIC

θ_{j-amb}		290	degC/W
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†ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 50V, I_E = 0$	2N2905	-	20	nA
		2N2905A	-	10	nA
	$-V_{CB} = 50V, I_E = 0,$				
	$T_{amb} = 150^\circ C$	2N2905	-	20	μA
		2N2905A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE} = 30V, +V_{BE} = 0.5V$		-	50	nA
I_{BEX}	Base current				
	$-V_{CE} = 30V, +V_{BE} = 0.5V$		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C = 10\mu A, I_E = 0$		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C = 10mA, I_B = 0$	2N2905	40	-	V
		2N2905A	60	-	V

†J.E.D.E.C. registered data

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2905 2N2905A

		Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A, I_C = 0$	5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$	-	0.4	V
	$-I_C = 500mA, -I_B = 50mA$	-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$	-	1.3	V
	$-I_C = 500mA, -I_B = 50mA$	-	2.6	V
h_{FE}	Static forward current transfer ratio			
	$-I_C = 0.1mA, -V_{CE} = 10V$ 2N2905	35	-	
	2N2905A	75	-	
	$-I_C = 1.0mA, -V_{CE} = 10V$ 2N2905	50	-	
	2N2905A	100	-	
	$-I_C = 10mA, -V_{CE} = 10V$ 2N2905	75	-	
	2N2905A	100	-	
	* $-I_C = 150mA, -V_{CE} = 10V$	100	300	
	* $-I_C = 500mA, -V_{CE} = 10V$ 2N2905	30	-	
	2N2905A	50	-	
C_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V, I_E = 0, f = 100kHz$	-	8.0	pF
C_{ib}	Common base, open circuit input capacitance $+V_{BE} = 2.0V, I_C = 0, f = 100kHz$	-	30	pF
f_T	Transition frequency $-V_{CE} = 20V, -I_C = 50mA, f = 100MHz$	200	-	MHz

*Pulse conditions, pulse width = 300 μ A, duty cycle $\leq 2\%$.

Switching characteristics

Max.

Turn-on (see fig.1)

$$-V_{CC} = 30V, -I_{CS} = 150mA, -I_B = 15mA$$

t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	45	ns

Turn-off (see fig.2)

$$-V_{CC} = 6.0V, -I_{CS} = 150mA, -I_B = +I_{BM} = 15mA$$

t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time ($t_s + t_f$)	100	ns

TEST CIRCUITS

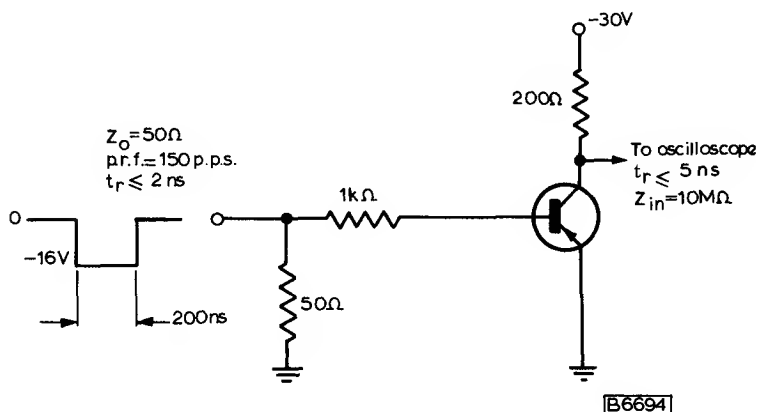


Fig.1

Test circuit for determining delay, rise and turn-on time

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2905
2N2905A

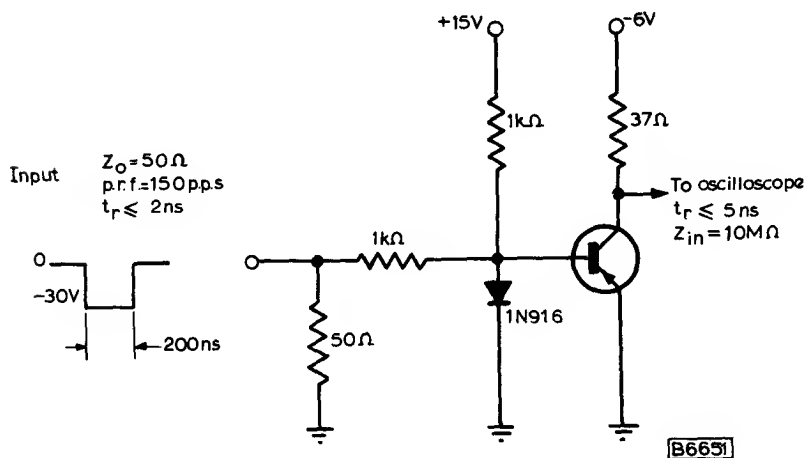


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

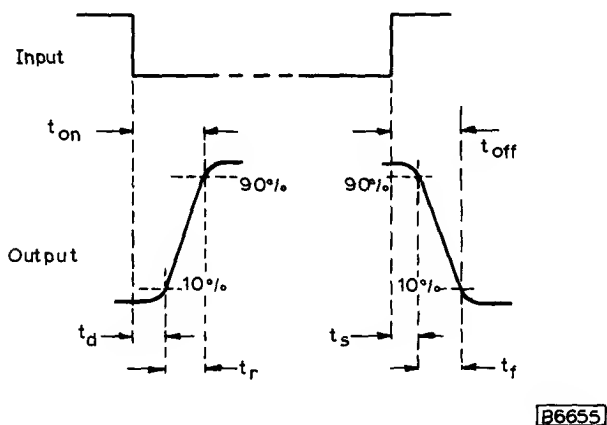


Fig. 3

Mullard

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2906
2N2906A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

QUICK REFERENCE DATA

	2N2906	2N2906A
$-V_{CBO}$ max.		60 V
$-V_{CEO}$ max. ($-I_C < 100\text{mA}$)	40	60 V
$-I_C$ max.		600 mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)	400	mW
T_j max.	200	$^\circ\text{C}$
h_{FE} ($-I_C = 150\text{mA}$, $-V_{CE} = 10\text{V}$)	40-120	
f_T min. ($-I_C = 50\text{mA}$, $f = 100\text{MHz}$)	200	MHz
t_s max. ($-I_{CS} = 150\text{mA}$, $-I_B = +I_{BM} = 15\text{mA}$)	80	ns

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-18

B.S. 3934 SO-12A/SB3-6A

	Millimetres		
	Min.	Typ.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Viewed from underside
Connections 1. Emitter 3. Collector connected to envelope
2. Base

Mullard

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C = 0$ to 100mA)	2N2906	40	V
	2N2906A	60	V
$-V_{EBO}$ max.		5.0	V
$-I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^{\circ}C$)		400	mW

Temperature

T_{stg} min.		-65	$^{\circ}C$
T_{stg} max.		200	$^{\circ}C$
T_j max.		200	$^{\circ}C$

†THERMAL CHARACTERISTIC

Θ_{j-amb}		0.44	degC/mW
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†ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$ unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 50V, I_E = 0$	2N2906	-	20	nA
		2N2906A	-	10	nA
	$-V_{CB} = 50V, I_E = 0,$				
	$T_{amb} = 150^{\circ}C$	2N2906	-	20	μA
		2N2906A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE} = 30V, +V_{BE} = 0.5V$		-	50	nA
I_{BEX}	Base current				
	$-V_{CE} = 30V, +V_{BE} = 0.5V$		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C = 10\mu A, I_E = 0$		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C = 10mA, I_B = 0$	2N2906	40	-	V
		2N2906A	60	-	V

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

†J.E.D.E.C. registered data.

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2906
2N2906A

			Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A, I_C = 0$		5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$		-	0.4	V
	$-I_C = 500mA, -I_B = 50mA$		-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$		-	1.3	V
	$-I_C = 500mA, -I_B = 50mA$		-	2.6	V
h_{FE}	Static forward current transfer ratio				
	$-I_C = 0.1mA, -V_{CE} = 10V$	2N2906	20	-	
		2N2906A	40	-	
	$-I_C = 1.0mA, -V_{CE} = 10V$	2N2906	25	-	
		2N2906A	40	-	
	$-I_C = 10mA, -V_{CE} = 10V$	2N2906	35	-	
		2N2906A	40	-	
	* $-I_C = 150mA, -V_{CE} = 10V$		40	120	
	* $-I_C = 500mA, -V_{CE} = 10V$	2N2906	20	-	
		2N2906A	40	-	
C_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V, I_E = 0, f = 100kHz$		-	8.0	pF
C_{ib}	Common base, open circuit input capacitance $V_{BE} = 2.0V, I_C = 0, f = 100kHz$		-	30	pF
f_T	Transition frequency $-V_{CE} = 20V, -I_C = 50mA,$ $f = 100MHz$		200	-	MHz

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Mullard

Switching characteristics

Max.

Turn-on (see Fig.1)

$$-V_{CC} = 30V, -I_{CS} = 150mA, -I_B = 15mA$$

t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	45	ns

Turn-off (see Fig.2)

$$-V_{CC} = 6V, -I_{CS} = 150mA, -I_B = +I_{BM} = 15mA$$

t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time ($t_s + t_f$)	100	ns

TEST CIRCUITS

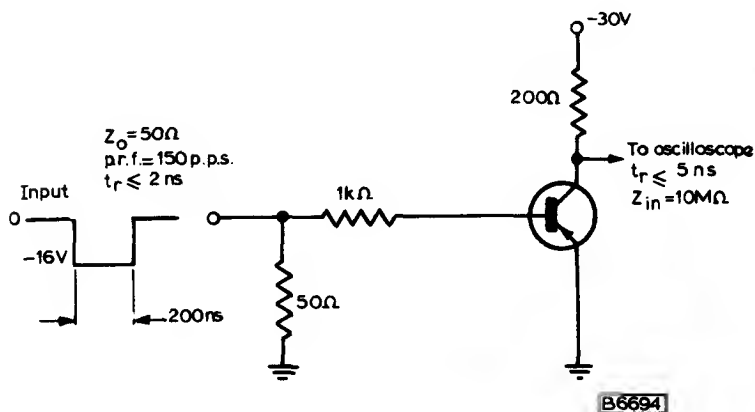


Fig.1

Test circuit for determining delay, rise and turn-on time

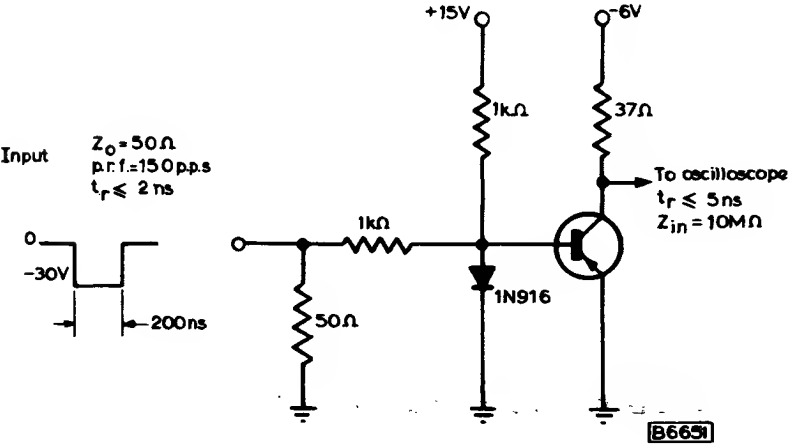


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

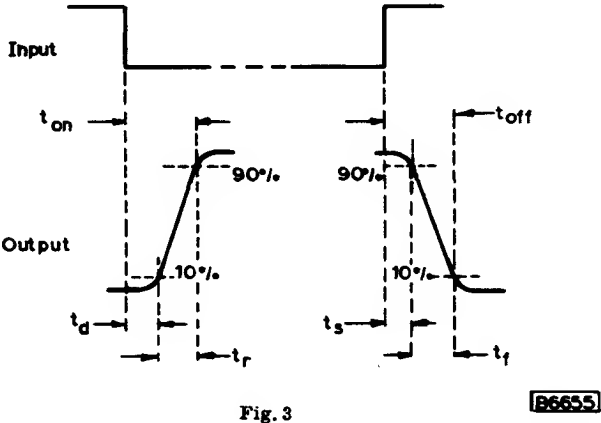


Fig. 3

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2907 2N2907A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

QUICK REFERENCE DATA

	2N2907	2N2907A	
$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C < 100\text{mA}$)	40	60	V
$-I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^\circ\text{C}$)		400	mW
T_j max.		200	$^\circ\text{C}$
h_{FE} ($-I_C = 150\text{mA}$, $-V_{CE} = 10\text{V}$)		100-300	
f_T min. ($-I_C = 50\text{mA}$, $f = 100\text{MHz}$)		200	MHz
t_s max. ($-I_{CS} = 150\text{mA}$, $-I_B = +I_{BM} = 15\text{mA}$)		80	ns

Unless otherwise stated data is applicable to both types

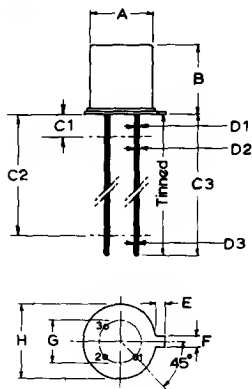
OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-18

B.S. 3934 SO-12A/SB3-6A

Millimetres

	Min.	Typ.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84



Viewed from underside

Connections 1. Emitter 3. Collector connected to envelope
2. Base

Mullard

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C = 0$ to 100mA)	2N2907	40	V
	2N2907A	60	V
$-V_{EBO}$ max.		5.0	V
$-I_C$ max.		600	mA
P_{tot} max. ($T_{amb} = 25^{\circ}C$)		400	mW

Temperature

T_{stg} min.	-65	$^{\circ}C$
T_{stg} max.	200	$^{\circ}C$
T_j max.	200	$^{\circ}C$

†THERMAL CHARACTERISTIC

θ_{j-amb}	0.44 degC/mW
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†ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$ unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 50V, I_E = 0$	2N2907	-	20	nA
		2N2907A	-	10	nA
	$-V_{CB} = 50V, I_E = 0,$				
	$T_{amb} = 150^{\circ}C$	2N2907	-	20	μA
		2N2907A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE} = 30V, +V_{BE} = 0.5V$		-	50	nA
I_{BEX}	Base current				
	$-V_{CE} = 30V, +V_{BE} = 0.5V$		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C = 10\mu A, I_E = 0$		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C = 10mA, I_B = 0$	2N2907	40	-	V
		2N2907A	60	-	V

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

†J.E.D.E.C. registered data

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2907 2N2907A

		Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A, I_C = 0$	5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$ $-I_C = 500mA, -I_B = 50mA$	-	0.4 1.6	V V
$-V_{BE(sat)}$	*Base-emitter saturation voltage $-I_C = 150mA, -I_B = 15mA$ $-I_C = 500mA, -I_B = 50mA$	-	1.3 2.6	V V
h_{FE}	Static forward current transfer ratio			
	$-I_C = 0.1mA, -V_{CE} = 10V$	2N2907 35 2N2907A 75	-	
	$-I_C = 1.0mA, -V_{CE} = 10V$	2N2907 50 2N2907A 100	-	
	$-I_C = 10mA, -V_{CE} = 10V$	2N2907 75 2N2907A 100	-	
	* $-I_C = 150mA, -V_{CE} = 10V$	100	300	
	* $-I_C = 500mA, -V_{CE} = 10V$	2N2907 30 2N2907A 50	-	
C_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V, I_E = 0, f = 100kHz$	-	8.0	pF
C_{ib}	Common base, open circuit input capacitance $+V_{BE} = 2.0V, I_C = 0, f = 100kHz$	-	30	pF
f_T	Transition frequency $-V_{CE} = 20V, -I_C = 50mA, f = 100MHz$	200	-	MHz

*Pulse conditions, pulse width = $300\mu A$, duty cycle $\leq 2\%$.

Switching characteristics

Max.

Turn-on (see fig.1)

$$-V_{CC} = 30V, -I_{CS} = 150mA, -I_B = 15mA$$

t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	45	ns

Turn-off (see fig.2)

$$-V_{CC} = 6.0V, -I_{CS} = 150mA, -I_B = +I_{BM} = 15mA$$

t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time ($t_s + t_f$)	100	ns

TEST CIRCUITS

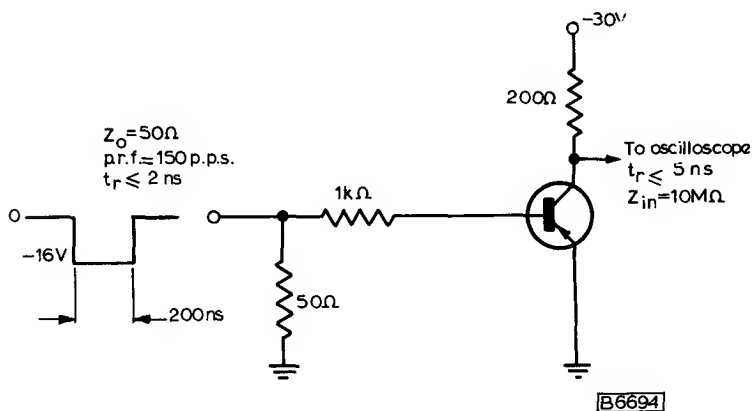


Fig. 1

Test circuit for determining delay, rise and turn-on time

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2907
2N2907A

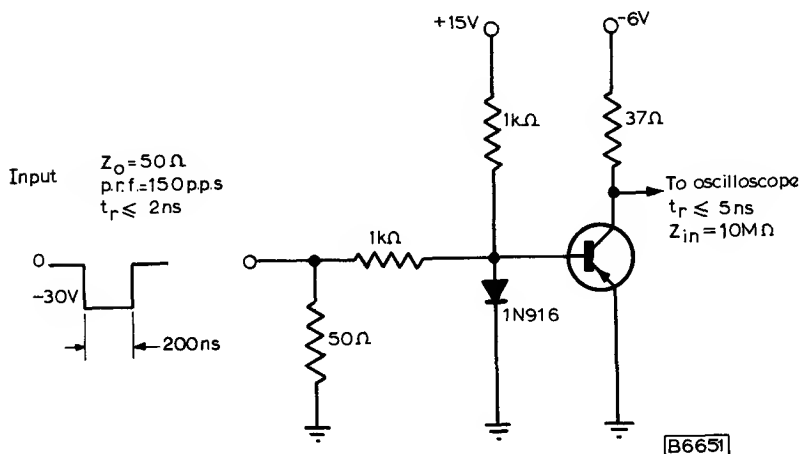


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

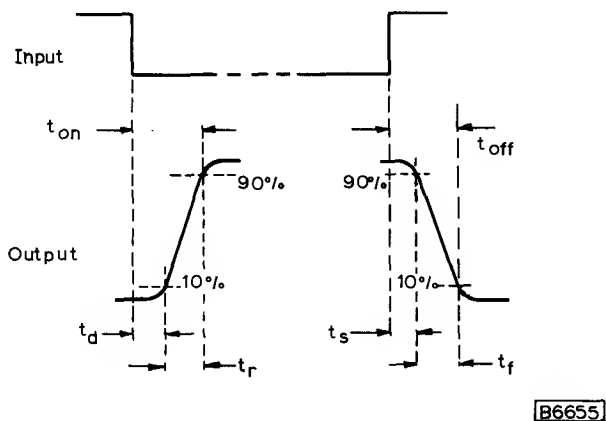


Fig. 3

Mullard

N-P-N SILICON PLANAR TRANSISTOR

2N3053

N-P-N silicon planar transistor designed for medium speed, saturated and nonsaturated switching applications for industrial service.

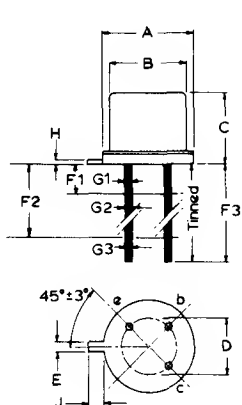
QUICK REFERENCE DATA

V_{CBO} max.	60	V
V_{CEO} max.	40	V
I_C max.	700	mA
P_{tot} max. ($T_{case} = 25^\circ C$)	5.0	W
T_j max.	200	$^\circ C$
h_{FE} ($I_C = 150mA$, $V_{CE} = 10V$)	50-250	
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$, $f = 20MHz$)	100	MHz

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5

Millimetres



	Min.	Nom.	Max.
A	9.10	-	9.39
B	8.20	-	8.50
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

Mullard

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	60	V
$*V_{CEO}$ max.	40	V
V_{EBO} max.	5.0	V
I_C max.	700	mA
P_{tot} max. ($T_{case} = 25^{\circ}C$)	5.0	W

Temperature

T_{stg} min.	-65	$^{\circ}C$
T_{stg} max.	200	$^{\circ}C$
T_j max.	200	$^{\circ}C$

*For $I_C = 0$ to 100mA (pulsed), pulse duration = 300 μ s, duty factor = 1.8%;
0 to 700mA for shorter pulses.

†THERMAL CHARACTERISTIC

Θ_{j-case} (above $25^{\circ}C$)	35	degC/W
--	----	--------

†ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$)

		Min.	Max.
I_{CEX}	Collector-emitter cut-off current $V_{CE} = 60V, -V_{BE} = 1.5V$	-	0.25 μA
$-I_{BEX}$	Base current $V_{CE} = 60V, -V_{BE} = 1.5V$	-	0.25 μA
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 100\mu A, I_E = 0$	60	- V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 100\mu A, I_C = 0$	5.0	- V
	**Collector-emitter breakdown voltage $I_C = 100\mu A, I_B = 0$	40	- V
$V_{(BR)CEO}$		50	- V
$V_{(BR)CER}$	$I_C = 100mA, R_{BE} = 10\Omega$		

**Pulse test, pulse width = 300 μ s, duty factor = 1.8%.

†J.E.D.E.C. registered data.

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Max.
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 150\text{mA}$, $I_B = 15\text{mA}$	-	1.4 V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 150\text{mA}$, $I_B = 15\text{mA}$	-	1.7 V
V_{BE}	Base-emitter voltage $I_C = 150\text{mA}$, $V_{CE} = 2.5\text{V}$	-	1.7 V
h_{FE}	Static forward current transfer ratio $I_C = 150\text{mA}$, $V_{CE} = 2.5\text{V}$	25	-
	** $I_C = 150\text{mA}$, $V_{CE} = 10\text{V}$	50	250
f_T	Transition frequency $I_C = 50\text{mA}$, $V_{CE} = 10\text{V}$, $f = 20\text{MHz}$	100	- MHz
C_{ob}	Output capacitance $V_{CB} = 10\text{V}$, $I_C = 0$, $f = 140\text{kHz}$	-	15 pF
C_{ib}	Input capacitance $V_{EB} = 0.5\text{V}$, $I_E = 0$, $f = 140\text{kHz}$	-	80 pF

**Pulse test, pulse width = 300 μ s, duty factor = 1.8%.

N-P-N SILICON DIFFUSED POWER TRANSISTOR

2N3055

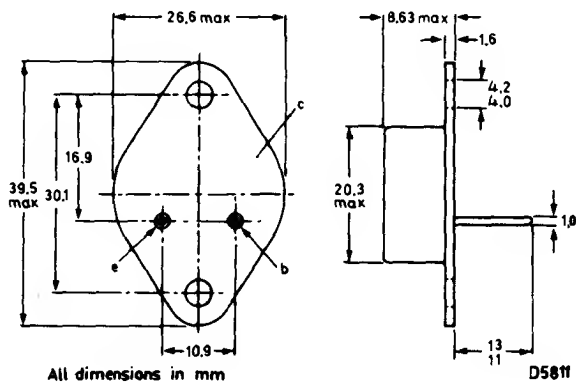
N-P-N silicon diffused power transistor, intended for high quality amplifiers, power supplies, inverters and similar industrial applications.

QUICK REFERENCE DATA

V_{CBO} max.	100	V
V_{CER} max. ($R_{BE} = 100\Omega$)	70	V
I_C max.	15	A
P_{tot} max. ($T_{mb} \leq 25^\circ\text{C}$)	115	W
T_j max.	200	$^\circ\text{C}$
h_{FE} ($I_C = 4.0\text{A}$, $V_{CE} = 4.0\text{V}$)	20-70	
f_T min. ($I_C = 1.0\text{A}$, $V_{CE} = 4.0\text{V}$, $f = 1.0\text{MHz}$)	0.8	MHz

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-5B/SB2-2
J.E.D.E.C. TO-3



Collector connected to envelope

Accessories available: 56239A (insulating bush), 56201B (mica washer),
56214 (lead washer)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	100	V
V_{CER} max. ($R_{BE} = 100\Omega$)	70	V
V_{EBO} max.	7.0	V
I_C max.	15	A
I_B max.	7.0	A
P_{tot} max. ($T_{mb} \leq 25^\circ C$)	115	W

Temperature

T_{stg} range	-65 to +200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	1.5	degC/W
----------------	-----	--------

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Max.	
I_{CEO}	Collector cut-off current			
	$V_{CE} = 30V, I_B = 0$	-	0.7	mA
I_{CEX}	$V_{CE} = 100V, -V_{BE} = 1.5V$	-	5.0	mA
I_{CEX}	$V_{CE} = 100V, -V_{BE} = 1.5V,$			
	$T_j = 150^\circ C$	-	10	mA
I_{EBO}	Emitter cut-off current			
	$V_{EB} = 7.0V, I_C = 0$	-	5.0	mA
$V_{CEO(sust)}$	Collector-emitter sustaining voltage			
	$I_C = 0.2A, I_B = 0$	60	-	V
$V_{CER(sust)}$	$I_C = 0.2A, R_{BE} = 100\Omega$	70	-	V
V_{BE}	Base-emitter voltage			
	$I_C = 4.0A, V_{CE} = 4.0V$	-	1.8	V
$V_{CE(sat)}$	Collector-emitter saturation voltage			
	$I_C = 4.0A, I_B = 0.4A$	-	1.1	V
	$I_C = 10A, I_B = 3.3A$	-	4.0	V

N-P-N SILICON DIFFUSED POWER TRANSISTOR

2N3055

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Max.
h_{FE}	Static forward current transfer ratio $I_C = 4.0A, V_{CE} = 4.0V$	20	70
f_T	Transition frequency $I_C = 1.0A, V_{CE} = 4.0V,$ $f = 1.0MHz$	0.8	~ MHz
h_{fe}	Small signal forward current transfer ratio $I_C = 1.0A, V_{CE} = 4.0V,$ $f = 1.0kHz$	15	-

SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632

The 2N3553, 2N3375, and 2N3632 are silicon power transistors. The 2N3553 and 2N3375 are designed for v.h.f./u.h.f. application and the 2N3632 for v.h.f. application in industrial and military transmitting equipment.

QUICK REFERENCE DATA

	2N3553	2N3375	2N3632	
V_{CB0} max.	65	65	65	V
V_{CE0} max.	40	40	40	V
I_{CM} max.	1.0	1.5	3.0	A
P_{tot} max. ($T_{mb} \leq 25^{\circ}C$)	7.0	11.6	23	W
T_j max. (operating)	200	200	200	$^{\circ}C$
f_T typ.	500	500	400	MHz
Output power				
at $V_{CE} = 28V$, common emitter				
P_{out} min. ($P_{in} = 0.25W$, $f = 175MHz$)	2.5	—	—	W
P_{out} min. ($P_{in} = 1.0W$, $f = 100MHz$)	—	7.5	—	W
P_{out} min. ($P_{in} = 1.0W$, $f = 400MHz$)	—	3.0	—	W
P_{out} min. ($P_{in} = 3.5W$, $f = 175MHz$)	—	—	13.5	W

OUTLINE AND DIMENSIONS

For details see page D4.

2N3553 Conforms to J.E.D.E.C. TO-39, B.S. 3934 SO-3/SB3-3B
2N3375 and 2N3632 Conform to J.E.D.E.C. TO-60

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	2N3553	2N3375	2N3632	
V_{CBO} max.	65	65	65	V
V_{CEO} max.	40	40	40	V
V_{EBO} max.	4.0	4.0	4.0	V
I_C max.	0.35	0.5	1.0	A
I_{CM} max.	1.0	1.5	3.0	A
P_{tot} max. ($T_{mb} \leq 25^\circ\text{C}$)	7.0	11.6	23	W

Temperature

T_{stg} min.			-65	$^\circ\text{C}$
T_{stg} max.			+200	$^\circ\text{C}$
T_j max. (operating)			+200	$^\circ\text{C}$

*See safe operation area curves on pages C1 and C2

THERMAL CHARACTERISTICS

θ_{j-mb}	25	15	7.5 degC/W
θ_{mb-h}	—	0.6	0.6 degC/W
θ_{mb-h} (mounted with top clamping washer of accessory 56218)	1.0	—	— degC/W
θ_{mb-h} (mounted with top clamping washer of accessory 56218 and a Boron nitride washer for electrical insulation)	1.2	—	— degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$)

$V_{(BR)CBO}$ min.	Collector-base breakdown voltage $I_C = 250\mu\text{A}$, $I_E = 0$	65	65	65	V
$V_{(BR)CEX}$ min.**	Collector-emitter breakdown voltage $I_C = 0$ to 200mA, $V_{EB} = 1.5\text{V}$, $R_B = 33\Omega$	65	65	65	V
$V_{(BR)CEO}$ min.**	$I_C = 0$ to 200mA, $I_B = 0$	40	40	40	V
$V_{(BR)EBO}$ min.	Emitter-base breakdown voltage $I_E = 250\mu\text{A}$, $I_C = 0$	4.0	4.0	4.0	V
I_{CEO} max.	Collector cut-off current $V_{CE} = 30\text{V}$, $I_B = 0$	100	100	250	μA
h_{FE}	Large signal forward current transfer ratio $I_C = 125\text{mA}$, $V_{CE} = 5.0\text{V}$				
	min.	15	15	—	
	max.	200	200	—	
	$I_C = 250\text{mA}$, $V_{CE} = 5.0\text{V}$				
	min.	10	10	10	
	max.	100	100	150	
	$I_C = 1000\text{mA}$, $V_{CE} = 5.0\text{V}$				
	min.	—	—	5	
	max.	—	—	110	

**Pulsed through an inductor (25mH); $\delta = 0.5$; $f = 50\text{Hz}$.

SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$)

		2N3553	2N3375	2N3632	
V_{BE}	Base-Emitter Voltage (max.)				
	$I_C = 250\text{mA}$, $V_{CE} = 5\text{V}$	1.5	—	—	V
	$I_C = 500\text{mA}$, $V_{CE} = 5\text{V}$	—	1.5	—	V
	$I_C = 1000\text{mA}$, $V_{CE} = 5\text{V}$	—	—	1.5	V
$V_{CE(\text{Sat})}$	Collector-emitter saturation voltage (max.)				
	$I_C = 250\text{mA}$, $I_B = 50\text{mA}$	1.0	—	—	V
	$I_C = 500\text{mA}$, $I_B = 100\text{mA}$	—	1.0	—	V
	$I_C = 1000\text{mA}$, $I_B = 200\text{mA}$	—	—	1.0	V
f_T typ.	Transition frequency				
	$V_{CE} = 28\text{V}$, $I_C = 125\text{mA}$	500	500	—	MHz
	$I_C = 500\text{mA}$	—	—	400	MHz
C_{tc}	Collector capacitance				
	$V_{CB} = 28\text{V}$, $I_E = I_C = 0$, $f = 1\text{MHz}$ (max.)	10	10	20	pF
C_C	Collector-case capacitance (max.)	—	6.0	6.0	pF
$R_{e(\text{hie})}$	Real part of input impedance				
	$f = 200\text{MHz}$, $I_C = 125\text{mA}$, $V_{CE} = 28\text{V}$ (max.)	20	20	—	Ω
	$f = 200\text{MHz}$, $I_C = 250\text{mA}$, $V_{CE} = 28\text{V}$ (max.)	—	—	20	Ω

R.F. Performance

in un-neutralised common emitter amplifier

$V_{CE} = 28\text{V}$

Type	Freq.	Power out	Power in	I_C	η	Circuit No.
2N3553	175MHz	2.5W	<0.25W	<180mA	>50%	fig 2
2N3375	100MHz	7.5W	<1.0W	<410mA	>65%	fig 1
2N3375	400MHz	>3.0W	1.0W	270mA	>40%	fig 3
2N3632	175MHz	>13.5W	3.5W	690mA	>70%	fig 2

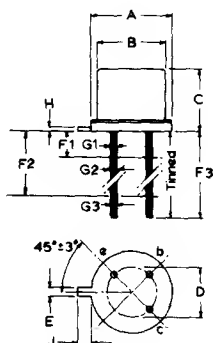
The transistors can withstand an output V.S. W.R. of 3 : 1 varied through all phases for the conditions mentioned in the above table.

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OUTLINE AND DIMENSIONS FOR 2N3553

Conforms to J.E.D.E.C. TO-39

B.S.3934 SO-3/SB3-3B

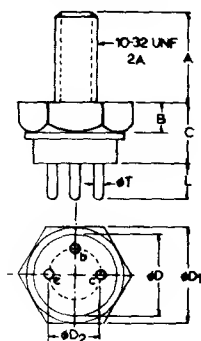


	Millimetres		
	Min.	Nom.	Max.
A	8.64	8.9	9.4
B	7.75	8.15	8.5
C	6.1	6.36	6.6
D	—	5.08	—
E	0.71	0.79	0.86
F	13	—	—
H	—	0.4	—
J	0.74	0.85	1.0

Collector connected to case

OUTLINE AND DIMENSIONS FOR 2N3375, 2N3632

Conforms to TO-60



	Millimetres	
	Nom.	
A	11.10	
B	3.18	
C	6.86	
ϕD	8.38	
ϕD_1	10.92	
ϕD_2	5.08	
L	3.81	
ϕT	0.97	

SOLDERING AND WIRING RECOMMENDATIONS (2N3553)

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated, flux.

NOTES (2N3375, 2N3632)

1. A heatsink thermal resistance of 3degC/W is recommended for operation in ambient temperature up to 65°C.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled. Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they **MUST NOT** be sent through the post. In this case advice is available from the Service Department.

Service Department,
Mullard Limited,
New Road,
Mitcham,
Surrey.

COMMON EMITTER TEST CIRCUIT 100MHz 2N3375

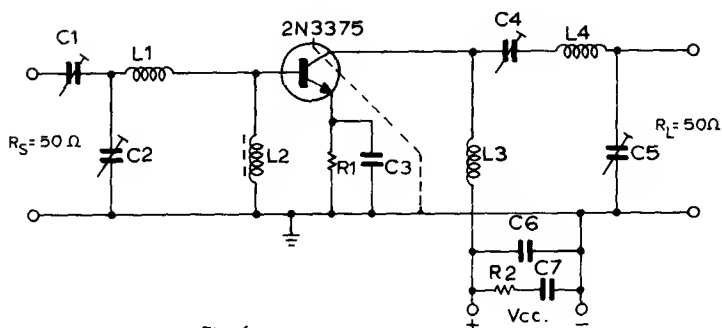


Fig. 1

$C_1 = 3,5-61,5\text{pF}$	air trimmer.
$C_2 = 3,5-61,5\text{pF}$	air trimmer.
$C_3 = 10\text{nF}$	polyester.
$C_4 = 4-29\text{pF}$	air trimmer.
$C_5 = 4-29\text{pF}$	air trimmer.
$C_6 = 330\text{pF}$	ceramic.
$C_7 = 10\mu\text{F}$	polyester.

$L_1 = 2$ turns of 1.5mm closely wound enamelled Cu wire, int. diam. 10mm, leads: $2 \times 10\text{mm}$.

$L_2 =$ Ferroxcube choke coil, Z (at 100MHz) = $700\Omega \pm 20\%$.

$L_3 = 23$ turns of 0.7mm closely wound enamelled Cu wire, int. diam. 6mm.

$L_4 = 5$ turns of 1.5mm closely wound enamelled Cu wire, int. diam. 12mm, leads: $2 \times 10\text{mm}$.

$R_1 = 1.35\Omega$ carbon.

$R_2 = 10\Omega$ carbon.

COMMON EMITTER TEST CIRCUIT 175MHz 2N3553, 2N3632

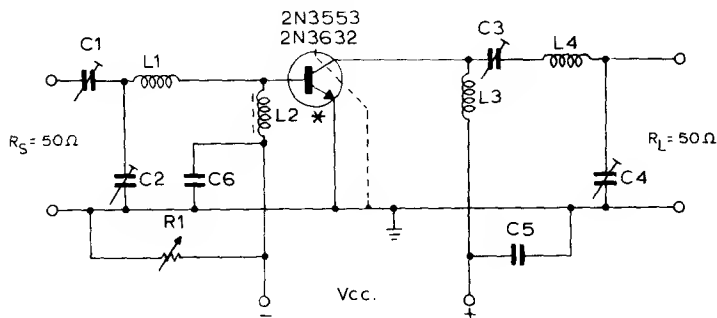


Fig. 2

$\left. \begin{matrix} C_1 \\ C_2 \\ C_3 \\ C_4 \end{matrix} \right\} \approx 4-29\text{pF}$ air trimmer.

$C_5 = 10\text{nF}$ polyester.

$C_6 = 100\text{pF}$ ceramic.

$L_1 = 1$ turn of 1mm Cu wire, int. diam. 10mm; Leads: $2 \times 10\text{mm}$.

$L_2 =$ Ferroxcube choke coil. Z (at 175MHz) $= 550\Omega \pm 20\%$.

$L_3 = 15$ turns of 0.7mm closely wound enamelled Cu wire, int. diam 4mm.

$L_4 = 3$ turns of 1.5mm closely wound enamelled Cu wire, int. diam 12mm, Leads: $2 \times 20\text{mm}$.

$R = 0-2\Omega$ for 2N3632 and $R = 0\Omega$ for 2N3553.

*Emitter of the 2N3632 is connected to case as short as possible. The length of the external emitter wire of the 2N3553 is 1.6mm.

COMMON EMITTER TEST CIRCUIT 400MHz 2N3375

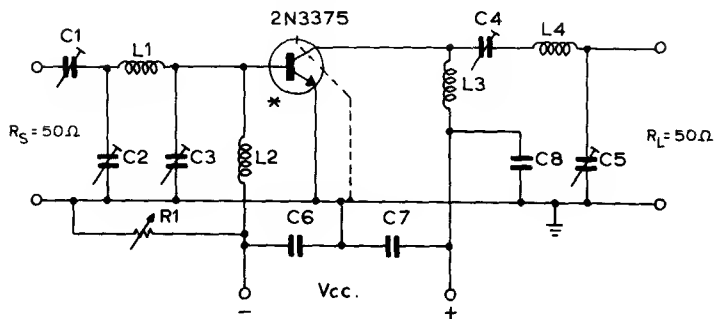


Fig. 3

$C_1 = 0.7-6.7\text{pF}$	ceramic trimmer.
$C_2 = 0.7-6.7\text{pF}$	ceramic trimmer.
$C_3 = 0.5-3.5\text{pF}$	ceramic trimmer.
$C_4 = 3-19\text{pF}$	air trimmer.
$C_5 = 3-19\text{pF}$	air trimmer.
$C_6 = 15\text{pF}$	ceramic.
$C_7 = 15\text{pF}$	ceramic.
$C_8 = 4700\text{pF}$	ceramic.

$L_1 = 20\text{mm}$ straight Cu wire diam. 1.5mm, spaced 8mm from chassis.

$L_2 = 17$ turns of 0.5mm closely wound enamelled Cu wire, int. diam. 3mm.

$L_3 = 7$ turns of 0.5mm closely wound enamelled Cu wire, int. diam. 3mm.

$L_4 = 1$ turn of 1.5mm Cu wire, int. diam. 10mm, leads: $2 \times 5\text{mm}$.

$R = 0-5\Omega$.

*Emitter connected to case as short as possible.

FREQUENCY DOUBLER TEST CIRCUIT 87.5MHz-175MHz 2N3553

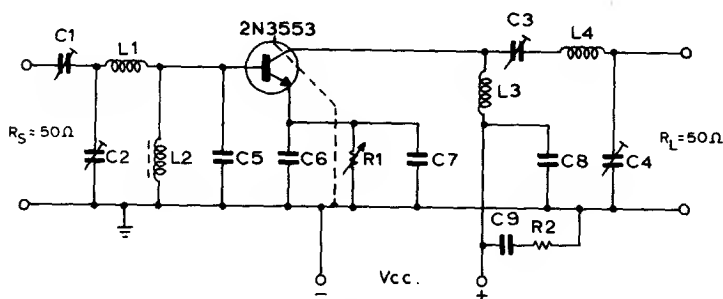


Fig. 4

$\left. \begin{matrix} C_1 \\ C_2 \\ C_3 \end{matrix} \right\} = 4-29\text{pF}$ air trimmer.

$C_4 = 3.5-61.5\text{pF}$ air trimmer.

$C_5 = 56\text{pF}$ ceramic.

$C_6 = 680\text{pF}$ ceramic.

$C_7 = 150\text{pF}$ ceramic.

$C_8 = 100\text{pF}$ ceramic.

$C_9 = 10\text{nF}$ polyester.

$L_1 = 5$ turns of 1mm Cu wire, winding pitch 1.5mm, int. diam. 6mm,
Leads: $2 \times 12\text{mm}$.

$L_2 =$ Ferroxcube choke coil, Z (at 87.5MHz) $= 750\Omega \pm 20\%$.

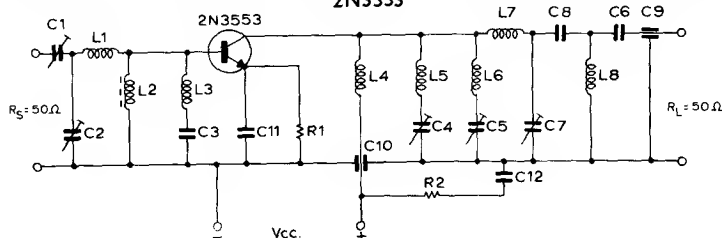
$L_3 = 15$ turns of 0.7mm closely wound enamelled Cu wire, int. diam. 4mm.

$L_4 = 6$ turns of 1mm Cu wire, winding pitch 1.5mm, int. diam. 6mm,
leads: $2 \times 12\text{mm}$.

$R_1 = 0-50\Omega$.

$R_2 = 10\Omega$ carbon.

PARAMETRIC FREQUENCY TREBLER TEST CIRCUIT 156.7MHz-470MH 2N3553



*Tuned to second harmonic frequency.

Fig. 5

C_1		$C_8 = 1\text{pF}$	ceramic.	} feed through.
C_2	} 4-29pF	$C_9 = 12\text{pF}$	ceramic.	
C_3		$C_{10} = 100\text{pF}$	ceramic.	
C_4		$C_{11} = 1000\text{pF}$	ceramic.	
C_5	} 4-10.4pF	$C_{12} = 15\text{nF}$	polyester.	
C_6		$R_1 = 2.2\Omega$	carbon.	
C_7		$R_2 = 10\Omega$	carbon.	

$L_1 = 35\text{mm}$ straight Cu wire, diam. 1mm, spaced 5.5mm from chassis.

$L_2 =$ Ferroxcube choke coil, Z (at 156,7MHz) = $600\Omega \pm 20\%$.

$L_3 = 18\text{mm}$ straight Cu wire, diam. 1mm, spaced 5.5mm from chassis.

$L_4 = 7$ turns of 0.5mm closely wound enamelled Cu wire, int. diam. 3.5mm.

$L_5 = 3$ turns of 1mm Cu wire, winding pitch 1.7mm, int. diam. 8.5mm, leads: $2 \times 10\text{mm}$.

$L_6 = 2$ turns of 1mm Cu wire, winding pitch 1.7mm, int. diam. 7mm, leads: $2 \times 10\text{mm}$.

$L_7 = 40\text{mm}$ straight Cu wire, diam. 1.5mm spaced 5.5mm from chassis.

$L_8 = 1$ turn of 1mm Cu wire, int. diam. 7mm, leads: $2 \times 5\text{mm}$.

Performance

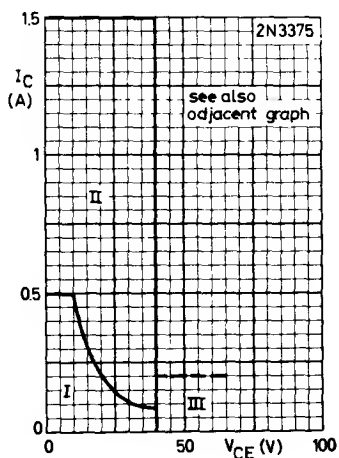
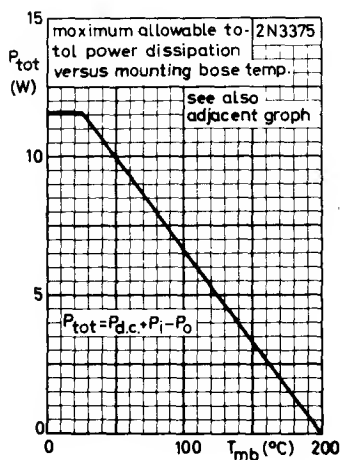
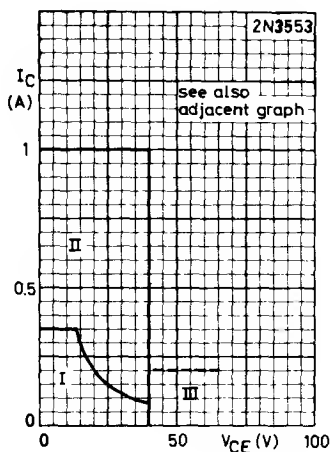
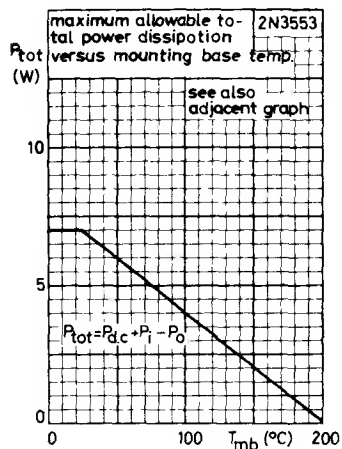
Typical performance at a supply voltage of 28V.

P_o	P_i	G	I_c	η
(W)	(W)	(dB)	(mA)	(%)
1.5	0.27	7.5	125	43
2.0	0.39	7.1	156	46

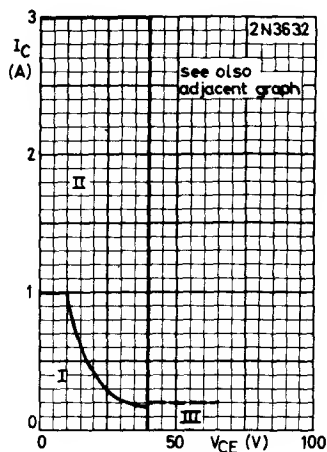
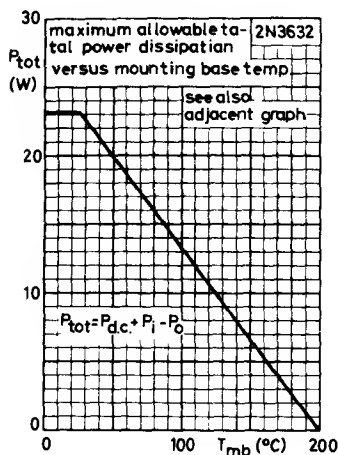
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SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632



Mullard

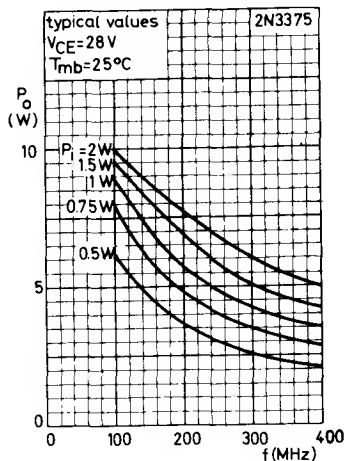
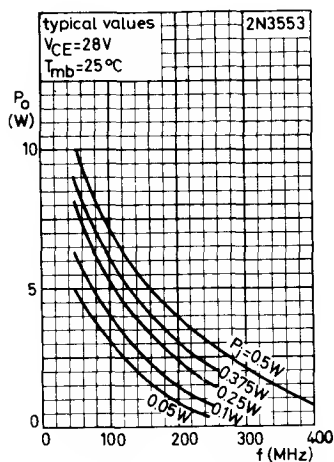


EXPLANATION OF AREAS OF SAFE OPERATION

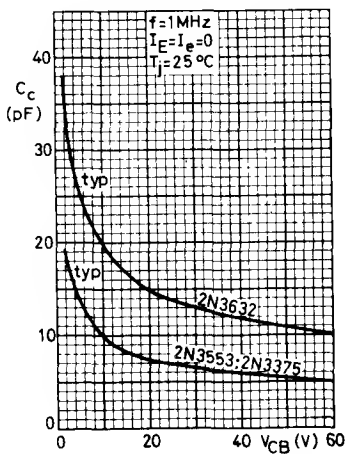
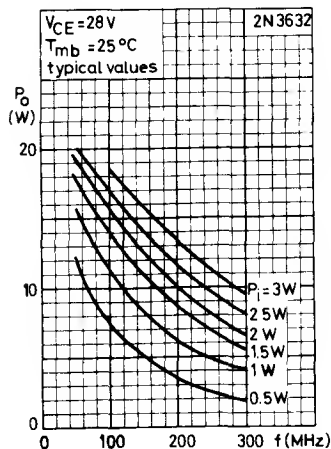
- Region I Operation is allowed under all base-emitter conditions, provided no limiting values are exceeded (d.c. and a.c. operation).
- Region II Operating is allowed under all base-emitter conditions with frequencies $\geq 1\text{MHz}$, provided no limiting values are exceeded. Care must be taken to reduce the d.c. adjustment to region I before removing the a.c. signal. This may be achieved by an appropriate bias in class A, B or C.
- Region III Operating during switching-off in this region is allowed, provided the transistor is cut-off with $-V_{BE} \leq 1.5\text{V}$ and $R_{BE} \geq 33\Omega$, $I_C \leq 400\text{mA}$ and the transient energy does not exceed 2mWs .

SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632



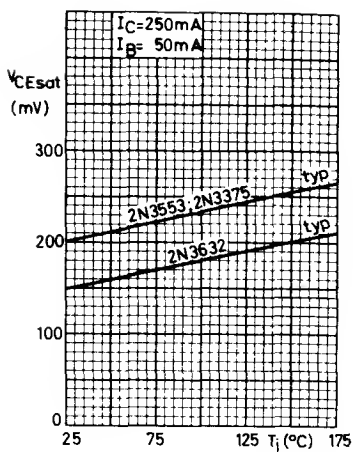
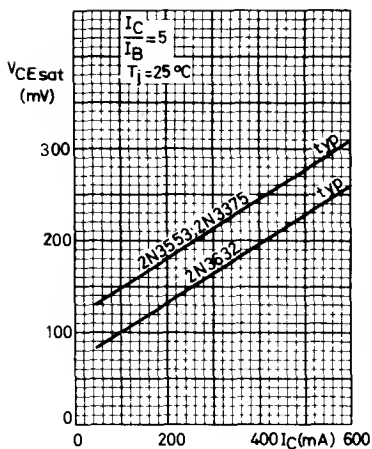
TYPICAL OUTPUT POWER PLOTTED AGAINST FREQUENCY



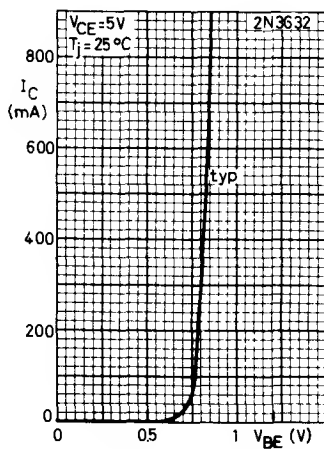
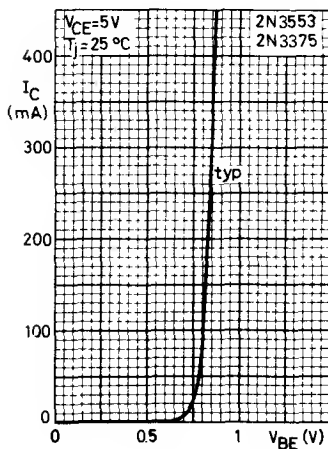
TYPICAL OUTPUT POWER PLOT-
TED AGAINST FREQUENCY

TYPICAL COLLECTOR CAPACIT-
ANCE PLOTTED AGAINST COL-
LECTOR-BASE VOLTAGE

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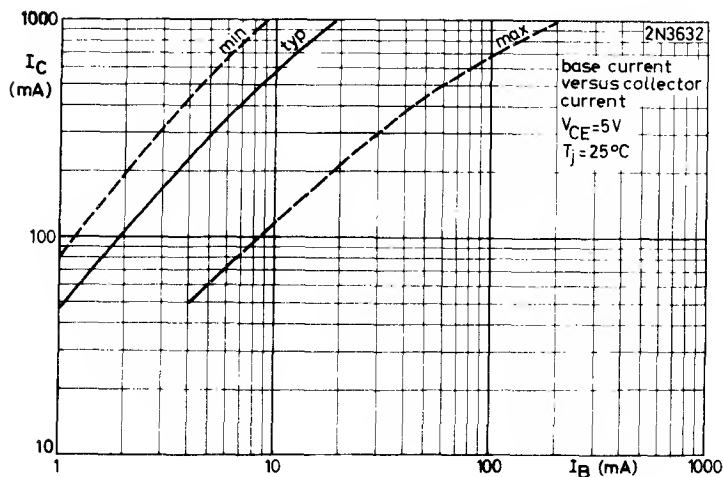
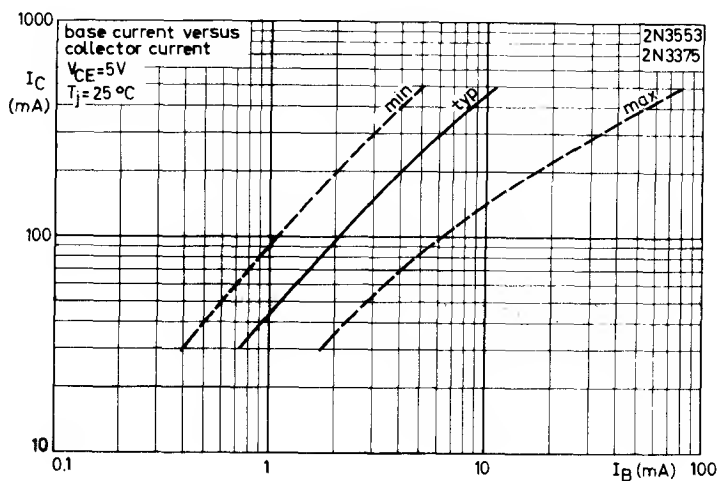
TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL COLLECTOR CURRENT PLOTTED AGAINST BASE-
EMITTER VOLTAGE

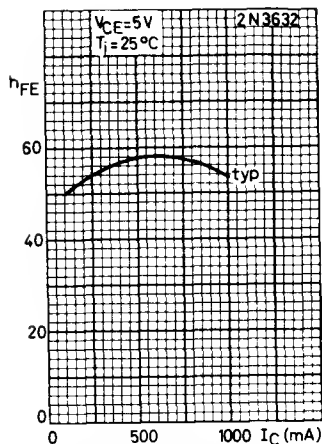
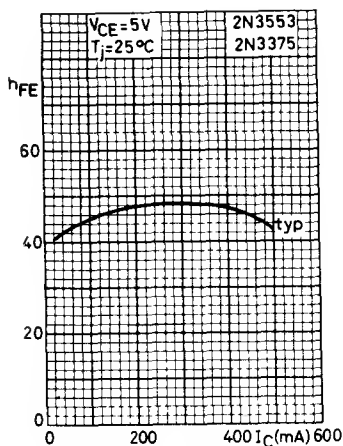
SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632

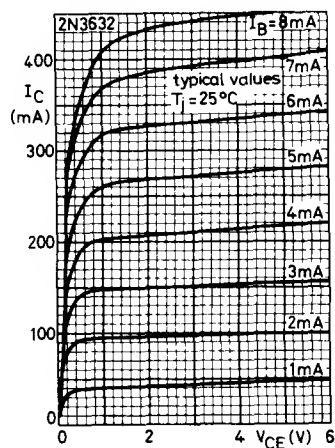
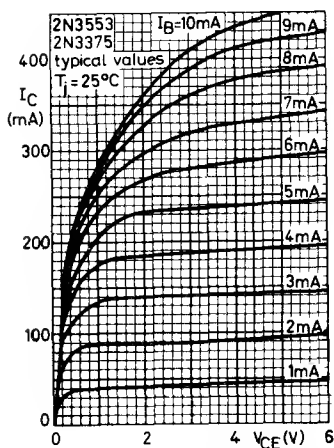


COLLECTOR CURRENT PLOTTED AGAINST BASE CURRENT

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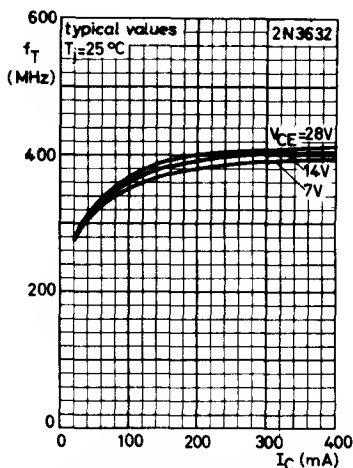
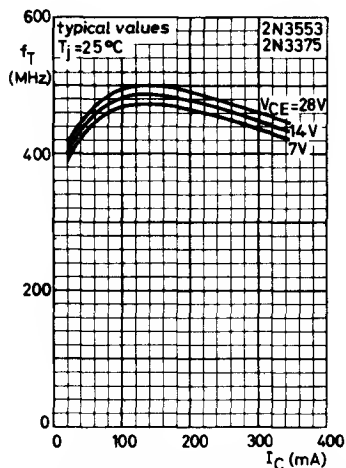
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT



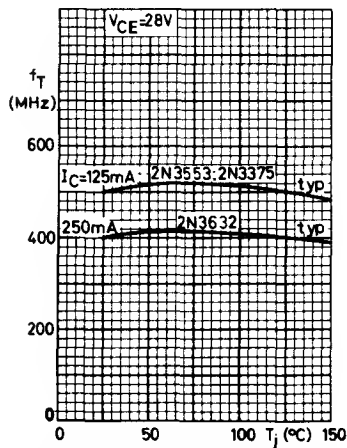
COLLECTOR CURRENT PLOTTED AGAINST COLLECTOR-EMITTER VOLTAGE WITH BASE CURRENT AS A PARAMETER

SILICON V.H.F. N-P-N POWER TRANSISTORS

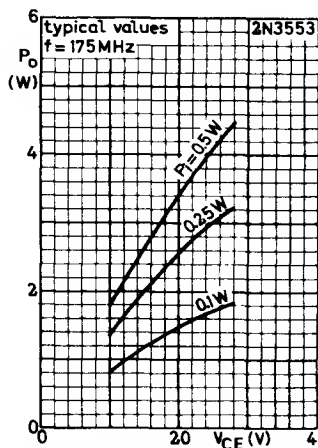
2N3375
2N3553
2N3632



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST
COLLECTOR CURRENT WITH COLLECTOR-EMITTER VOLT-
AGE AS A PARAMETER

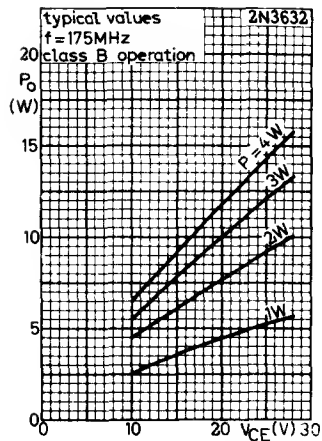
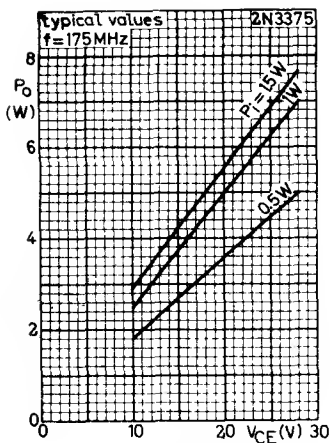


TYPICAL TRANSITION FRE-
QUENCY PLOTTED AGAINST
JUNCTION TEMPERATURE

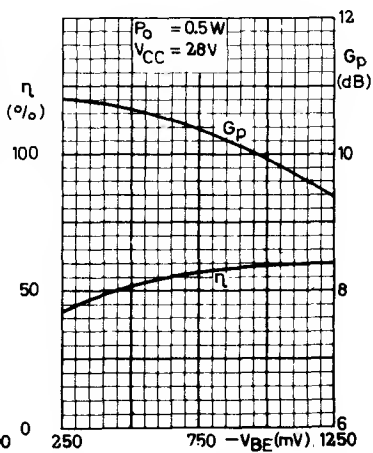
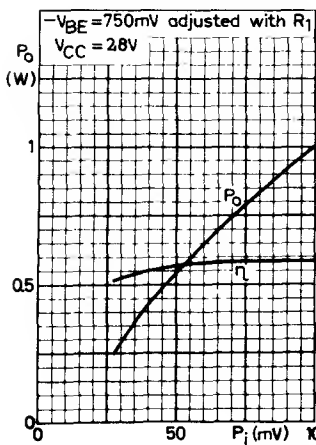


OUTPUT POWER PLOTTED
AGAINST COLLECTOR-EMITTER
VOLTAGE WITH INPUT POWER
AS A PARAMETER

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OUTPUT POWER PLOTTED AGAINST COLLECTOR-EMITTER VOLTAGE WITH INPUT POWER AS A PARAMETER



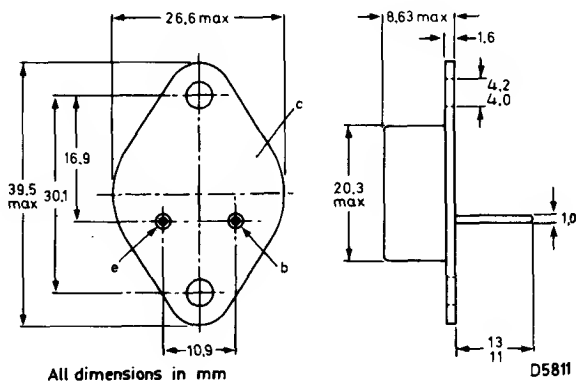
POWER GAIN, POWER OUTPUT, AND EFFICIENCY CURVES PLOTTED AGAINST INPUT POWER AND BASE-EMITTER VOLTAGE FOR DOUBLER CIRCUIT ON PAGE D9

2N3442
2N4347

QUICK REFERENCE DATA

	2N3442	2N4347	
$V_{CBO} \text{ max.}$	160	140	V
$V_{CEO} \text{ max.}$	140	120	V
$I_C \text{ max.}$	10	5	A
$P_{tot} \text{ max. (T}_{mb} \leq 25^{\circ}\text{C)}$	117	100	W
$T_j \text{ max.}$	200	200	$^{\circ}\text{C}$
$h_{FE} \text{ min., } I_C = 3A, V_{CE} = 4V$	20-70	-	
$I_C = 2A, V_{CE} = 4V$	-	20-70	

Conforms to B.S. 3934 SO-5B /SB2-2
J.E.D.E.C. TO-3



Accessories available: 56239A (insulating bush), 56201B (mica washer), 56214 (lead washer)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical	2N3442	2N4347	
$V_{CBO} \text{ max.}$	160	140	V
$V_{CEO} \text{ max.}$	140	120	V
$V_{CER} \text{ max. (} R_{BE} = 100\Omega \text{)}$	150	130	V
$V_{EBO} \text{ max.}$	7.0	7.0	V
$I_C \text{ max.}$	10	5.0	A
$I_{CM} \text{ max.}$	15	10	A
$I_B \text{ max.}$	7.0	3.0	A
$P_{tot} \text{ max. (} T_{mb} \leq 25^\circ\text{C} \text{)}$	117	100	W
Temperature			
T_{stg}	-65 to +200		$^\circ\text{C}$
$T_j \text{ max.}$	200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$	Thermal resistance, junction to mounting-base	1.5	1.75	degC/W
$R_{th(mb-h)}$	Thermal resistance, mounting-base to heatsink		0.5	degC/W
$R_{th(mb-h)}$	Thermal resistance, mounting-base to heatsink with accessories 56201, 56214		0.75	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

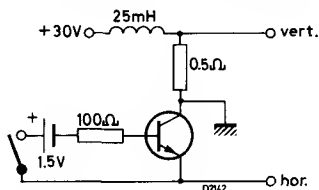
		Min.	Typ.	Max.	
I_{CBO}	Collector-base cut-off current $I_E = 0, V_{CB} = 140\text{V}$	-	50	1000	μA
I_{CEX}	Collector-emitter cut-off current				
	$-V_{BE} = 1.5\text{V}, V_{CE} = 140\text{V}$	2N3442 -	5.0	1000	μA
	$-V_{BE} = 1.5\text{V}, V_{CE} = 140\text{V}, T_{mb} = 150^\circ\text{C}$	2N3442 -	0.1	10	mA
	$-V_{BE} = 1.5\text{V}, V_{CE} = 120\text{V}$	2N3442 -	1.0	-	μA
		2N4347 -	5.0	2000	μA
	$-V_{BE} = 1.5\text{V}, V_{CE} = 120\text{V}, T_{mb} = 150^\circ\text{C}$	2N4347 -	0.1	10	mA
I_{EBO}	Emitter cut-off current $I_C = 0, V_{EB} = 7\text{V}$	-	1.0	5000	μA

N-P-N SILICON DIFFUSED POWER TRANSISTORS

2N3442
2N4347

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.
$V_{(BR)CER}$	Collector-emitter breakdown voltage $I_C = 0.1A, R_{BE} = 100\Omega$	2N3442	150	-	V
		2N4347	130	-	V
$V_{CEO(sust)}$	Collector-emitter sustaining voltage $I_B = 0, I_C = 0.2 \text{ to } 3.0A$	2N3442	140	-	V
		2N4347	120	-	V
$V_{CEX(sust)}$	$-V_{BE} = 1.5V, I_C = 0.1 \text{ to } 1.5A$	2N3442	160	-	V
		2N4347	140	-	V



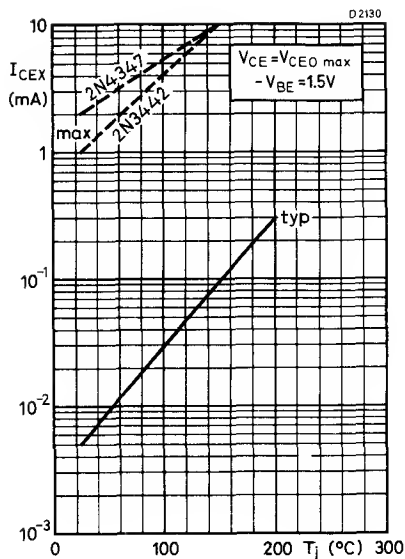
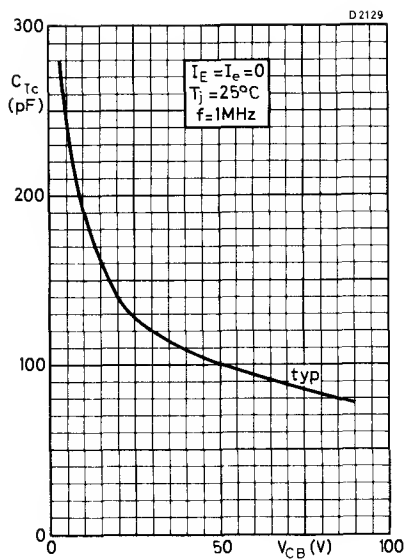
V _{BE}	Base-emitter voltage (t _p = 10ms)					
	I _C = 2.0A, V _{CE} = 4.0V	2N4347	-	0.95	2.0	V
	I _C = 3.0A, V _{CE} = 4.0V	2N3442	-	1.15	1.7	V
	I _C = 5.0A, V _{CE} = 4.0V	2N4347	-	1.55	4.0	V
	I _C = 10A, V _{CE} = 4.0V	2N3442	-	2.8	5.7	V

$V_{CE(sat)}$	Collector-emitter saturation voltage ($t_p=10ms$)					
	$I_C=2.0A, I_B=0.2A$	2N4347	-	-	1.0	V
	$I_C=3.0A, I_B=0.3A$	2N3442	-	-	1.0	V
	$I_C=5.0A, I_B=1.0A$	2N4347	-	-	5.0	V
	$I_C=10A, I_B=2.0A$	2N3442	-	-	5.0	V

h_{FE}	Static forward current transfer ratio ($t_p=10ms$)					
	$I_C=2.0A, V_{CE}=4.0V$	2N4347	20	35	70	
	$I_C=3.0A, V_{CE}=4.0V$	2N3442	20	25	70	
	$I_C=5.0A, V_{CE}=4.0V$	2N4347	7.5	15	-	
	$I_C=10A, V_{CE}=4.0V$	2N3442	7.5	10	-	

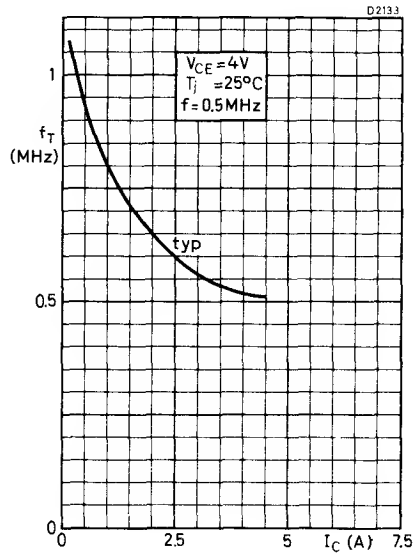
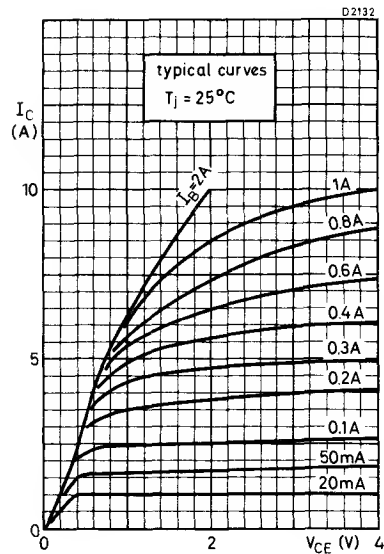
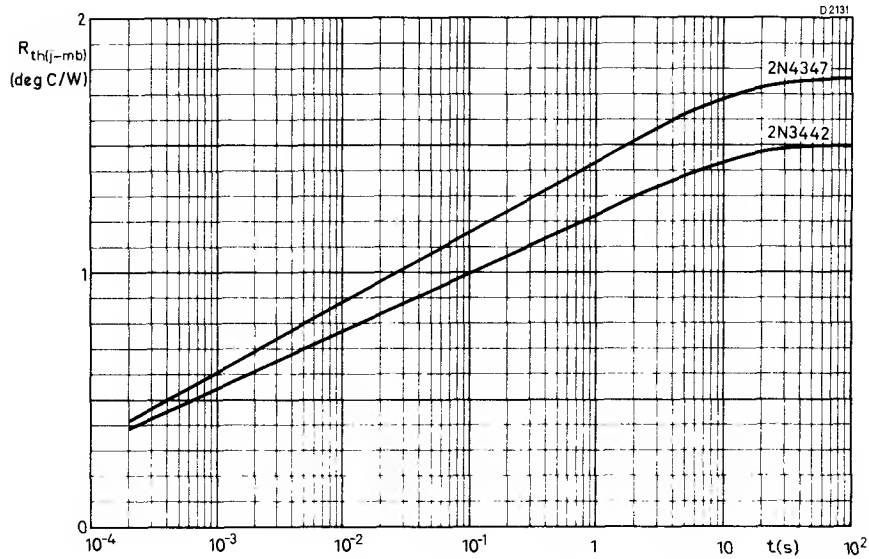
h_{fe}	Small signal current gain				
	$I_C = 2.0A, V_{CE} = 4.0V$				
	$f = 40kHz$	2N3442	2.0	9.5	-
	$f = 1.0kHz$	2N3442	12	18	72

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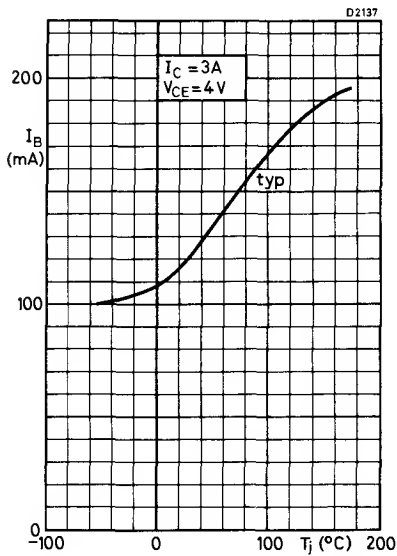
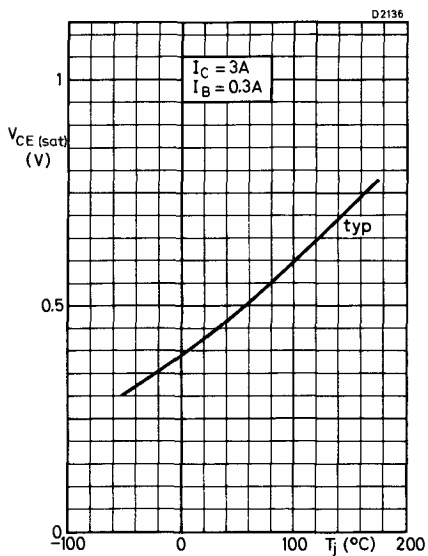
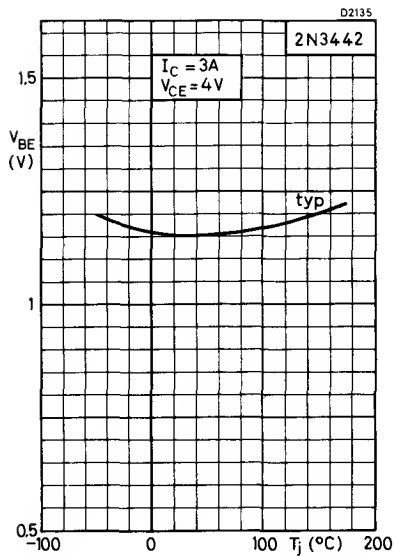
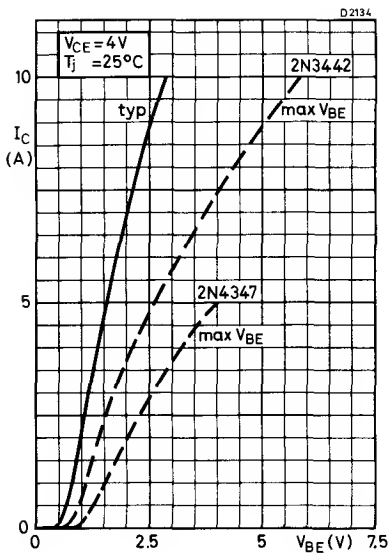


N-P-N SILICON DIFFUSED
POWER TRANSISTORS

2N3442
2N4347

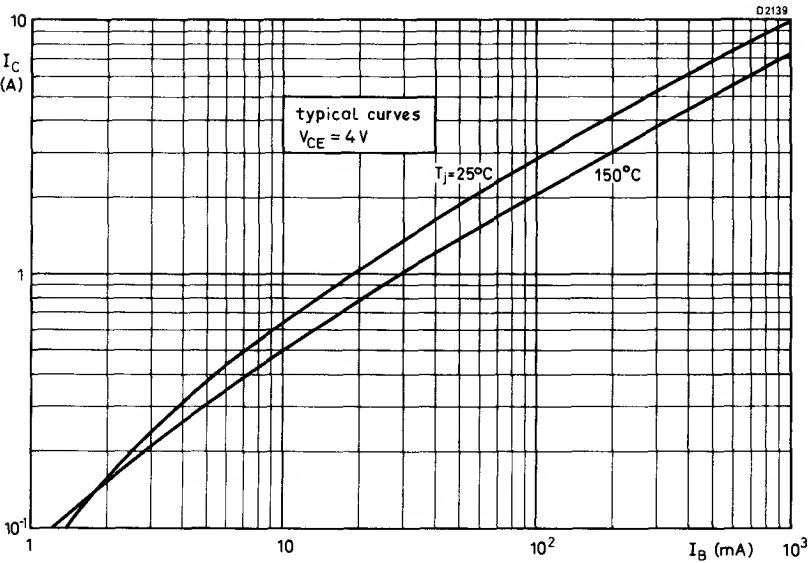
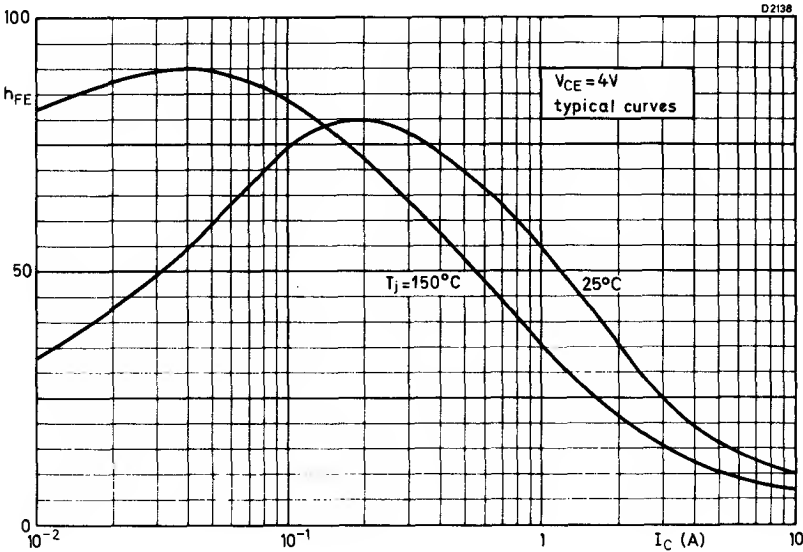


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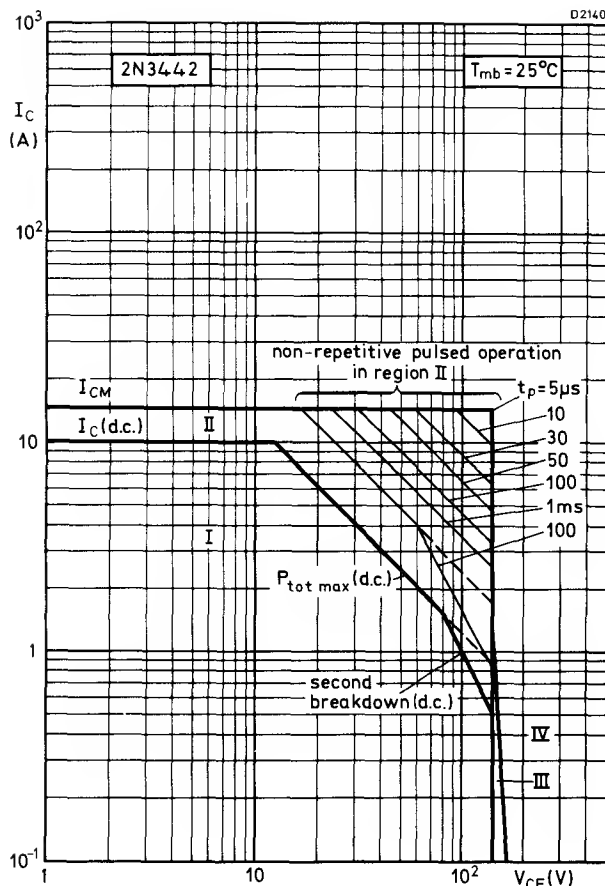


N-P-N SILICON DIFFUSED
POWER TRANSISTORS

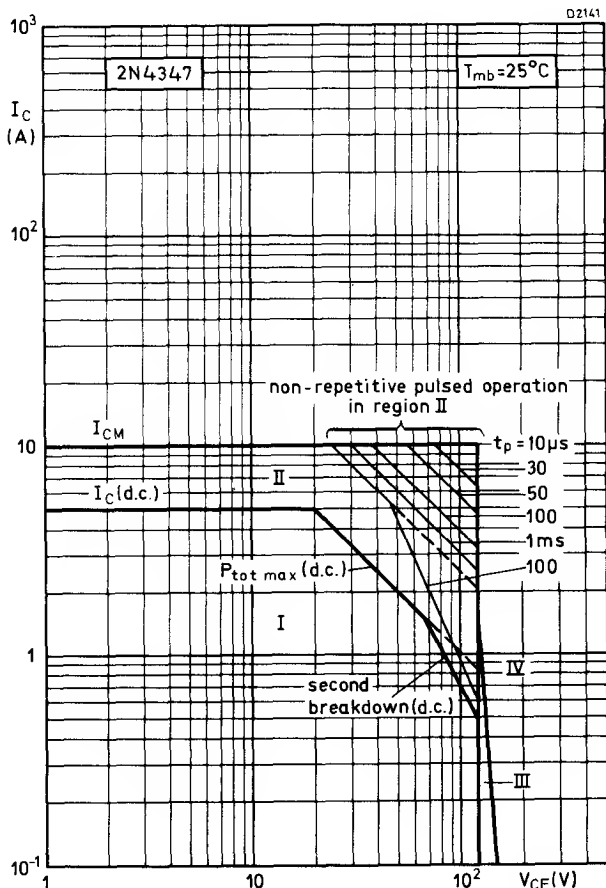
2N3442
2N4347



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- I Region of permissible operation under all base-emitter conditions and at all frequencies, including d.c.
- II Permissible extension for repetitive pulsed operation and non-repetitive pulsed operation. For sinusoidal operation care must be taken to reduce the d.c. adjustment to region I before removing the a.c. signal. This may be achieved by an appropriate bias in class A, B or C.
- III Operation during switching off in this region is allowed, provided the transistor is cut-off with $-V_{BE} \leq 1.5$; $I_{CM} < 1.5\text{A}$.
- IV Operation during switching off is allowed provided the transistor is cut-off with $-V_{BE} \leq 1.5\text{V}$ and the transient energy does not exceed 30mWs.



- I Region of permissible operation under all base-emitter conditions and at all frequencies, including d.c.
- II Permissible extension for repetitive pulsed operation and non-repetitive pulsed operation. For sinusoidal operation care must be taken to reduce the d.c. adjustment to region I before removing the a.c. signal. This may be achieved by an appropriate bias in class A, B or C.
- III Operation during switching off in this region is allowed, provided the transistor is cut-off with $-V_{BE} \leq 1.5\text{V}$; $I_{CM} < 1.5\text{A}$.
- IV Operation during switching off is allowed provided the transistor is cut-off with $-V_{BE} \leq 1.5\text{V}$ and the transient energy does not exceed 30mWs.

**N-P-N SILICON V.H.F.
POWER TRANSISTORS**

**2N3553
2N3632**

For details see data sheet for type 2N3375

Mullard

N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

2N3823

N-channel, depletion-type, silicon planar epitaxial field-effect transistor intended for v.h.f. amplifier and mixer applications in industrial service.

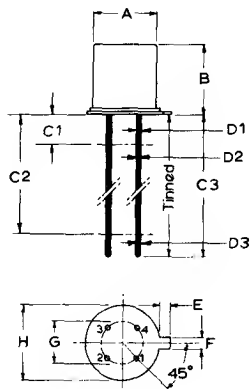
QUICK REFERENCE DATA

V_{DS} max.	30	V
$-V_{GSS}$ max.	30	V
I_{DSS} ($V_{DS}=15V$, $V_{GS}=0$)	4.0 - 20	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	300	mW
C_{rss} max. ($V_{DS}=15V$, $V_{GS}=0$, $f=1.0MHz$)	2.0	pF
$ y_{fs} $ min. ($V_{DS}=15V$, $V_{GS}=0$, $f=200MHz$)	3.2	mmho
N max. ($V_{DS}=15V$, $V_{GS}=0$, $f=100MHz$, $R_G=1.0k\Omega$)	2.5	dB

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72

Millimetres



	Min.	Nom.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Viewed from underside

All electrodes are electrically insulated from the case

Connections

1. Source
2. Drain
3. Gate
4. Case

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DS} max.	30	V
V_{DG} max.	30	V
$-V_{GSS}$ max. ($-I_G = 1.0\mu A$, $V_{DS} = 0$)	30	V
I_G max.	10	mA
P_{tot} max. ($T_{amb} \leq 25^\circ C$)	300	mW

Temperature

T_{stg} range	-65 to +200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	0.59 degC/mW
-----------------	--------------

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise stated)

The fourth lead (case) is connected to the source for all measurements.

		Min.	Max.	
Static				
$-I_{GSS}$	Gate cut-off current			
	$-V_{GS} = 20V$, $V_{DS} = 0$	-	0.5	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_{amb} = 150^\circ C$	-	0.5	μA
I_{DSS}	Zero-gate-voltage drain current			
	$*V_{DS} = 15V$, $V_{GS} = 0$	4.0	20	mA
$-V_{(BR)GSS}$	Gate-source breakdown voltage			
	$-I_G = 1.0\mu A$, $V_{DS} = 0$	30	-	V
$-V_{GS}$	Gate-source voltage			
	$V_{DS} = 15V$, $I_D = 400\mu A$	1.0	7.5	V
$-V_{GS(off)}$	Gate-source cut-off voltage			
	$V_{DS} = 15V$, $I_D = 0.5nA$	-	8.0	V

*Pulse measurements, pulse width = 100ms, duty cycle $\leq 10\%$.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

2N3823

ELECTRICAL CHARACTERISTICS (cont'd)

Small signal y-parameters

Common source, $V_{DS} = 15V$, $V_{GS} = 0$

* $f = 1.0kHz$

Min.

Max.

$ y_{fs} $	Transfer admittance	3.5	6.5 mmho
$ y_{os} $	Output admittance	-	35 μ mho

$f = 1.0MHz$

C_{rss}	Feedback capacitance	-	2.0 pF
C_{iss}	Input capacitance	-	6.0 pF

$f = 200MHz$

$ y_{fs} $	Transfer admittance	3.2	- mmho
g_{is}	Input conductance	-	800 μ mho
g_{os}	Output conductance	-	200 μ mho

Noise

N

Spot noise figure
 $f = 100MHz$, $R_G = 1.0k\Omega$,
 $V_{DS} = 15V$, $V_{GS} = 0$

-

2.5 dB

*Pulse measurements, pulse width = 100ms, duty cycle $\leq 10\%$.

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

2N3866

N-P-N silicon planar epitaxial transistor primarily intended for use in the output, driver and pre-driver stages of class A, B or C amplifiers, frequency multipliers and oscillators of v.h.f. and u.h.f. equipment.

Encapsulated in a metal TO-39 envelope with the collector connected to the case.

QUICK REFERENCE DATA

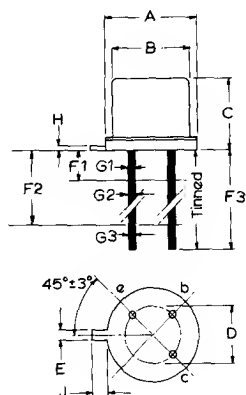
V_{CER} max.	55	V
V_{CEO} max.	30	V
I_C max.	400	mA
P_{tot} max. ($T_{case} \leq 25^\circ C$)	5.0	W
T_j max.	200	$^\circ C$
f_T typ. ($I_C = 25mA$, $V_{CE} = 15V$, $f = 100MHz$)	700	MHz
P_o typ. ($P_i < 100mW$, $V_{CE} = 28V$, $f = 400MHz$)	1.0	W
η min. ($P_o = 1.0W$, $V_{CE} = 28V$, $f = 400MHz$)	45	%

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B

J.E.D.E.C. TO-39

Millimetres



	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	55	V
V_{CER} max. ($R_{BE} = 10\Omega$)	55	V
V_{CEO} max.	30	V
V_{EBO} max.	3.5	V
I_C max.	400	mA
I_{CM} max.	400	mA
P_{tot} max. ($T_{case} \leq 25^\circ C$)	5.0	W

Temperature

T_{stg} min.	-65	$^\circ C$
T_{stg} max.	200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	In free air	200	degC/W
$R_{th(j-case)}$		35	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218	1.0	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CEO}	Collector cut-off current $V_{CE} = 28V, I_B = 0$	-	-	20	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 100\mu A, I_E = 0$	55	-	-	V
	Collector-emitter breakdown voltages				
$V_{(BR)CER}$	$I_C = 5.0mA, R_{BE} = 10\Omega$	55	-	-	V
$V_{(BR)CEO}$	$I_C = 5.0mA, I_B = 0$	30	-	-	V
$V_{(BR)EBO}$	Collector-base breakdown voltage $I_E = 100\mu A, I_C = 0$	3.5	-	-	V

Mullard

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100\text{mA}$, $I_B = 20\text{mA}$	-	-	1.0	V
h_{FE}	Static forward current transfer ratio $I_C = 50\text{mA}$, $V_{CE} = 5.0\text{V}$ $I_C = 360\text{mA}$, $V_{CE} = 5.0\text{V}$	10 5	- -	200 -	
f_T	Transition frequency $I_C = 25\text{mA}$, $V_{CE} = 15\text{V}$, $f = 100\text{MHz}$	-	700	-	MHz
C_{tc}	Collector capacitance $V_{CB} = 28\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	-	3.0	pF

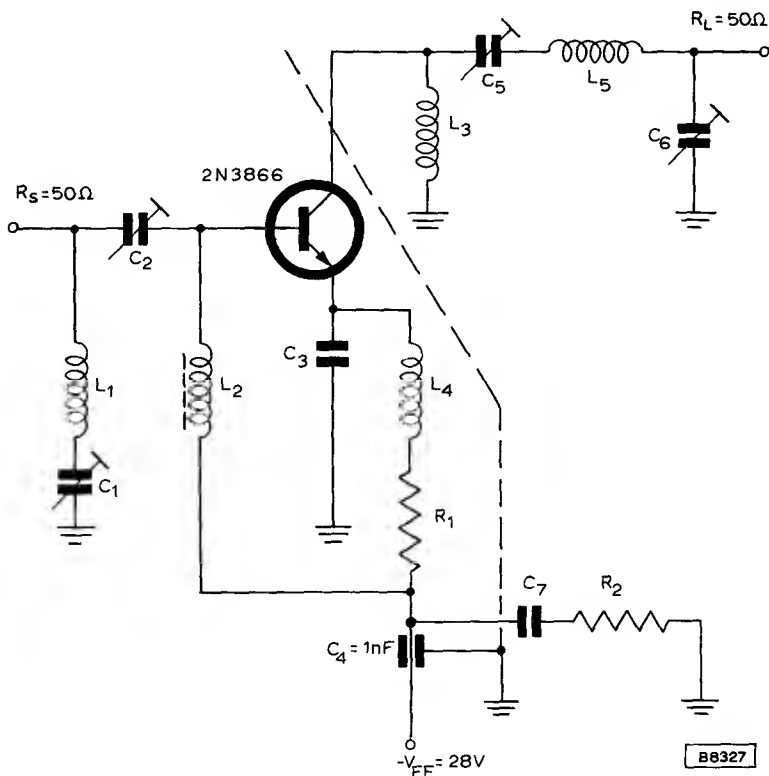
Typical r.f. performance

$$V_{CE} = 28\text{V}, T_{case} = 25^{\circ}\text{C}$$

f	Frequency	100	250	400*	MHz
P_i	Input power	50	100	<100	mW
I_C	Collector current	<107	<107	<79	mA
P_o	Output power	1.8	1.5	1.0	W
η	Efficiency	>60	>50	>45	%

*The transistor can withstand a load mismatch having a v.s.w.r. of 3, varied through all phases for conditions as given above (see also test circuit)

Common emitter test circuit ($f = 400\text{MHz}$)



Components

$C_1, C_2, C_5 = 4 \text{ to } 29\text{pF}$ air trimmers

$C_3 = 12\text{pF}$

$C_6 = 4 \text{ to } 14\text{pF}$ air trimmer

$C_7 = 12\text{nF}$

$R_1 = 5.6\Omega$

$R_2 = 10\Omega$

$L_1 = 2 \text{ turns of } 1\text{mm Cu wire, int. dia. } 6\text{mm, winding pitch } 3\text{mm}$

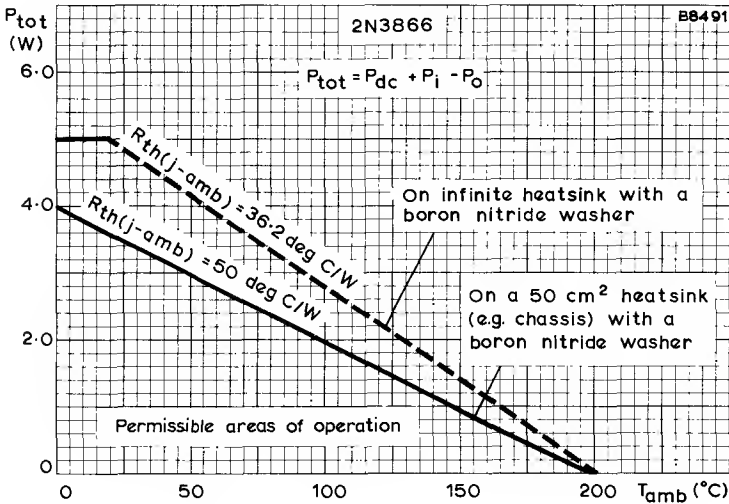
$L_2 = \text{ferroxcube choke coil (Z = } 450\Omega \text{ at } 250\text{MHz)}$

$L_3, L_4 = 6 \text{ turns of } 0.5\text{mm en. Cu wire, int. dia. } 3.5\text{mm (100nH)}$

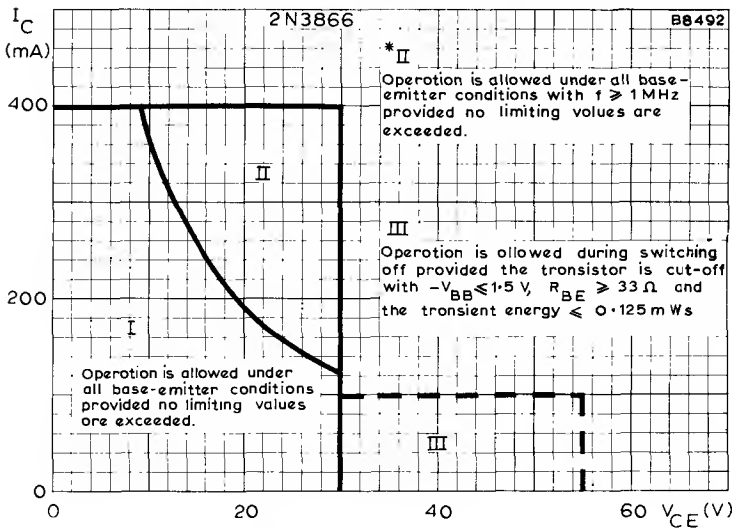
$L_5 = 2 \text{ turns of } 1\text{mm Cu wire, int. dia. } 7\text{mm, winding pitch } 2.5\text{mm, leads } 2 \times 15\text{mm}$

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

2N3866

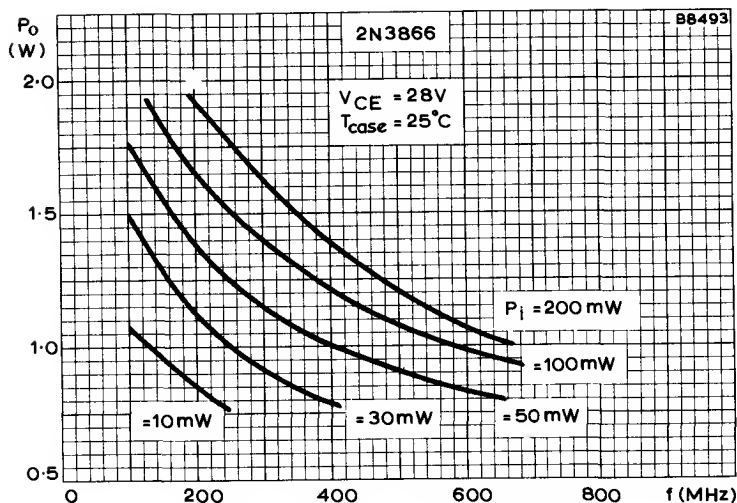


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST
AMBIENT TEMPERATURE

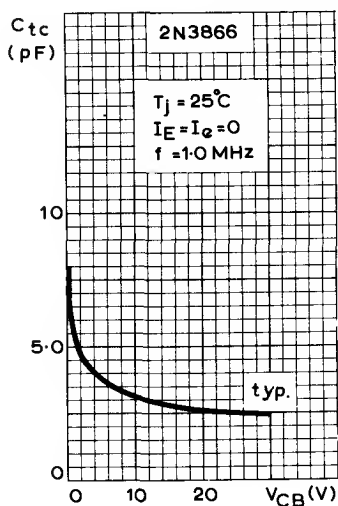


*II Care must be taken to reduce the steady state current to region I before removing the a.c. signal. This may be achieved by appropriate bias in class A, B or C.

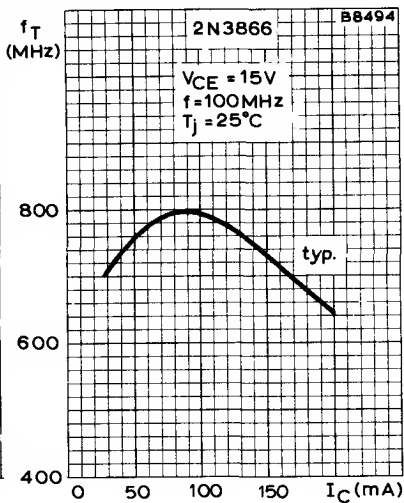
Mullard



TYPICAL VARIATION OF OUTPUT POWER WITH
FREQUENCY AND INPUT POWER



Collector capacitance versus
collector-base voltage



Transition frequency versus
collector current

N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

2N3966

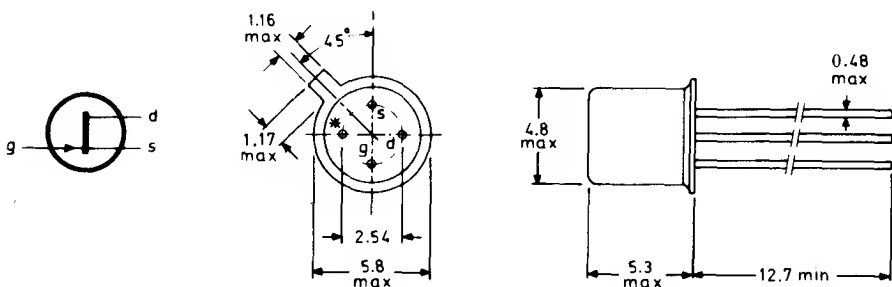
Silicon n-channel planar epitaxial junction field-effect transistor intended for low power switching applications, e.g., in multiplexing systems.

QUICK REFERENCE DATA

$\pm V_{DS}$ max.	Drain-source voltage	30	V
$-V_{GSO}$ max.	Gate-source voltage	30	V
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^{\circ}\text{C}$)	300	mW
I_{DSS} min.	Drain current ($V_{DS} = 20\text{V}$, $V_{GS} = 0$)	2.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D = 10\text{nA}$, $V_{DS} = 10\text{V}$)	4 to 6	V
$-C_{rs}$ max.	Feedback capacitance ($V_{DS} = 0$, $V_{GS} = 7\text{V}$, $f = 1\text{MHz}$)	1.5	pF
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($V_{GS} = 0$, $I_D = 0$, $f = 1\text{kHz}$)	220	Ω

OUTLINE AND DIMENSIONS

Conforms to B.S.3934 SO-12A/SB4-3 } Insulated electrodes
J.E.D.E.C. TO-72 }



All dimensions in mm

D2967

*shield lead (connected to case)

Accessories available: 56246, 56263

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	30	V
V_{DGO} max.	Drain-gate voltage (open source)	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	30	V
I_G max.	Gate current	10	mA
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^\circ\text{C}$)	300	mW

Temperature

T_{stg}	Storage temperature	-55 to +200	$^\circ\text{C}$
T_j max.	Junction temperature	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance from junction to ambient	0.59	$^\circ\text{C}/\text{mW}$
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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise stated)

		Min.	Max.	
$-I_{GSS}$	Gate cut-off current $-V_{GS} = 20\text{V}, V_{DS} = 0$	-	0.1	nA
I_{DGO}	Drain current $V_{DG} = 20\text{V}, I_S = 0$	-	0.1	nA
	$V_{DG} = 20\text{V}, I_S = 0, T_{amb} = 150^\circ\text{C}$	-	0.2	μA
I_{DSS}	Drain current $V_{DS} = 20\text{V}, V_{GS} = 0$	2.0	-	mA
$-V_{(BR)GS}$	Gate-source breakdown voltage $-I_G = 1.0\mu\text{A}, V_{DS} = 0$	30	-	V
$-V_{(P)GS}$	Gate-source voltage $I_D = 10\text{nA}, V_{DS} = 10\text{V}$	4.0	6.0	V
V_{DS}	Drain-source voltage $I_D = 1.0\text{mA}, V_{GS} = 0$	-	0.25	V

N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

2N3966

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Max.	
I_D	Drain cut-off current			
	$V_{DS} = 10V, -V_{GS} = 7V$	-	1.0	nA
	$V_{DS} = 10V, -V_{GS} = 7V, T_{amb} = 150^{\circ}C$	-	2.0	μA
$r_{DS(on)}$	Drain-source 'on' resistance			
	$V_{GS} = 0, I_D = 0, f = 1kHz$	-	220	Ω
C_{is}	Input capacitance			
	$V_{DS} = 20V, V_{GS} = 0, f = 1MHz$	-	6.0	pF
$-C_{rs}$	Feedback capacitance			
	$V_{DS} = 0, V_{GS} = 7V, f = 1MHz$	-	1.5	pF

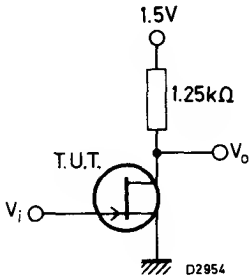
Switching times

$$V_{DD} = 1.5V, I_{D(on)} = 1.0mA$$

$$V_{GS(on)} = 0, -V_{GS(off)} = 6.0V$$

t_d	Delay time	-	20	ns
t_r	Rise time	-	100	ns
t_{off}	Turn-off time	-	100	ns

Test circuit



Pulse generator:

$$t_r < 1.0 \text{ ns}$$

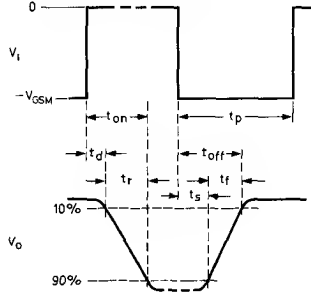
$$t_f < 1.0 \text{ ns}$$

$$t_p = 1.0 \text{ } \mu s$$

$$d < 0.5$$

$$R_S = 50 \text{ } \Omega$$

Input and output waveforms



Oscilloscope:

$$t_r < 10 \text{ ns}$$

$$R_i > 5 \text{ M}\Omega$$

$$C_i < 10 \text{ pF}$$

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4091
2N4092
2N4093

Silicon n-channel, depletion type, junction field-effect transistors intended for low power switching applications.

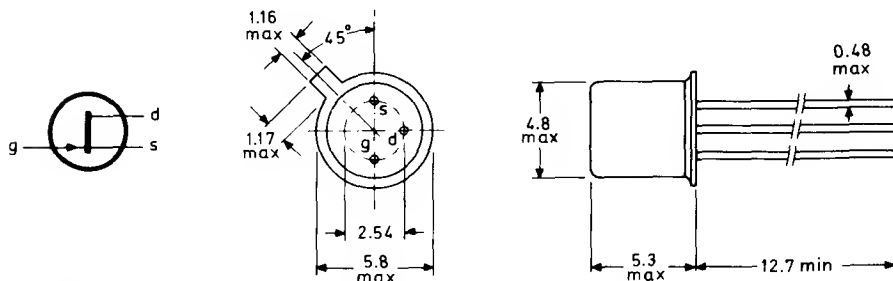
QUICK REFERENCE DATA

		2N4091	2N4092	2N4093	
V_{DS} max.	Drain-source voltage	40	40	40	V
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^{\circ}C$)	1.8	1.8	1.8	W
I_{DSS} min.	Drain current ($V_{DS} = 20V, V_{GS} = 0$)	30	15	8.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D = 1mA, V_{DS} = 20V$)	5 to 10	2 to 7	1 to 5	V
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($I_D = 0, V_{GS} = 0, f = 1kHz$)	30	50	80	Ω
$-C_{rs}$ max.	Feedback capacitance ($V_{DS} = 0, -V_{GS} = 20V, f = 1MHz$)	5.0	5.0	5.0	pF
t_{off} max.	Turn-off time ($V_{GS} = 0, V_{DD} = 3V$) ($I_D = 6.6mA, -V_{GSM} = 12V$)	40	-	-	ns
	($I_D = 4.0mA, -V_{GSM} = 8V$)	-	60	-	ns
	($I_D = 2.5mA, -V_{GSM} = 6V$)	-	-	80	ns

Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB3-6A } Gate connected to case
J. E. D. E. C. TO-18 }



All dimensions in mm

D2872

Accessories supplied on request: 56246, 56263

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{DS}$ max.	Drain-source voltage	40	V
V_{DGO} max.	Drain-gate voltage (open source)	40	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	V
I_G max.	Forward gate current (d.c.)	10	mA
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^\circ\text{C}$)	1.8	W

Temperature

T_{stg}	Storage temperature	-65 to +200	$^\circ\text{C}$
T_j max.	Junction temperature	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-c)}$	Thermal resistance from junction to case in free air	0.1	$^\circ\text{C}/\text{mW}$
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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise stated)

			Min.	Typ.	Max.
I_{DGO}	Drain current				
	$V_{DG} = 20\text{V}, I_S = 0$		-	-	0.2 nA
	$V_{DG} = 20\text{V}, I_S = 0, T_{amb} = 150^\circ\text{C}$		-	-	0.4 μA
I_{SGO}	Source current				
	$V_{SG} = 20\text{V}, I_D = 0$		-	-	0.2 nA
I_D	Drain cut-off current				
	$V_{DS} = 20\text{V}, -V_{GS} = 12\text{V}$	2N4091	-	-	0.2 nA
	$V_{DS} = 20\text{V}, -V_{GS} = 8\text{V}$	2N4092	-	-	0.2 nA
	$V_{DS} = 20\text{V}, -V_{GS} = 6\text{V}$	2N4093	-	-	0.2 nA
	$V_{DS} = 20\text{V}, -V_{GS} = 12\text{V},$ $T_{amb} = 150^\circ\text{C}$	2N4091	-	-	0.4 μA
	$V_{DS} = 20\text{V}, -V_{GS} = 8\text{V},$ $T_{amb} = 150^\circ\text{C}$	2N4092	-	-	0.4 μA
	$V_{DS} = 20\text{V}, -V_{GS} = 6\text{V},$ $T_{amb} = 150^\circ\text{C}$	2N4093	-	-	0.4 μA

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4091
2N4092
2N4093

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
$-V_{(BR)GSS}$	Gate-source breakdown voltage $-I_G = 1.0\mu A, V_{DS} = 0$	40	-	-	V
I_{DSS}	Drain current (measured under pulsed conditions, $t_p < 300\mu s$, $d < 0.03$) $V_{DS} = 20V, V_{GS} = 0$	2N4091 30 2N4092 15 2N4093 8.0	- - -	- - -	mA mA mA
$-V_{GS}$	Gate-source voltage $I_D = 1mA, V_{DS} = 20V$	2N4091 5.0 2N4092 2.0 2N4093 1.0	- - -	10 7.0 5.0	V V V
$V_{DS(on)}$	Drain-source 'on' voltage $I_D = 6.6mA, V_{GS} = 0$ $I_D = 4.0mA, V_{GS} = 0$ $I_D = 2.5mA, V_{GS} = 0$	2N4091 - 2N4092 - 2N4093 -	- - -	0.2 0.2 0.2	V V V
$r_{DS(on)}$	Drain-source 'on' resistance $I_D = 1mA, V_{GS} = 0$ $I_D = 0, V_{GS} = 0, f = 1kHz$	2N4091 - 2N4092 - 2N4093 - 2N4091 - 2N4092 - 2N4093 -	- - - - - -	30 50 80 30 50 80	Ω Ω Ω Ω Ω Ω
y-parameters (common source)					
$V_{DS} = 20V, V_{GS} = 0, f = 1MHz$					
C_{is}	Input capacitance	-	-	16	pF
$-C_{rs}$	Feedback capacitance	-	-	5.0	pF

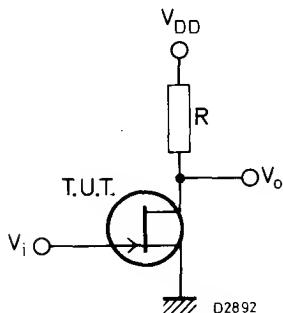
ELECTRICAL CHARACTERISTICS (contd.)

Switching times

$$V_{DD} = 3.0V, V_{GS} = 0$$

t_d Delay time
 t_r Rise time
 t_{off} Turn-off time

Test circuit



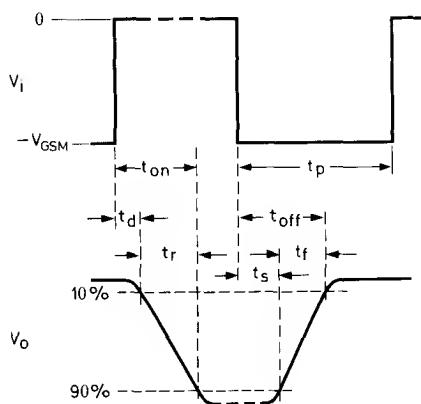
$$R = \frac{2.8}{I_D} \Omega$$

Pulse generator:

$$\begin{aligned} t_r &< 1ns \\ t_f &< 1ns \\ t_p &= 1\mu s \\ d &= 0.1 \\ R_S &= 50\Omega \end{aligned}$$

	2N4091	2N4092	2N4093	
$I_D =$	6.6	4.0	2.5	mA
$-V_{GSM} =$	12	8.0	6.0	V
max.	15	15	20	ns
max.	10	20	40	ns
max.	40	60	80	ns

Input and output waveforms



D2874

Oscilloscope:

$$\begin{aligned} t_r &< 0.4ns \\ R_i &> 9.8M\Omega \\ Z_i &< 1.7pF \end{aligned}$$

**N-P-N SILICON DIFFUSED
POWER TRANSISTOR**

2N4347

For details see data sheet for type 2N3442

Mullard

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4391
2N4392
2N4393

Silicon n-channel, depletion type, junction field-effect transistors intended for low power chopper or switching applications.

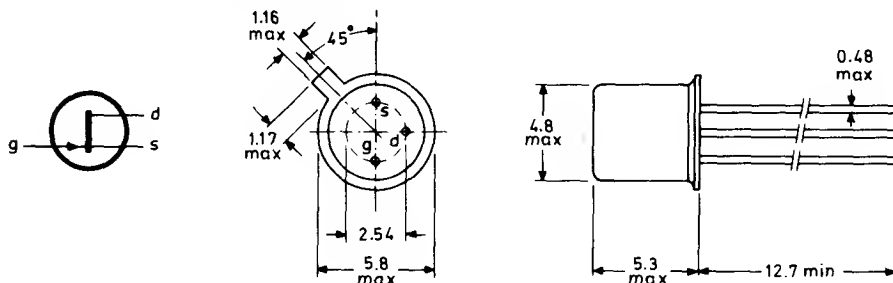
QUICK REFERENCE DATA

		2N4391	2N4392	2N4393	
$+V_{DS}$ max.	Drain-source voltage	40	40	40	V
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^\circ\text{C}$)	1.8	1.8	1.8	W
I_{DSS} min.	Drain current ($V_{DS} = 20\text{V}$, $V_{GS} = 0$)	50	25	5.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D = 1\text{nA}$, $V_{DS} = 20\text{V}$)	4 to 10	2 to 5	0.5 to 3	V
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($I_D = 0$, $V_{GS} = 0$, $f = 1\text{kHz}$)	30	60	100	Ω
$-C_{rs}$ max.	Feedback capacitance ($V_{DS} = 0$, $-V_{GS} = 12\text{V}$, $f = 1\text{MHz}$)	3.5	-	-	pF
	($V_{DS} = 0$, $-V_{GS} = 7\text{V}$, $f = 1\text{MHz}$)	-	3.5	-	pF
	($V_{DS} = 0$, $-V_{GS} = 5\text{V}$, $f = 1\text{MHz}$)	-	-	3.5	pF
t_{off} max.	Turn-off time ($V_{GS} = 0$, $V_{DD} = 10\text{V}$)				
	($I_D = 12\text{mA}$, $-V_{GSM} = 12\text{V}$)	20	-	-	ns
	($I_D = 6\text{mA}$, $-V_{GSM} = 7\text{V}$)	-	35	-	ns
	($I_D = 3\text{mA}$, $-V_{GSM} = 5\text{V}$)	-	-	50	ns

Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB3-6A } Gate connected to case
J.E.D.E.C. TO-18



All dimensions in mm

02872

Accessories supplied on request: 56246, 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	40	V
V_{DGO} max.	Drain-gate voltage (open source)	40	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	V
I_G max.	Gate current	50	mA
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^\circ\text{C}$)	1.8	W

Temperature

T_{stg}	Storage temperature	-65 to +200	$^\circ\text{C}$
T_j max.	Junction temperature	200	$^\circ\text{C}$

THERMAL CHARACTERISTIC

$R_{th(j-c)}$	Thermal resistance from junction to case in free air	0.1	$^\circ\text{C/mW}$
---------------	---	-----	---------------------

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise stated)

			Min.	Typ.	Max.
$-I_{GSS}$	Gate cut-off current				
	$-V_{GS} = 20\text{V}, V_{DS} = 0$		-	-	0.1 nA
	$-V_{GS} = 20\text{V}, V_{DS} = 0, T_{amb} = 150^\circ\text{C}$		-	-	0.2 μA
I_{DSX}	Drain cut-off current				
	$V_{DS} = 20\text{V}, -V_{GS} = 12\text{V}$	2N4391	-	-	0.1 nA
	$V_{DS} = 20\text{V}, -V_{GS} = 7\text{V}$	2N4392	-	-	0.1 nA
	$V_{DS} = 20\text{V}, -V_{GS} = 5\text{V}$	2N4393	-	-	0.1 nA
	$V_{DS} = 20\text{V}, -V_{GS} = 12\text{V},$ $T_{amb} = 150^\circ\text{C}$	2N4391	-	-	0.2 μA
	$V_{DS} = 20\text{V}, -V_{GS} = 7\text{V},$ $T_{amb} = 150^\circ\text{C}$	2N4392	-	-	0.2 μA
	$V_{DS} = 20\text{V}, -V_{GS} = 5\text{V},$ $T_{amb} = 150^\circ\text{C}$	2N4393	-	-	0.2 μA
	Drain current (pulse measurement, $t_p = 100\mu\text{s}, d = 0.01$)				
	$V_{DS} = 20\text{V}, V_{GS} = 0$	2N4391	50	-	150 mA
I_{DSS}	$V_{DS} = 20\text{V}, V_{GS} = 0$	2N4392	25	-	75 mA
	$V_{DS} = 20\text{V}, V_{GS} = 0$	2N4393	5.0	-	30 mA

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4391
2N4392
2N4393

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
$-V_{(BR)GSS}$	Gate-source breakdown voltage $-I_G = 1\mu A, V_{DS} = 0$		40	-	-	V
$V_{GS(on)}$	Gate-source 'on' voltage $I_G = 1mA, V_{DS} = 0$		-	-	1.0	V
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 1nA, V_{DS} = 0$	2N4391	4.0	-	10	V
		2N4392	2.0	-	5.0	V
		2N4393	0.5	-	3.0	V
$V_{DS(on)}$	Drain-source 'on' voltage $I_D = 12mA, V_{GS} = 0$	2N4391	-	-	0.4	V
	$I_D = 6mA, V_{GS} = 0$	2N4392	-	-	0.4	V
	$I_D = 3mA, V_{GS} = 0$	2N4393	-	-	0.4	V
$r_{DS(on)}$	Drain-source 'on' resistance $I_D = 1mA, V_{GS} = 0$	2N4391	-	-	30	Ω
		2N4392	-	-	60	Ω
		2N4393	-	-	100	Ω
	$I_D = 0, V_{GS} = 0, f = 1kHz$	2N4391	-	-	30	Ω
		2N4392	-	-	60	Ω
		2N4393	-	-	100	Ω
y-parameters (common source)						
C_{is}	Input capacitance $V_{DS} = 20V, V_{GS} = 0, f = 1MHz$		-	-	14	pF
$-C_{rs}$	Feedback capacitance $-V_{GS} = 12V, V_{DS} = 0, f = 1MHz$	2N4391	-	-	3.5	pF
	$-V_{GS} = 7V, V_{DS} = 0, f = 1MHz$	2N4392	-	-	3.5	pF
	$-V_{GS} = 5V, V_{DS} = 0, f = 1MHz$	2N4393	-	-	3.5	pF

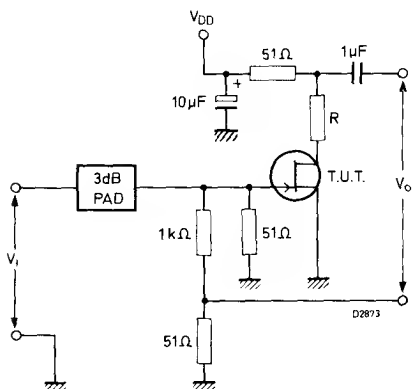
ELECTRICAL CHARACTERISTICS (contd.)

Switching times

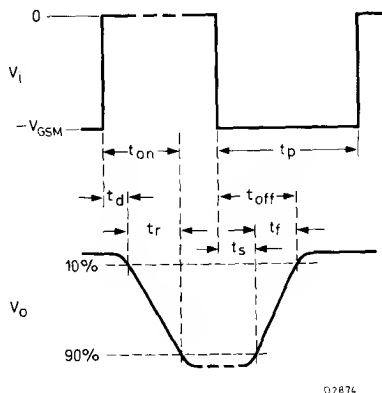
$$V_{DD} = 10V, V_{GS} = 0$$

		2N4391	2N4392	2N4393	
I_D		12	6.0	3.0	mA
$-V_{GSM}$		12	7.0	5.0	V
t_r	Rise time	max. 5.0	5.0	5.0	ns
t_{on}	Turn-on time	max. 15	15	15	ns
t_f	Fall time	max. 15	20	30	ns
t_{off}	Turn-off time	max. 20	35	50	ns

Test circuit



Input and output waveforms



$$R = \frac{9.6}{I_D} - 51\Omega$$

Pulse generator :

$$t_r < 0.5ns$$

$$t_f < 0.5ns$$

$$t_p = 100\mu s$$

$$d = 0.01$$

Oscilloscope:

$$R_i = 50\Omega$$

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

2N4427

N-P-N silicon planar epitaxial transistor primarily intended for use in the output, driver and pre-driver stages of class A, B or C amplifiers, frequency multipliers and oscillators of v.h.f. and u.h.f. equipment.

Encapsulated in a metal TO-39 envelope with the collector connected to the case.

QUICK REFERENCE DATA

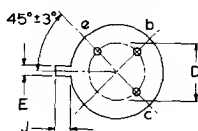
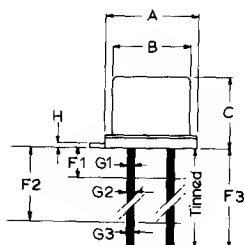
V_{CER} max.	40	V
V_{CEO} max.	20	V
I_C max.	400	mA
P_{tot} max. ($T_{case} \leq 25^\circ\text{C}$)	3.5	W
T_j max.	200	$^\circ\text{C}$
f_T typ. ($I_C = 25\text{mA}$, $V_{CE} = 10\text{V}$, $f = 100\text{MHz}$)	700	MHz
P_o typ. ($P_i < 100\text{mW}$, $V_{CE} = 12\text{V}$, $f = 175\text{MHz}$)	1.0	W
η min. ($P_o = 1.0\text{W}$, $V_{CE} = 12\text{V}$, $f = 175\text{MHz}$)	50	%

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B

J.E.D.E.C. TO-39

Millimetres



	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	40	V
V_{CER} max. ($R_{BE} = 10\Omega$)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	2.0	V
I_C max.	400	mA
I_{CM} max.	400	mA
P_{tot} max. ($T_{case} \leq 25^\circ C$)	3.5	W

Temperature

T_{stg} min.	-65	$^\circ C$
T_{stg} max.	200	$^\circ C$
T_j max.	200	$^\circ C$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	In free air	200	degC/W
$R_{th(j-case)}$		35	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218	1.0	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CEO}	Collector cut-off current $V_{CE} = 12V, I_B = 0$	-	-	20	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 100\mu A, I_E = 0$	40	-	-	V
	Collector-emitter breakdown voltages				
$V_{(BR)CER}$	$I_C = 5.0mA, R_{BE} = 10\Omega$	40	-	-	V
$V_{(BR)CEO}$	$I_C = 5.0mA, I_B = 0$	20	-	-	V
$V_{(BR)EBO}$	Collector-base breakdown voltage $I_E = 100\mu A, I_C = 0$	2.0	-	-	V

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

2N4427

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100\text{mA}$, $I_B = 20\text{mA}$	-	-	0.5	V
h_{FE}	Static forward current transfer ratio $I_C = 100\text{mA}$, $V_{CE} = 5.0\text{V}$ $I_C = 360\text{mA}$, $V_{CE} = 5.0\text{V}$	10 5	- -	200 -	
f_T	Transition frequency $I_C = 25\text{mA}$, $V_{CE} = 10\text{V}$, $f = 100\text{MHz}$	-	700	-	MHz
C_{tc}	Collector capacitance $V_{CB} = 12\text{V}$, $I_E = I_e = 0$, $f = 1.0\text{MHz}$	-	-	4.0	pF

Typical r.f. performance

$$V_{CE} = 12\text{V}, T_{case} = 25^{\circ}\text{C}$$

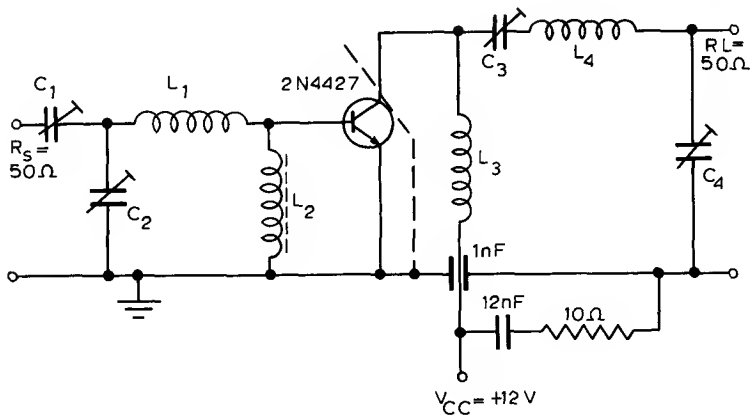
f	Frequency	175*	470	MHz
P_i	Input power	< 100	100	mW
I_C	Collector current	< 167	67	mA
P_o	Output power	1.0	0.4	W
η	Efficiency	> 50	50	%

*The transistor can withstand a load mismatch having a v.s.w.r. of 3, varied through all phases for conditions as given above (see also test circuit)

Mullard

Common emitter test circuit ($f = 175\text{MHz}$)

B8403



Components

$C_1, C_2, C_3, C_4 = 4$ to 29pF air trimmers

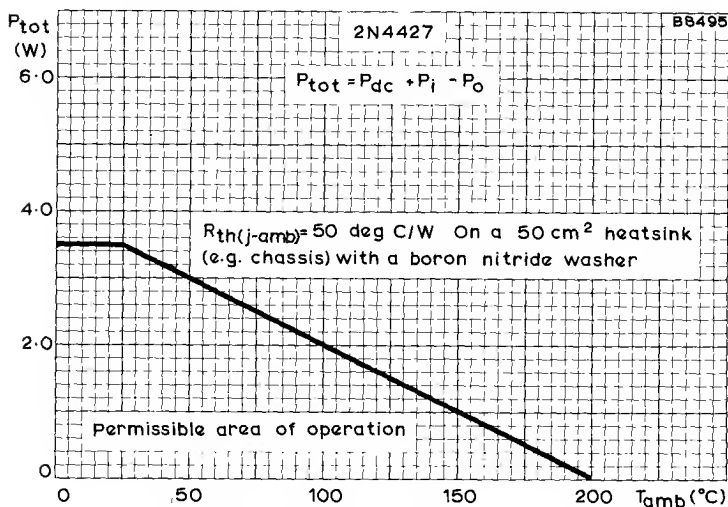
$L_1 = 2$ turns of 1mm Cu wire, int. dia. 6mm , winding pitch 2mm , leads $2 \times 10\text{mm}$

$L_2 =$ ferroxcube choke coil ($Z = 550\Omega$ at 175MHz)

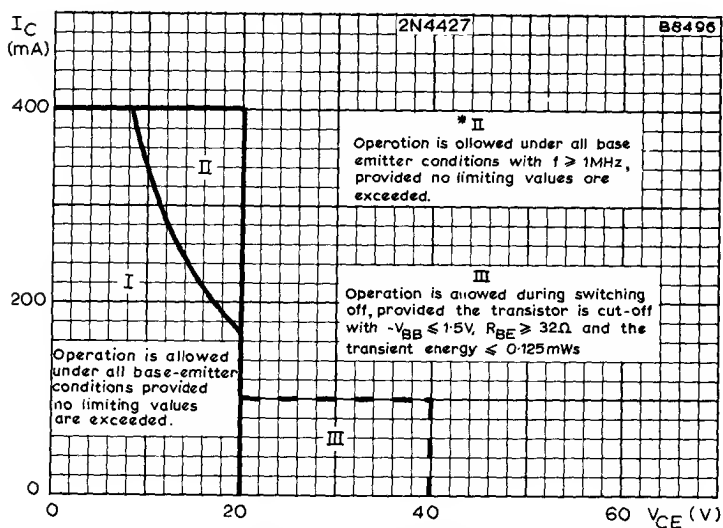
$L_3 = 2$ turns of 1mm Cu wire, int. dia. 5mm , winding pitch 2mm , leads $2 \times 10\text{mm}$

$L_4 = 3$ turns of 1.5mm Cu wire, int. dia. 10mm , winding pitch 2mm , leads $2 \times 15\text{mm}$

The length of the external emitter wire of the 2N4427 is 1.6mm

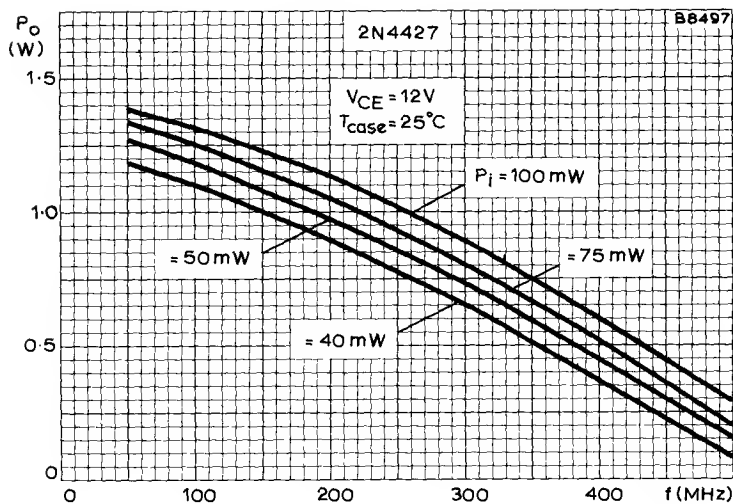


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST
AMBIENT TEMPERATURE

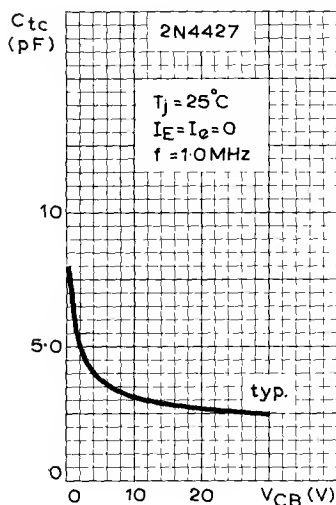


AREAS OF SAFE OPERATION

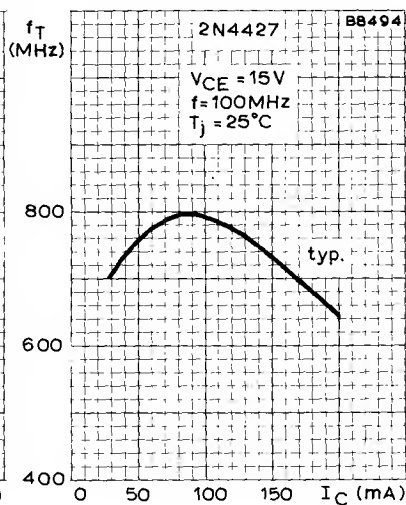
*II Care must be taken to reduce the steady state current to region I before removing the a.c. signal. This may be achieved by appropriate bias in class A, B or C.



TYPICAL VARIATION OF OUTPUT POWER WITH
FREQUENCY AND INPUT POWER



Collector capacitance versus
collector-base voltage



Transition frequency versus
collector current

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4856 to 2N4861

Silicon n-channel, depletion type, junction field-effect transistors intended for low power chopper or switching applications.

QUICK REFERENCE DATA

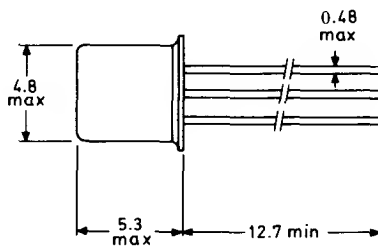
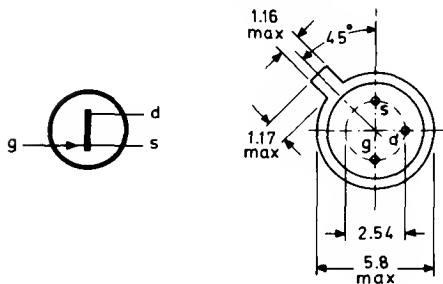
$\pm V_{DS}$ max.	Drain-source voltage	2N4856 to 2N4858		40	V
		2N4859 to 2N4861		30	V
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^{\circ}\text{C}$)	360			mW
		2N4856	2N4857	2N4858	
		2N4859	2N4860	2N4861	
I_{DSS} min.	Drain current ($V_{DS} = 15\text{V}$, $V_{GS} = 0$)	50	20	8	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D = 0.5\text{nA}$, $V_{DS} = 15\text{V}$)	4-10	2-6	0.8-4	V
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($I_D = 0$, $V_{GS} = 0$, $f = 1\text{kHz}$)	25	40	60	Ω
$-C_{rs}$ max.	Feedback capacitance ($V_{DS} = 0$, $-V_{GS} = 10\text{V}$, $f = 1\text{MHz}$)	8	8	8	pF
t_{off} max.	Turn-off time ($V_{DD} = 10\text{V}$, $V_{GS} = 0$)				
	$I_D = 20\text{mA}$, $-V_{GSM} = 10\text{V}$	25	-	-	ns
	$I_D = 10\text{mA}$, $-V_{GSM} = 6\text{V}$	-	50	-	ns
	$I_D = 5\text{mA}$, $-V_{GSM} = 4\text{V}$	-	-	100	ns

Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB3-6A
J. E. D. E. C. TO-18

Gate connected to the case



All dimensions in mm

D2872

Accessories supplied on request: 56246; 56263

Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

		2N4856	2N4859	
		2N4857	2N4860	
		2N4858	2N4861	
$\pm V_{DS}$ max.	Drain-source voltage	40	30	V
V_{DGO} max.	Drain-gate voltage (open source)	40	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	30	V
I_G max.	Gate current (d.c.)		50	mA
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^\circ\text{C}$)		360	mW
Temperature				
T_{stg}	Storage temperature	-65 to +200		$^\circ\text{C}$
T_j	Junction temperature	200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance from junction to ambient in free air	0.49	$^\circ\text{C}/\text{mW}$
-----------------	--	------	----------------------------

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise stated)

			Min.	Max.	
$-I_{GSS}$	Gate cut-off current				
	$-V_{GS} = 20\text{V}, V_{DS} = 0$	2N4856 to 2N4858	-	0.25	nA
	$-V_{GS} = 15\text{V}, V_{DS} = 0$	2N4859 to 2N4861	-	0.25	nA
	$-V_{GS} = 20\text{V}, V_{DS} = 0, T_{amb} = 150^\circ\text{C}$	2N4856 to 2N4858	-	0.5	μA
	$-V_{GS} = 15\text{V}, V_{DS} = 0, T_{amb} = 150^\circ\text{C}$	2N4859 to 2N4861	-	0.5	μA
I_{DSX}	Drain cut-off current				
	$V_{DS} = 15\text{V}, -V_{GS} = 10\text{V}$		-	0.25	nA
	$V_{DS} = 15\text{V}, -V_{GS} = 10\text{V}, T_{amb} = 150^\circ\text{C}$		-	0.5	μA
I_{DSS}	Drain current (pulse measurement, $t_p = 100\text{ms}, d \leq 0.1$)				
	$V_{DS} = 15\text{V}, V_{GS} = 0$	2N4856, 2N4859	50	-	mA
		2N4857, 2N4860	20	100	mA
		2N4858, 2N4861	8.0	80	mA

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4856
to
2N4861

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Max.	
-V _{(BR)GSS}	Gate-source breakdown voltage				
	-I _G = 1μA, V _{DS} = 0	2N4856 to 2N4858	40	-	V
		2N4859 to 2N4861	30	-	V
-V _{(P)GS}	Gate-source cut-off voltage				
	I _D = 0.5mA, V _{DS} = 15V	2N4856, 2N4859	4.0	10	V
		2N4857, 2N4860	2.0	6.0	V
		2N4858, 2N4861	0.8	4.0	V
V _{DS(on)}	Drain-source 'on' voltage				
	I _D = 20mA, V _{GS} = 0	2N4856, 2N4859	-	0.75	V
	I _D = 10mA, V _{GS} = 0	2N4857, 2N4860	-	0.50	V
	I _D = 5mA, V _{GS} = 0	2N4858, 2N4861	-	0.50	V
r _{DS(on)}	Drain-source 'on' resistance				
	I _D = 0, V _{GS} = 0, f = 1kHz	2N4856, 2N4859	-	25	Ω
		2N4857, 2N4860	-	40	Ω
		2N4858, 2N4861	-	60	Ω
y-parameters (common source)					
-V _{GS} = 10V, V _{DS} = 0, f = 1MHz					
C _{is}	Input capacitance		-	18	pF
-C _{rs}	Feedback capacitance		-	8.0	pF

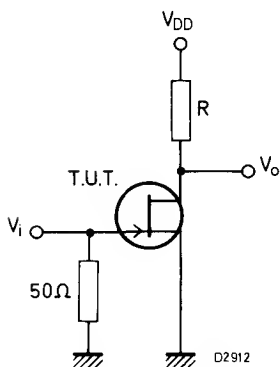
ELECTRICAL CHARACTERISTICS (contd.)

Switching times

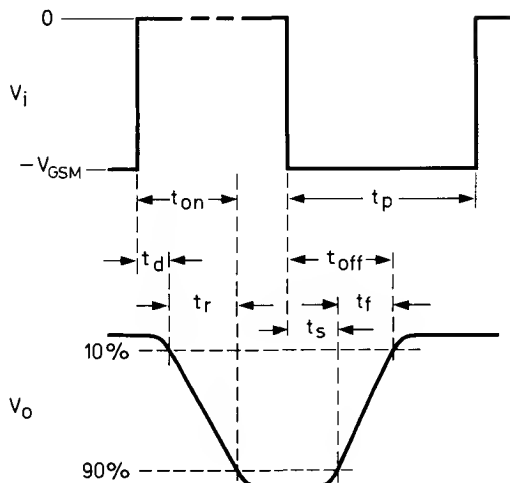
$$V_{DD} = 10V, V_{GS} = 0$$

		2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
	I_D	= 20	10	5.0	mA
	$-V_{GSM}$	= 10	6.0	4.0	V
t_d	Delay time	max. 6.0	6.0	10	ns
t_r	Rise time	max. 3.0	4.0	10	ns
t_{off}	Turn-off time	max. 25	50	100	ns

Test circuit:



Input and output waveforms



D2874

	2N4856	2N4857	2N4859
	2N4859	2N4860	2N4861
R =	464	953	1910 Ω

Pulse generator:

$$\begin{aligned} t_p &= 200 \text{ ns} \\ t_r &\leq 1 \text{ ns} \\ t_f &\leq 1 \text{ ns} \\ d &= 0.02 \\ Z_o &= 50 \Omega \end{aligned}$$

Oscilloscope:

$$\begin{aligned} t_r &\leq 0.75 \text{ ns} \\ R_i &\geq 1 \text{ M}\Omega \\ C_i &\leq 2.5 \text{ pF} \end{aligned}$$

ACCESSORIES

C





ACCESSORIES FOR TRANSISTORS

Section 1 Cooling Clips

PART NUMBER	FOR USE ON OUTLINES		PAGE
	J.E.D.E.C.	BS 3934	
56200*	TO-1	SO-21/SB3-10	3
56207*	TO-7	SO-23/SB4-4	4
56209*	TO-1	SO-21/SB3-10	5
56226	TO-1	SO-21/SB3-10	6
56227	TO-1	SO-21/SB3-10	7
56263	TO-18	SO-12A/SB3-6A	8
	TO-71	SO-12A/SB8-1B	
	TO-72	SO-12A/SB4-3	
56265	TO-5	SO-3/SB3-3A	9
	TO-12	SO-3/SB4-1	
	TO-33	SO-3/SB4-1	
	TO-39	SO-3/SB3-3B	

*These devices are supplied on a maintenance basis only, they are not recommended for current design

Section 2 Mounting Accessories

PART NUMBER	DESCRIPTION	FOR USE ON OUTLINES	PAGE
56201A	Insulating bush	TO-3 3.15mm (thick or medium with 56300)	10
56201B	Mica washer	TO-3 all	10
56239A	Insulating bush	TO-3 1.6mm (medium)	16
56336A	Insulating bush (2kV)	TO-3 3.15mm (thick)	17
56336B	Mica washer (2kV)	TO-3 all	17
56214	Lead washer	TO-3 all	10
56300	Steel spacer	TO-3 0.9 or 1.6mm (thin or medium)	11
56218	Top and bottom clamping washer and Mylar washer	TO-5, TO-39 (and TO-12, TO-33 for non-insulated mounting)	12
56245	Insulated distance disc	TO-5, TO-12, TO-33, TO-39	13
56246	Insulated distance disc	TO-18, TO-72	13
56301B	Mica washer	TO-126	14-15
56326	Flat metal washer	TO-126	14-15
56325	Mica washer	TO-220	18
56338	Insulating bush	TO-220	18
56239A	Insulating bush	— SO-55 (BS 3934)	16
56239B	Mica washer	— SO-55 (BS 3934)	16

All information on thermal resistance of the accessories combined with flat heatsinks is valid for **square** heatsinks of **blackened aluminium**.

For a few variations the thermal resistance may be derived as follows:

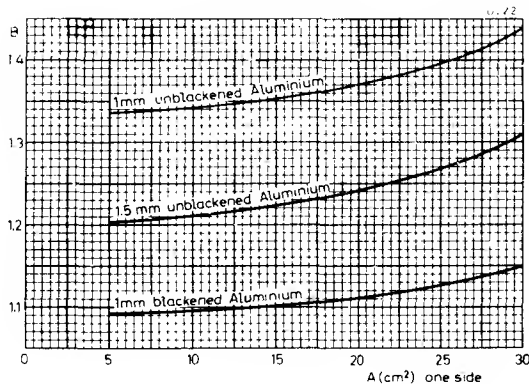
a. **Rectangular heatsinks** (sides a and $2a$)

When mounted with long side horizontal, multiply by 0.95.

When mounted with short side horizontal, multiply by 1.10.

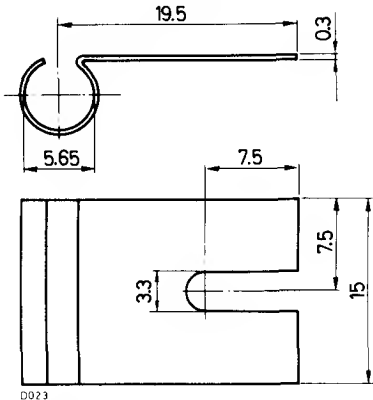
b. **Unblackened or thicker heatsinks**

Multiply by the factor B given below as a function of the heatsink size A .



COOLING CLIP

MECHANICAL DATA (Dimensions in mm)

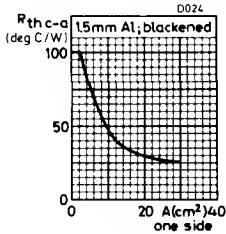


Clip material: brass, nickel plated

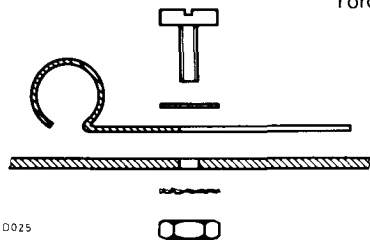
THERMAL CHARACTERISTICS

$R_{th(case-amb)}$ Thermal resistance case to ambient,
cooling clip only
with heatsink

100 degC/W
see graph



MOUNTING INSTRUCTIONS

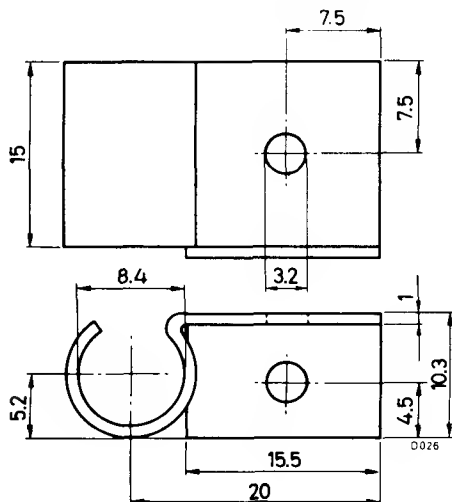


Torque on nut for good heat transfer: 5kg cm

- M3 bolt
- washer
- cooling fin
- heatsink
- lock washer
- nut

COOLING CLIP

MECHANICAL DATA (Dimensions in mm)

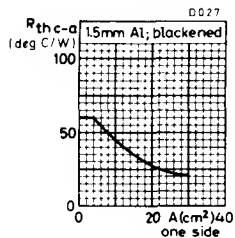


Clip material: aluminium, blackened

THERMAL CHARACTERISTICS

$R_{th}(case-amb)$ Thermal resistance case to ambient,
cooling clip only
with heatsink

60 degC/W
see graph

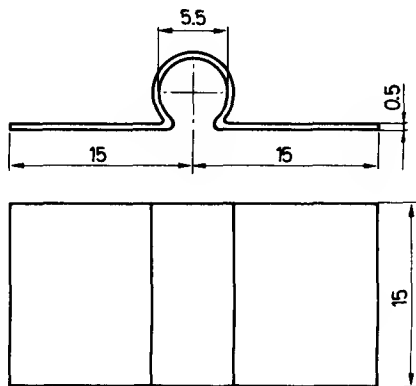


MOUNTING INSTRUCTIONS

Torque on M3 bolts for good heat transfer: 5kg cm

COOLING CLIP

MECHANICAL DATA (Dimensions in mm)



0028

Clip material: brass, nickel plated

THERMAL CHARACTERISTIC

$R_{th(case-amb)}$

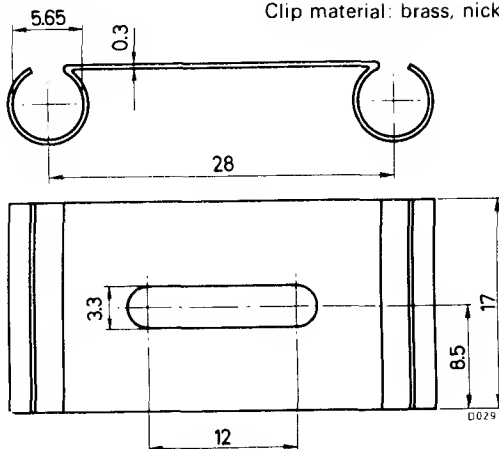
Thermal resistance case to ambient,
cooling clip only

75 degC/W

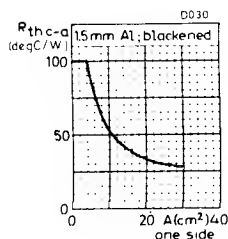
COOLING CLIP

MECHANICAL DATA (Dimensions in mm)

Clip material: brass, nickel plated



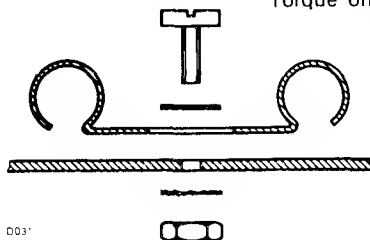
THERMAL CHARACTERISTICS

 $R_{th(case-amb)}$ Thermal resistance case to ambient,
cooling clip only
with heatsink100 degC/W
see graph

The thermal resistance values apply to each transistor, provided the two transistors have been mounted so that the heat flow from each one is equal.

MOUNTING INSTRUCTIONS

Torque on nut for good heat transfer: 5kg cm.



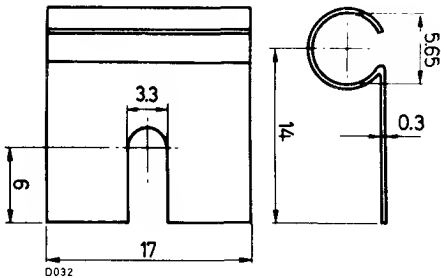
M3 bolt

washer
cooling finheatsink
lock washer

nut

COOLING CLIP

MECHANICAL DATA (Dimensions in mm)

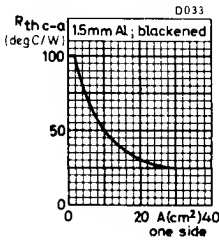


Clip material: brass, nickel plated

THERMAL CHARACTERISTICS

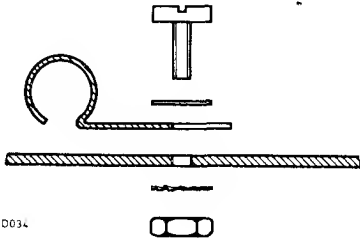
$R_{th(case-amb)}$ Thermal resistance case to ambient,
cooling clip only
with heatsink

100 degC/W
see graph



MOUNTING INSTRUCTIONS

Torque on nut for good heat transfer: 5kg cm



M3 bolt

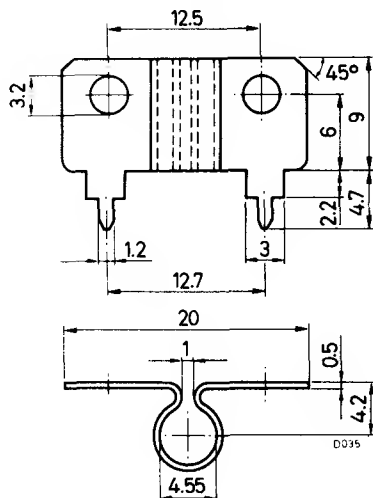
washer
cooling fin

heatsink
lock washer

nut

COOLING CLIP

MECHANICAL DATA (Dimensions in mm)



Clip material: copper, tin plated

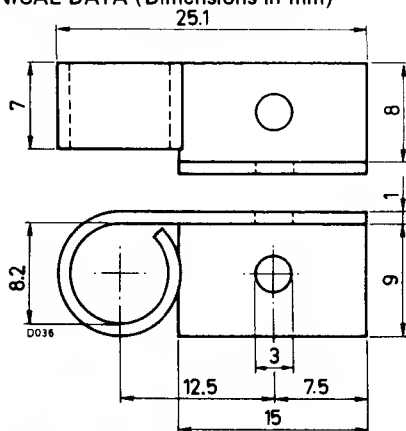
THERMAL CHARACTERISTIC

 $R_{th(case-amb)}$ Thermal resistance case to ambient

100 degC/W

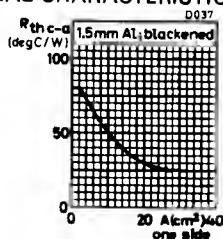
COOLING CLIP

MECHANICAL DATA (Dimensions in mm)



Clip material: aluminium, blackened

THERMAL CHARACTERISTICS

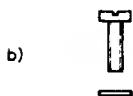
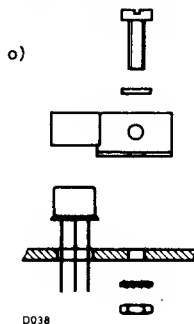


$R_{th(case-a+mb)}$

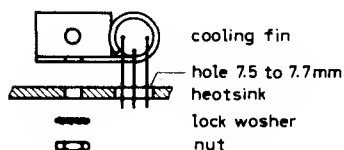
Thermal resistance case to ambient,
cooling clip only
with heatsink

80 degC/W
see graph

MOUNTING INSTRUCTIONS



M3 bolt
washer



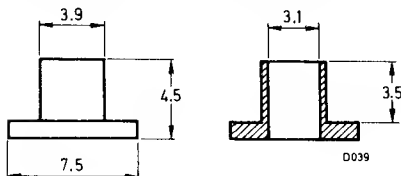
Torque on nut for good heat transfer: 5kg cm.

56201A
56201B
56214

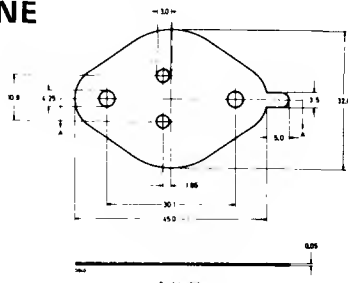
**ACCESSORIES FOR
TRANSISTORS**

MOUNTING ACCESSORIES FOR TO-3 OUTLINE

MECHANICAL DATA (Dimensions in mm)



Insulating bush
56201A



Mica washer
56201B

THERMAL CHARACTERISTIC

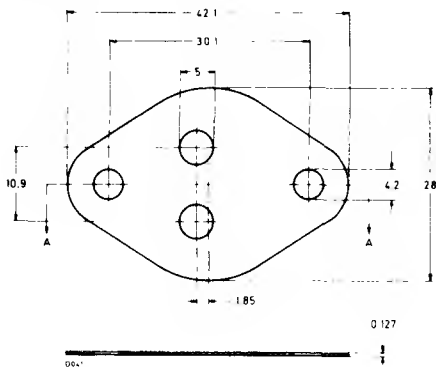
$R_{th(m-b-h)}$

Thermal resistance
mounting-base to heatsink

1 degC/W

56214 Lead washer

MECHANICAL DATA (Dimensions in mm)



Section A-A

THERMAL CHARACTERISTIC

$R_{th(m-b-h)}$

Thermal resistance mounting-base to
heatsink, with mica washer and lead
washer

0.75 degC/W

TEMPERATURE

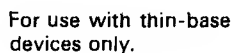
T_{max}

Max. allowable temperature

150 °C

Mullard

56300 Steel spacer



nut

lock washer

soldering tag

lead washer

micro washer

heatsink

insulating bush

M3 bolt

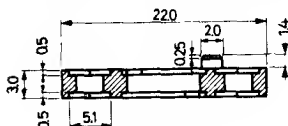
D943

Torque on nut for good heat transfer: 5kg cm

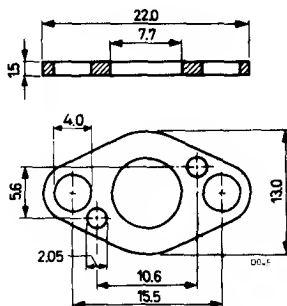
MOUNTING ACCESSORIES FOR TO-5, TO-12, TO-33, TO-39 OUTLINES

56218 Top and bottom clamping washers and Mylar washer

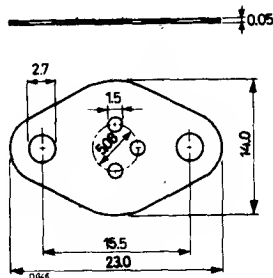
MECHANICAL DATA (Dimensions in mm)



Top clamping washer
of insulating material



Bottom clamping washer
material: brass, tin plated



Mylar washer

THERMAL CHARACTERISTICS

$R_{th}(m b-h)$

Thermal resistance mounting-base to heatsink,
non-insulated mounting
insulated mounting

1 degC/W
6 degC/W

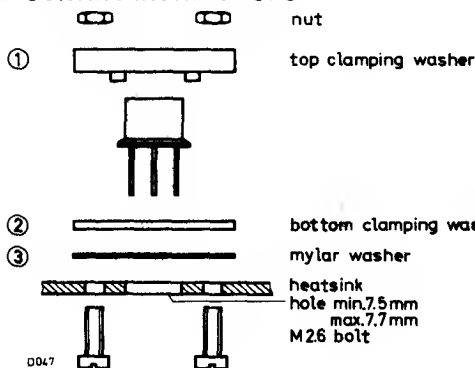
TEMPERATURE

T_{max}

Max. allowable temperature

100 °C

MOUNTING INSTRUCTIONS

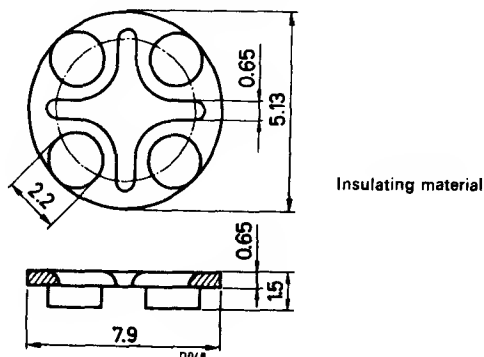


Non-insulated: without items 2 and 3
Note: Item 1 must then be mounted
upside down.

**MOUNTING ACCESSORIES FOR
TO-5, TO-12, TO-33, TO-39 OUTLINES (cont'd)**

56245 Distance disc

MECHANICAL DATA (Dimensions in mm)



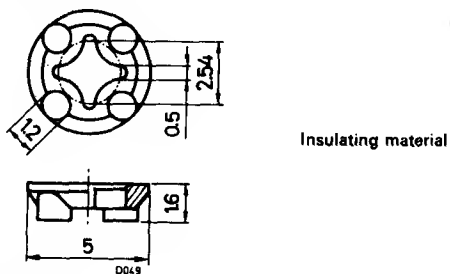
TEMPERATURE

T_{max}

Max. allowable temperature

100 °C

56246 Distance disc



TEMPERATURE

T_{max}

Max. allowable temperature

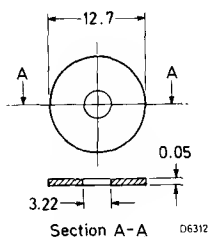
100 °C

MOUNTING ACCESSORIES FOR TO-126 OUTLINE

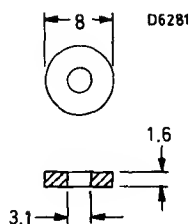
56301B Mica washer

56326 Steel washer

MECHANICAL DATA (Dimensions in mm)



Mica washer



Steel washer

Thermal CHARACTERISTICS

$R_{th(m b-h)}$

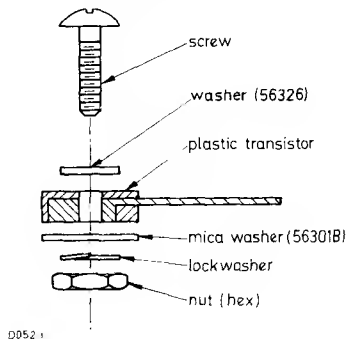
Thermal resistance
mounting-base to heatsink,

without insulating material
with mica washer (56301B)

1 degC/W

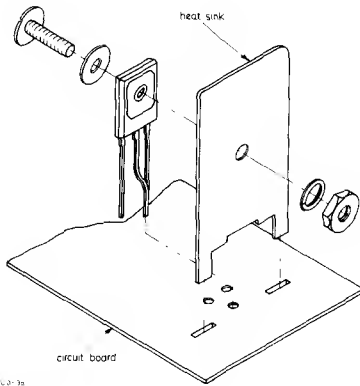
4 degC/W

MOUNTING INSTRUCTIONS

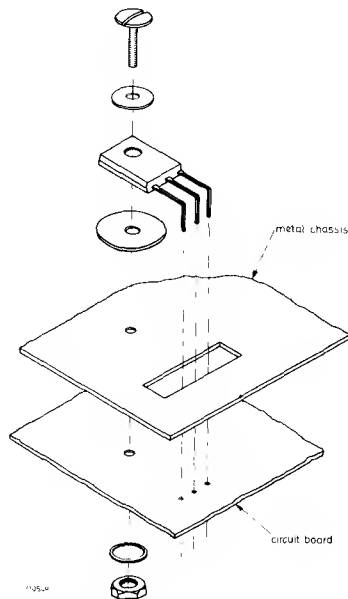


**MOUNTING DETAILS
TO-126 OUTLINE**

METHOD 1

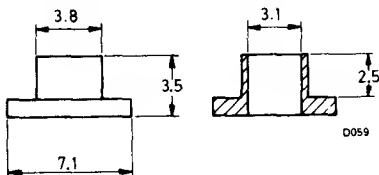


METHOD 2

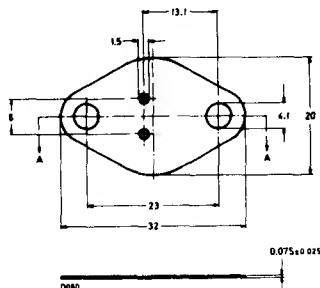


**MOUNTING ACCESSORIES FOR
BS 3934 SO-55B OUTLINE**

MECHANICAL DATA (Dimensions in mm)



**Insulating bush
56239A**



**Mica washer
56239B**

THERMAL CHARACTERISTIC

$R_{th(m b-h)}$

Thermal resistance mounting-base
to heatsink

1.5 degC/W

TEMPERATURE

T_{max}

Max. allowable temperature

150 °C

MOUNTING INSTRUCTIONS

nut

lock washer

soldering tag



nut

lock washer



holes max 4mm



mica washer

heatsink

insulating bush



M3 bolt

D051

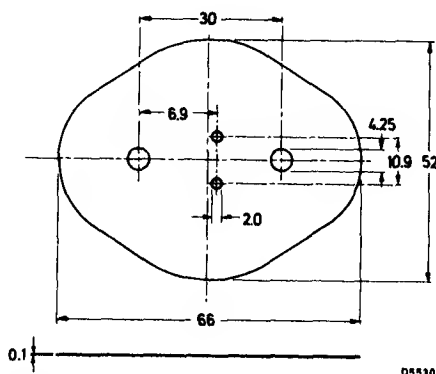
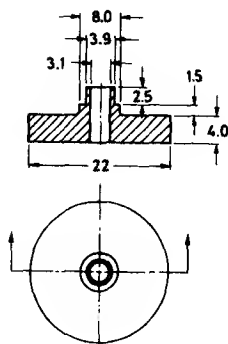


Torque on nut for good heat transfer: 5kg cm.

MOUNTING ACCESSORIES FOR TO-3 OUTLINE

(High Voltage Application, up to 2kV)

56336A Insulating bush
56336B Mica washer



Dimensions in mm

THERMAL CHARACTERISTICS

$R_{th(mb-h)}$

Thermal resistance, mounting-base to
heatsink 1°C/W

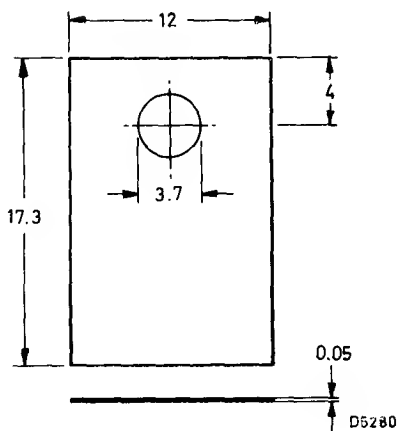
The use of a heatsink compound is essential.
When the mica washer is used, the compound must be applied
to both sides of the washer.

MOUNTING ACCESSORIES FOR TO-220

→ 56325 Mica washer

MECHANICAL DATA

Dimensions in mm



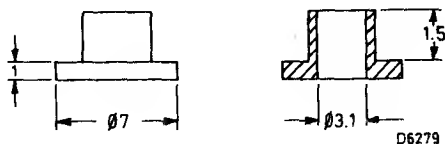
THERMAL RESISTANCE

From mounting base to heatsink $R_{th(mb-h)} = 2.5^{\circ}\text{C/W}$.

→ 56338 Insulating bush

MECHANICAL DATA

Dimension in mm



ABRIDGED DATA FOR EARLIER TYPES

D





ABRIDGED DATA FOR EARLIER TYPES

Abridged data only are given in these tables. Full data for these types are available on request
GERMANIUM TRANSISTORS

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C (mW)	h_{fe} at I_C			f_T min. (MHz)	$V_{CE(sat)}$ at I_B			Typical power gain at f	
			V_{CB} (V)	V_{CE} (V)	I_{CM} (mA)	$I_{C(AV)}$ (mA)	T_J (°C)		min.	max.	(mA)		max.	I_C (mA)	I_B (mA)	(dB)	(MHz)
ACY17	p-n-p	TO-5	-70	-60	2A	500	90	260	50**	150	300	1*	-0.35	500	25	—	—
ACY18	p-n-p	TO-5	-50	-40	2A	500	90	260	40**	120	300	1*	-0.35	500	25	—	—
ACY19	p-n-p	TO-5	-50	-40	2A	500	90	260	80**	250	300	1.3*	-0.35	500	25	—	—
ACY20	p-n-p	TO-5	-40	-32	2A	500	90	260	50**	145	50	1*	-0.2	50	1.3	—	—
ACY21	p-n-p	TO-5	-40	-32	2A	500	90	260	90**	250	50	1.3*	-0.2	50	1.3	—	—
ACY22	p-n-p	TO-5	-20	-20	2A	500	90	260	30**	300	300	1*	-0.35	500	25	—	—
ACY39	p-n-p	TO-5	-110	-75	2A	500	90	260	50**	150	300	1*	-0.35	500	25	—	—
ACY40	p-n-p	TO-5	-32	-32	2A	500	90	260	30**	70	300	0.8*	-0.35	500	25	—	—
ACY41	p-n-p	TO-5	-32	-32	2A	500	90	260	50**	250	300	0.6*	-0.35	500	25	—	—
ACY44	p-n-p	TO-5	-50	-40	2A	500	90	260	30	100	1	1*	-0.2	50	1.3	—	—
ADY26	p-n-p	TO-36	-80	-60	30A	25A	90	100W	40**	120	5A	—	-0.5	25A	2.5A	—	—
ADZ11	p-n-p	TO-36	-50	-40	20A	15A	90	45W	40**	120	1.2A	80kHz	-1.0	15A	2A	—	—
ADZ12	p-n-p	TO-36	-80	-60	20A	15A	90	45W	40**	120	1.2A	100kHz	-1.0	15A	2A	—	—
AF114	p-n-p	TO-7	-20	-20	10	10	75	85	40	—	1	75*	—	—	—	14	100
AF115	p-n-p	TO-7	-20	-20	10	10	75	85	40	—	1	75*	—	—	—	13	100
AF116	p-n-p	TO-7	-20	-20	10	10	75	85	40	—	1	75*	—	—	—	25	10.7
AF117	p-n-p	TO-7	-20	-20	10	10	75	85	40	—	1	75*	—	—	—	42	0.4
ASY26	p-n-p	TO-5	-30	-15	300	200	85	150	30**	80	20	4	-0.2	10	0.3	—	—
ASY27	p-n-p	TO-5	-25	-15	300	200	85	150	50**	150	20	6	-0.2	10	0.2	—	—
ASY28	n-p-n	TO-5	30	15	300	200	85	150	30**	80	20	4	0.2	10	0.3	—	—

*typical

** h_{FE}



GERMANIUM TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C (mW)	h_{fe} min. max.		at I_C (mA)	f_T min. (MHz)	$V_{CE(sat)}$ max. at I_C I_B		Typical Power gain at f		
			V_{CB} (V)	V_{CE} (V)	I_{CM} (mA)	$I_{C(AV)}$ (mA)	T_j (°C)		(d8)	(MHz)							
ASY29	n-p-n	TO-5	25	15	300	200	85	150	50**	150	20	10	0.2	10	0.2	—	—
ASZ21	p-n-p	TO-18	-20	-15	50	30	85	120	35	75	10	300	-0.35	10	1.0	—	—
OC20	p-n-p	TO-3	-100	-75	10A	8A	90	30W†	25	—	1A	0.25	—	—	—	—	—
OC22	p-n-p	TO-3	-47	-32	2A	1A	90	22.5W†	50**	—	1A	2	-0.6*	1A	30	—	—
OC23	p-n-p	TO-3	-55	-40	2A	1A	90	22.5W†	50**	—	1A	2.5	-0.4*	1A	30	—	—
OC24	p-n-p	TO-3	-47	-40	2A	1A	90	22.5W†	50**	—	1A	2.5	-0.4*	1A	30	—	—
OC25	p-n-p	TO-3	-40	-40	4A	4A	90	22.5W†	15**	80	1A	0.25	—	—	—	—	—
OC41	p-n-p	SO-2	-16	-15	150	50	75	112	20	90	10	3	-0.2	50	3	—	—
OC42	p-n-p	SO-2	-16	-15	150	50	75	112	40	—	10	5.5	-0.2	50	1.5	—	—
OC43	p-n-p	SO-2	-15	-15	150	50	75	112	50	200	50	12	-0.28	125	7	—	—
OC44	p-n-p	SO-2	-15	-15	10	5	75	70	40	225	1	7.5	-0.15	8	0.5	—	—
OC45	p-n-p	SO-2	-15	-15	10	5	75	70	25	125	1	3	-0.15	8	0.5	—	—
OC70	p-n-p	SO-2	-30	-30	50	10	75	125	20	40	0.5	5kHz	-0.33	9	0.5	—	—
OC71	p-n-p	SO-2	-30	-30	50	10	75	125	41	—	1	5kHz	-0.21	9	0.5	—	—
OC72	p-n-p	SO-2	-32	-32	250	125	75	125	45	120	10	0.33	—	—	—	—	—
OC75	p-n-p	SO-2	-30	-30	50	10	75	125	60	130	3	0.9	-0.21	9	0.5	—	—
OC76	p-n-p	SO-2	-32	-32	250	125	75	125	45	—	10	0.35	—	—	—	—	—
OC77	p-n-p	SO-2	-60	-60	250	125	75	125	45	—	10	0.35	—	—	—	—	—
OC139	n-p-n	SO-2	20	20	250	250	75	145	20	84	15	3.5	0.22	50	3	—	—
OC140	n-p-n	SO-2	20	20	400	400	75	145	50	150	15	4.5	0.22	50	1.2	—	—
OC141	n-p-n	SO-2	20	20	400	400	75	145	80	200	15	9.0	0.22	50	0.7	—	—
OC170	p-n-p	TO-7	-20	-20	10	10	75	85	40	—	1	75*	—	—	—	25	10
OC171	p-n-p	TO-7	-20	-20	10	10	75	85	40	—	1	75*	—	—	—	14	100

*typical

** h_{FE}

† $T_{case} \leq 25^\circ C$

‡ $T_{case} \leq 45^\circ C$

SILICON TRANSISTORS

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C (mW)	h_{FE} at I_C		f_T min. (MHz)	$V_{CE(sat)}$ at I_B			t_{on} t_{off} at		
			V_{CBO} (V)	V_{CEO} (V)	I_{CM} (mA)	$I_{C(AV)}$ (mA)	T_J (°C)		min.	max.		max.	I_C (mA)	I_B (mA)	(ns)	(ns)	(mA)
BC146	n-p-n	μ min.	20	20	50	50	125	50	80	550	0.2	150*	0.18*	2.0	—	—	—
BC186	p-n-p	TO-18	-40	-25	200	100	175	300	40	200	2.0	50	-0.5	50	5	—	—
BC187	p-n-p	TO-18	-30	-25	200	100	175	300	100	500	2.0	50	-0.5	50	5	—	—
BC200	p-n-p	μ min.	-20	-20	50	50	125	50	50	400	0.2	90*	-0.2*	2.0	—	—	—
§BCY55	n-p-n	Block	45	45	60	30	125	300	200	600	10	50	1.0	10	0.5	—	—
BCZ11	p-n-p	SO-2	-30	-25	100	50	150	250	15	50	20	0.9	-0.55	20	3	—	—
BD115	n-p-n	TO-39	245	180	200	150	200	6†	22	—	50	145*	9.0	100	10	—	—
BD121	n-p-n	TO-3	60	35	5A	5A	175	45W	30	—	1A	60	0.65	1A	100	—	—
BD123	n-p-n	TO-3	90	60	5A	5A	175	45W	30	—	1A	60	0.65	1A	100	—	—
BD124	n-p-n	SO-55	70	45	4A	2A	175	15W	35	—	500	60	0.50	2A	200	—	—
BDY10	n-p-n	TO-3	50	40	4A	2A	175	150W†	10	50	2A	1.0	0.7	2A	400	—	—
BDY11	n-p-n	TO-3	100	70	4A	2A	175	150W†	10	50	2A	1.0	0.7	2A	400	—	—
BDY60	n-p-n	TO-3	120	60	10A	5A	175	15W	45	450	500	100*	0.7	5A	500	120	350
BDY61	n-p-n	TO-3	100	60	10A	5A	175	15W	45	450	500	100*	0.9	5A	500	120	350
BDY62	n-p-n	TO-3	60	30	10A	5A	175	15W	45	450	500	100*	0.9	5A	500	120	350
BF115	n-p-n	TO-72	50	30	30	30	175	145	48	—	1	230*	—	—	—	—	—
BF167	n-p-n	TO-72	40	30	25	25	175	130	—	—	—	350*	—	—	—	—	—
BF173	n-p-n	TO-72	40	25	25	25	175	260	—	—	—	550*	—	—	—	—	—
BF177	n-p-n	TO-5	100	50	60	50	200	600	20	—	15	120*	—	—	—	—	—
BF178	n-p-n	TO-5	160	115	50	50	200	600	20	—	30	120*	—	—	—	—	—

*typical

† $T_{mb} \leq 25^\circ C$

§Dual transistor



SILICON TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C (mW)	h_{FE} at I_C			f_T min. (MHz)	$V_{CE(sat)}$ at I_C			t_{on} t_{off} at		
			V_{CBO} (V)	V_{CEO} (V)	I_{CM} (mA)	$I_{C(AV)}$ (mA)	T_j (°C)		min.	max.	(mA)		max.	I_C (mA)	I_B (mA)	(ns)	(ns)	(mA)
BF179	n-p-n	TO-5	250	115	50	50	200	500	20	—	20	120*	—	—	—	—	—	—
BF182	n-p-n	TO-72	25	20	15	15	175	150	—	—	—	650*	—	—	—	—	—	—
BF183	n-p-n	TO-72	25	20	15	15	175	150	—	—	—	800*	—	—	—	—	—	—
BF262	n-p-n	T pack	30	20	20	20	125	120	—	—	—	650*	—	—	—	—	—	—
BF263	n-p-n	T pack	30	20	20	20	125	120	—	—	—	525	—	—	—	—	—	—
BF264	n-p-n	T pack	30	20	20	20	125	120	—	—	—	400	—	—	—	—	—	—
BFS18R	n-p-n	μ min.	30	20	30	30	125	110	35	125	1.0	200*	—	—	—	—	—	—
BFS19R	n-p-n	μ min.	30	20	30	30	125	110	65	225	1.0	260*	—	—	—	—	—	—
BFS92	p-n-p	TO-39	100	-60	1A	1A	200	5W†	30	—	150	70*	-1.0	500	50	—	—	—
BFS93	p-n-p	TO-39	100	-60	1A	1A	200	5W†	70	—	150	70*	-1.0	500	50	—	—	—
BFS94	p-n-p	TO-39	-80	-40	1A	1A	200	5W†	40	—	150	70*	-0.7	500	50	—	—	—
BFS95	p-n-p	TO-39	-40	-35	1A	1A	200	5W†	70	—	150	70*	-0.7	500	50	—	—	—
BFW16	n-p-n	TO-5	40	25	300	150	200	1.5W‡	25	—	150	1200*	—	—	—	—	—	—
BFW17	n-p-n	TO-5	40	25	300	150	200	1.5W‡	25	—	150	1100*	—	—	—	—	—	—
BFW45	n-p-n	TO-39	165	130	100	50	200	2.5W‡	20	120	50	80	3.0	10	1	—	—	—
BFW57	n-p-n	Lock-fit	80	60	1A	500	125	350	80	—	100	80	0.7	500	50	—	—	—
BFW58	n-p-n	Lock-fit	80	60	1A	500	125	350	50	—	100	80	0.7	500	50	—	—	—
BFW59	n-p-n	Lock-fit	40	35	1A	500	125	350	80	—	100	80	0.7	500	50	—	—	—
BFW60	n-p-n	Lock-fit	40	35	1A	500	125	350	50	—	100	80	0.7	500	50	50	290	100
BFW87	p-n-p	Lock-fit	-60	-60	500	500	125	300	80	320	150	100	-0.4	150	15	—	—	—

*typical ‡ $T_{case} \leq 125^\circ C$ † $T_{mb} \leq 50^\circ C$

SILICON TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C (mW)	h_{FE} at			f_T min. (MHz)	$V_{CE(\text{sat})}$ at			t_{on} (ns)	t_{off} (ns)	at (mA)
			V_{CBO}	V_{CEO}	I_{CM}	$I_{C(AV)}$	T_j		min.	max.	I_C		I_B					
			(V)	(V)	(mA)	(mA)	(°C)		(mA)				(V)	(mA)	(mA)			
BFW88	p-n-p	Lock-fit	-60	-60	500	500	125	300	40	130	150	100	-0.4	150	15	50	290	100
BFW89	p-n-p	Lock-fit	-40	-40	500	500	125	300	80	320	150	100	-0.4	150	15	50	290	100
BFW90	p-n-p	Lock-fit	-40	-40	500	500	125	300	40	120	150	100	-0.4	150	15	50	290	100
BFW91	p-n-p	Lock-fit	-20	-20	500	500	125	300	40	125*	150	100	-0.4	150	15	50	290	100
BFW92	n-p-n	T pack	25	15	50	25	125	130	20	150	2.0	1600*	0.75	20	—	—	—	—
BFX12	p-n-p	TO-18	-20	-15	140	100	200	300	20	60	10	150	-0.25	10	1	—	—	—
BFX13	p-n-p	TO-18	-20	-15	140	100	200	300	50	250	10	150	-0.25	10	1	—	—	—
BFX34	n-p-n	TO-39	120	60	5A	2A	200	870	40	150	2A	70	1.0	5A	500	210	340	5A
BFX37	p-n-p	TO-18	-60	-60	50	50	200	360	100	170*	10	—	-0.25	10	0.5	—	—	—
BLY17	n-p-n	TO-36	100	100**	10A	10A	175	100W†	5	—	5A	50	2.0	10A	2A	—	—	—
BSS27	n-p-n	TO-39	70	45	1A	1A	200	800	25	—	500	400*	0.4	500	35	25	40	500
BSS28	n-p-n	TO-39	50	30	1A	1A	200	800	30	—	500	400*	0.5	500	35	25	45	500
BSS29	n-p-n	TO-39	50	30	1A	1A	200	800	20	—	500	400*	0.5	500	35	30	50	500
BSW41	n-p-n	TO-18	40	25	500	300	200	1W	20	—	500	250	0.5	150	15	50	100	300
BSW65	n-p-n	TO-5	80	80	2A	1A	200	800	40	—	100	80*	0.4	500	5.0	—	—	—
BSW69	n-p-n	Plastic	150	150	50	50	125	125	30	—	4	130*	4.0	20	1.0	—	—	—
BSX12	n-p-n	TO-39	25	12	1A	1A	200	3W‡	30	120	300	450	0.33	300	30	11	19	1A
BSX12A	n-p-n	TO-39	25	15	1A	1A	200	3W‡	30	120	300	450	0.33	300	30	11	19	1A
BSX44	n-p-n	TO-18	15	6	200	—	200	300	30	150	20	600	0.45	50	5.0	20	15	20
BSX76	n-p-n	TO-18	20	20	400	200	200	350	35	—	10	50	0.35	50	2.5	40	80	100
*typical ** $V_{CE} = (P_{CE} < 100\text{mW})$ † $T_j = 125^\circ\text{C}$ ‡ $T_j = 175^\circ\text{C}$																		

*typical

** V_{CER} ($R_{BE} \leq 10\Omega$)

† $T_{mb} \leq 25^\circ\text{C}$

‡ $T_{case} \leq 95^\circ\text{C}$



SILICON TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C (mW)	h_{FE} at I_C			f_T min. (MHz)	$V_{CE(sat)}$ at I_C			t_{on} t_{off} at		
			V_{CBO} (V)	V_{CEO} (V)	I_{CM} (mA)	$I_{C(AV)}$ (mA)	T_j (°C)		min.	max.	(mA)		max.	I_C (mA)	I_B (mA)	(ns)	(ns)	(mA)
BSX77	n-p-n	TO-18	40	20	400	200	200	350	40	120	10	100	0.35	50	2.5	40	80	100
BSX78	n-p-n	TO-18	40	20	400	200	200	350	80	240	10	100	0.35	50	2.5	40	80	100
BSY26	n-p-n	TO-18	20	15	200	100	175	300	20	60	10	200	0.35	10	1	27	130	10
BSY27	n-p-n	TO-18	20	15	200	100	175	300	40	120	10	200	0.35	10	1	27	130	10
BSY38	n-p-n	TO-18	20	15	200	100	175	300	15	45	100	350*	0.6	100	10	14	45	100
BSY39	n-p-n	TO-18	20	15	200	100	175	300	20	70	100	350*	0.6	100	10	14	45	100
BSY40	p-n-p	TO-18	-25	-20	140	100	200	300	25	60	10	140	-0.2	10	1	25	100	50
BSY41	p-n-p	TO-18	-25	-20	140	100	200	300	50	200	10	140	-0.2	10	1	25	100	50
BSY95	n-p-n	TO-18	20	15	200	100	140	150	50	200	10	200	-0.35	10	0.2	—	—	—
BU105	n-p-n	TO-3	1500	1500	2.5A	2.5A	115	10W	—	—	—	7.5*	5.0	2.5A	1.5A	—	750	2A
OC200	p-n-p	SO-2	-30	-25	100	50	150	250	10	50	20	0.45	-0.55	20	3	—	—	—
OC201	p-n-p	SO-2	-25	-20	100	50	150	250	10	70	20	2.0	-0.55	20	3	—	—	—
OC202	p-n-p	SO-2	-15	-10	100	50	150	250	24	125	20	1.4	-0.55	20	3	—	—	—
OC203	p-n-p	SO-2	-60	-50	100	50	150	250	10	50	20	0.3	-0.55	20	3	—	—	—
OC204	p-n-p	SO-2	-32	-32	500	250	150	125	10	30	150	0.45	-0.56	125	17	—	—	—
OC205	p-n-p	SO-2	-60	-60	500	250	150	125	10	50	150	0.45	-0.56	125	17	—	—	—
OC206	p-n-p	SO-2	-32	-32	500	250	150	125	16	120	150	0.85	-0.55	125	17	—	—	—
OC207	p-n-p	SO-2	-50	-50	500	250	150	310	12	70	150	2.0	-0.56	150	17	—	—	—

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Type Number	Part/ Section	Suggested alternative	Type Number	Part/ Section	Suggested alternative
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AC128/AC176	1B		BCY72	1B	
AC176	1B		BCY87/8/9	1B	
AC187	1B		BCZ11	D*	
AC188	1B		BD115	D*	
ACY17 to 22	D*	AC128	BD121/3	D*	BDY92/60
ACY39 to 41	D*	AC128	BD124	D*	
ACY44	D*		BD131/2-BD131	1B	
AD140/2-AD140	*	AD149	BD132	1B	
AD149/2-AD149	1B		BD133	1B	
AD161	1B		BD135 to 140	1B	
AD161/2	1B		BD181 to 184	1B	
AD162	1B		BD201 to 204	1B	
ADY26	D*		BD232	1B	
ADZ11/12	D*		BD233 to 238	1B	
AF114 to 117	D*		BD262/A/B	1B	
AFY19	*	BFX88	BD263/A/B	1B	
ASY26 to 29	D*		BD433 to 438	1B	
ASY67	*	BCY70	BDX35/6/7	1B	
ASZ20	*	BCY70	BDX42/3/4	1B	
ASZ21	D*		BDX62/A/B	1B	
ASZ23	*	BCY70	BDX63/A/B	1B	
BC107/8/9	1B		BDX64/A/B	1B	
BC146	D*	BCW32R	BDX65/A/B	1B	
BC147/8/9	1B		BDY10/11	D*	BDY20
BC157/8/9	1B		BDY20/2-BDY20	1B	
BC186/7	D*	BCY70	BDY38/2-BDY38	1B	
BC200	D*	BCW30R	BDY60/1/2	D*	
BC327/8	1B		BDY90 to 95	1B	
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BCW69R to 72R	1B		BF180	1B	
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BCY30/1/2/3/4	1B		BF195	1B	
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BCY54	1B		BF197	1B	
BCY55	D*	BCY87	BF200	1B	

*Not recommended for the design of new equipment.
Full data for these types are available on request.

Type Number	Part/ Section	Suggested alternative	Type Number	Part/ Section	Suggested alternative
BF245A/B/C	1B	BF362/3	BFY50/1/2	2B	
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BF264	D*		BFY90	2B	
BF324	1B		BGY22/A	2B	
BF336/7/8	1B		BGY23/A	2B	
BF355	1B		BLX13	2B	
BF362/3	1B		BLX14	2B	
BF450/1	1B		BLX65	2B	
BFQ10 to 16	2B		BLX66	2B	
BFR29	2B		BLX67	2B	
BFR30/1	2B	BFS20R	BLX69	2B	BLX14
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BFR91	2B		BLX93	2B	
BFR92	2B		BLX94	2B	
BFR93	2B		BLY17	D*	
BFS17R	2B		BLY33/4	2B	
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BFS21/21A	2B		BLY53A	2B	
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BFW16A	2B	BFW17A	BLY93A	2B	
BFW17	D*		BLY94	2B	
BFW17A	2B		BLY97	2B	
BFW30	2B		BRY39	2B	
BFW45	D*	BSX21	BSS27/8/9	D*	BFR29/BSV81
BFW57/8/9/60	D*	BCX32-34	BSS40/1	2B	
BFW61	2B	BFXB5	BSS50/1/2	2B	
BFW87 to 91	D*		BSV22	D*	
BFW92	D*		BSV52R	2B	
BFW96	D*	BFR29/BSV81	BSV64	2B	BFX85
BFX12/13	D*	BCY70	BSV68	2B	
BFX29	2B	BSV64	BSV7B/9/80	2B	
BFX30	2B		BSV81	2B	
BFX34	D*		BSW41	D*	
BFX37	D*	BCY70	BSW65	D*	
BFX63	D*	BFR29/BSV81	BSW66/7/B	2B	
BFX84/5/6	2B		BSW69	D*	
BFX87/8	2B		BSX12/12A	D*	
BFX89	2B		BSX19/20	2B	
			BSX21	2B	

*Not recommended for the design of new equipment.
Full data for these types are available on request.

Type Number	Part/ Section	Suggested alternative	Type Number	Part/ Section	Suggested alternative
BSX44	D*	BSX19 BFR29/BSVB1 BSX19/20	2N3375	2B	
BSX59/60/61	2B		2N3442	2B	
BSX76/7/8	D*		2N3553	2B	
BSXB2	D*		2N3632	2B	
BSY26/7	D*		2N3823	2B	
BSY38/9	D*	BCY70	2N3866	2B	
BSY40/1	D*		2N3966	2B	
BSY95	D*		2N4091/2/3	2B	
BSY95A	2B		2N4347	2B	
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OC26	*		56207	C	
OC28/9	2B		56209	C	
OC35/6	2B		56214	C	
OC41/2/3/4/5	D*		5621B	C	
OC70/1/2	D*		56226	C	
OC75/6/7	D*	AC128 BFX87	56227	C	
OC122/3	*		56239A	C	
OC139/40/41	D*		56239B	C	
OC170/1	D*		56245	C	
OC200 to 207	D*		56246	C	
2N1613	2B		56263	C	
2N1711	2B		56265	C	
2N2297	2B		56300	C	
2N2369A	2B		56301B	C	
2N2904/4A	2B		56325	C	
2N2905/5A	2B		56326	C	
2N2906/6A	2B		56336A	C	
2N2907/7A	2B		56336B	C	
2N3053	2B		56338	C	
2N3055	2B				

*Not recommended for the design of new equipment.
Full data for these types are available on request.

TRANSISTORS

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